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B	Added SDA / SCL Pull-Up Requirement		9-03-13

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN9303M, 72-pin QFN Package

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Document Number	Revision
SC471223	B

Schematic Checklist for LAN9303M

Information Particular for the 72-pin QFN Package

The LAN9303M provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9303M provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the MII interface. In PHY mode, the device can be connected to an external MAC via the RMII/MII interface. Optionally, the internal PHY on Port 1 can be disabled and the associated Switch Fabric port operated in the MII PHY, RMII PHY, or MII MAC modes. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The eight possible combinations for the 3 ports are illustrated in the following block diagram. This schematic checklist is organized such that checking a LAN9303M schematic should be very straight forward. Upon deciding the configuration required for each block as per the application, the sections that follow the block diagram outline each port. Each possible configuration is described in each of the port sections.

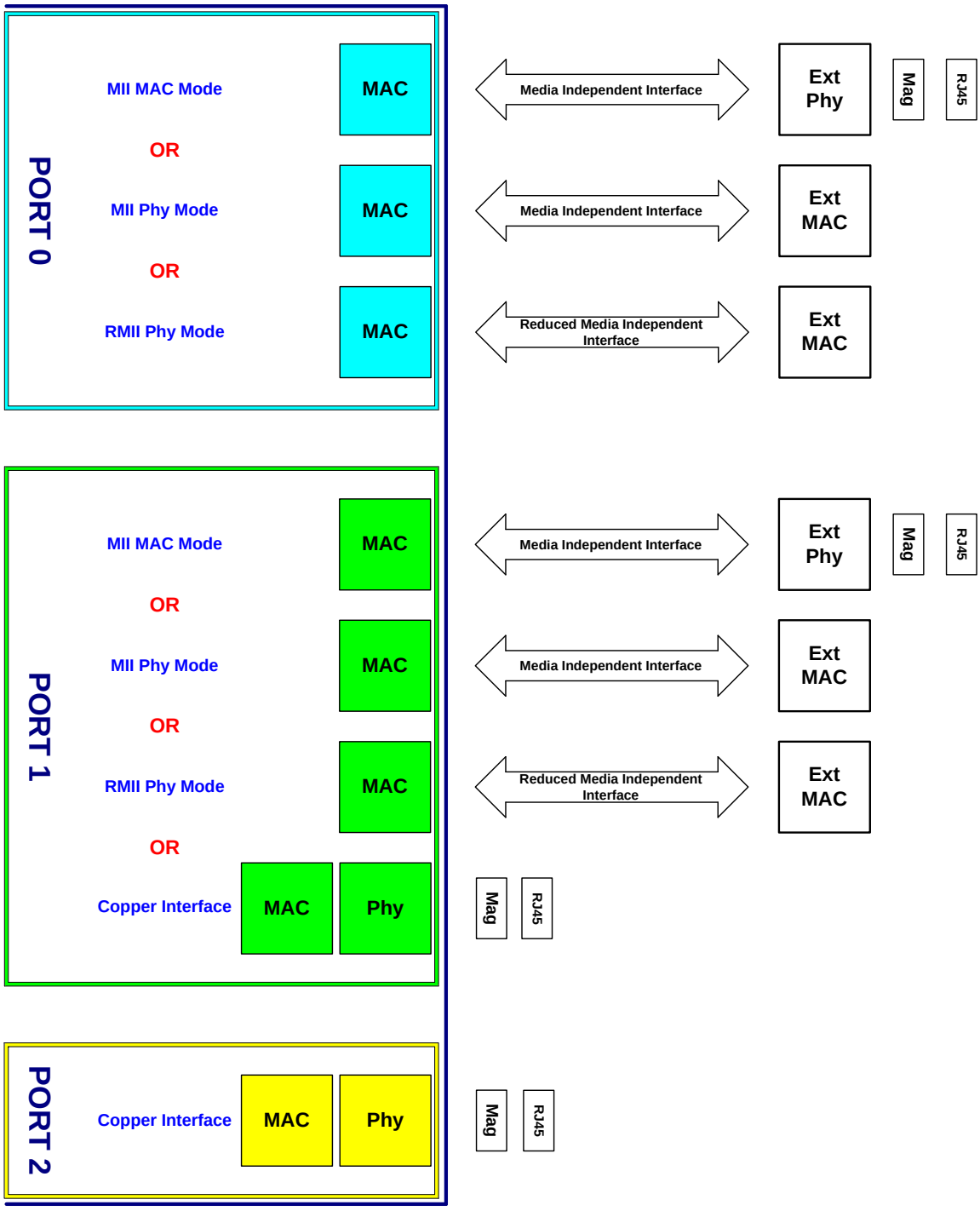


Figure 1 LAN9303M Block Diagram

Port 0 Configurations

Port 0 Configuration Straps:

1. P0_MODE2, P0_MODE1, P0_MODE0 (pins 10, 11 & 12), these three straps configure the mode of Port 0. These pins have weak internal pull-ups and can be driven low with an external 10.0K Ω resistor to digital ground. The possible modes for Port 0 are as follows:

Port 0 Mode Configuration Straps			
P0_MODE[2..0]	**Mode**	**Speed**	**Clock**
000	MII MAC Mode	100 Mbps	
001	MII Phy Mode	100 Mbps	
010	MII Phy Mode	200 Mbps	12 mA Output
011	MII Phy Mode	200 Mbps	16 mA Output
100	RMII Phy Mode	100 Mbps	12 mA Output
101	RMII Phy Mode	100 Mbps	16 mA Output
110	RMII Phy Mode	100 Mbps	Input
111	Reserved		

2. P0_DUPLEX (pin 25), this input sets the Duplex operation of Port 0. The value can be changed at any time (live value) and can be overridden by disabling the Auto Negotiation (VPHY_AN) bit in the Virtual PHY Basic Control register. In MAC mode, this pin is typically tied to the duplex indication from the external Phy. In PHY mode, this signal is typically held high or low as required. The polarity of this signal depends upon the DUPLEX_POL_0 pin. If the DUPLEX_POL_0 pin is zero, a P0_DUPLEX value of zero indicates Full Duplex and a one indicates Half Duplex operation. If DUPLEX_POL_0 is one, a P0_DUPLEX value of one indicates Full Duplex and a zero indicates Half Duplex operation. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

3. DUPLEX_POL_0 (pin 9), this strap selects the default of the duplex polarity strap for Port 0 MII (duplex_pol_strap_0). If the strap value is zero, a zero on P0_DUPLEX means full duplex, while a one indicates half duplex. If the strap value is one, then a one on P0_DUPLEX means full duplex, while a zero indicates half duplex. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Port 0 MII MAC Mode:

The following diagram shows each of the pins on the Port 0 MII MAC Interface of the LAN9303M device. The design engineer should always double check his connections and make sure that outputs from the LAN9303M device are driving inputs on the target device. Also, check that inputs on the LAN9303M are being driven from outputs on the target device.

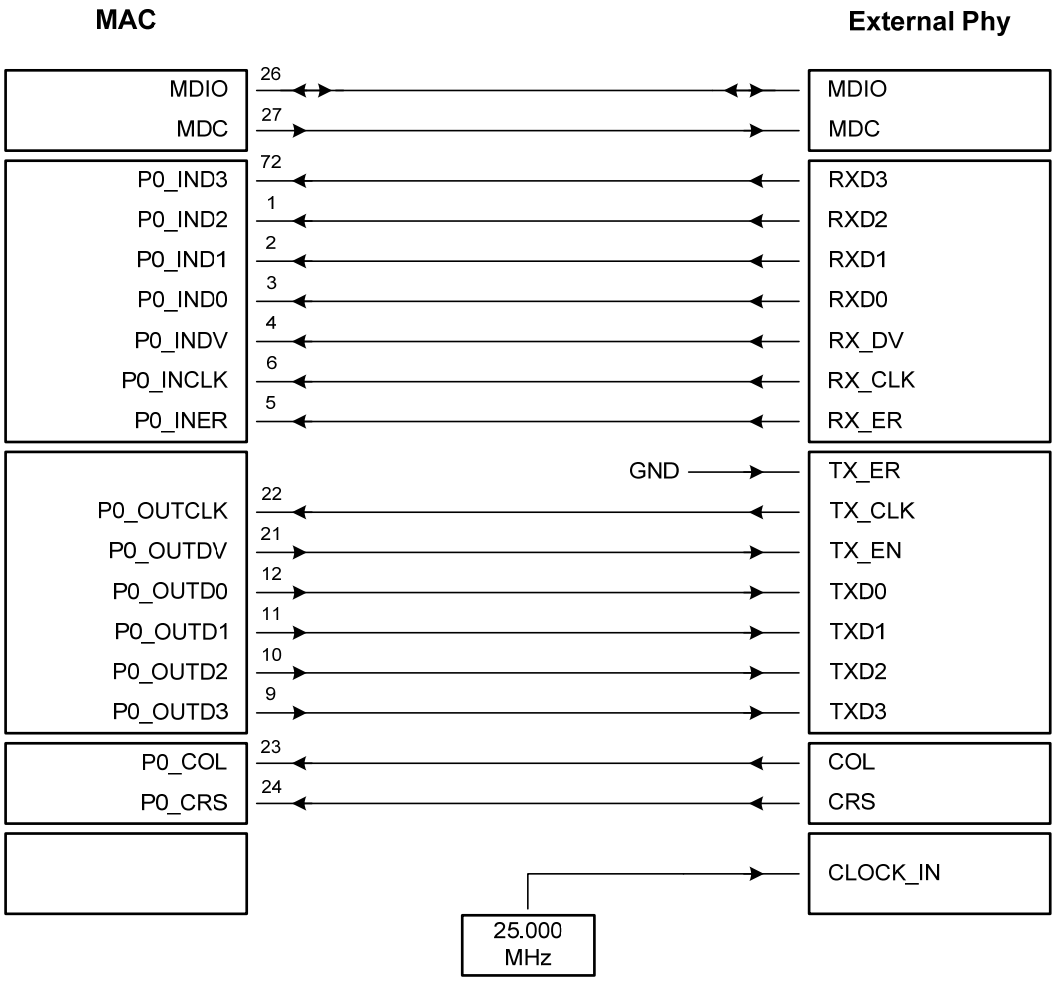


Figure 2 LAN9303M MII MAC Mode

The 25.000 MHz clock supplied to the external Phy provides the TX_CLK and RX_CLK clocks to the MAC in the LAN9303M.

Port 0 MII Phy & MII Turbo Phy Mode:

The following diagram shows each of the pins on the Port 0 MII Phy Interface of the LAN9303M device. The design engineer should always double check his connections and make sure that outputs from the LAN9303M device are driving inputs on the target device. Also, check that inputs on the LAN9303M are being driven from outputs on the target device.

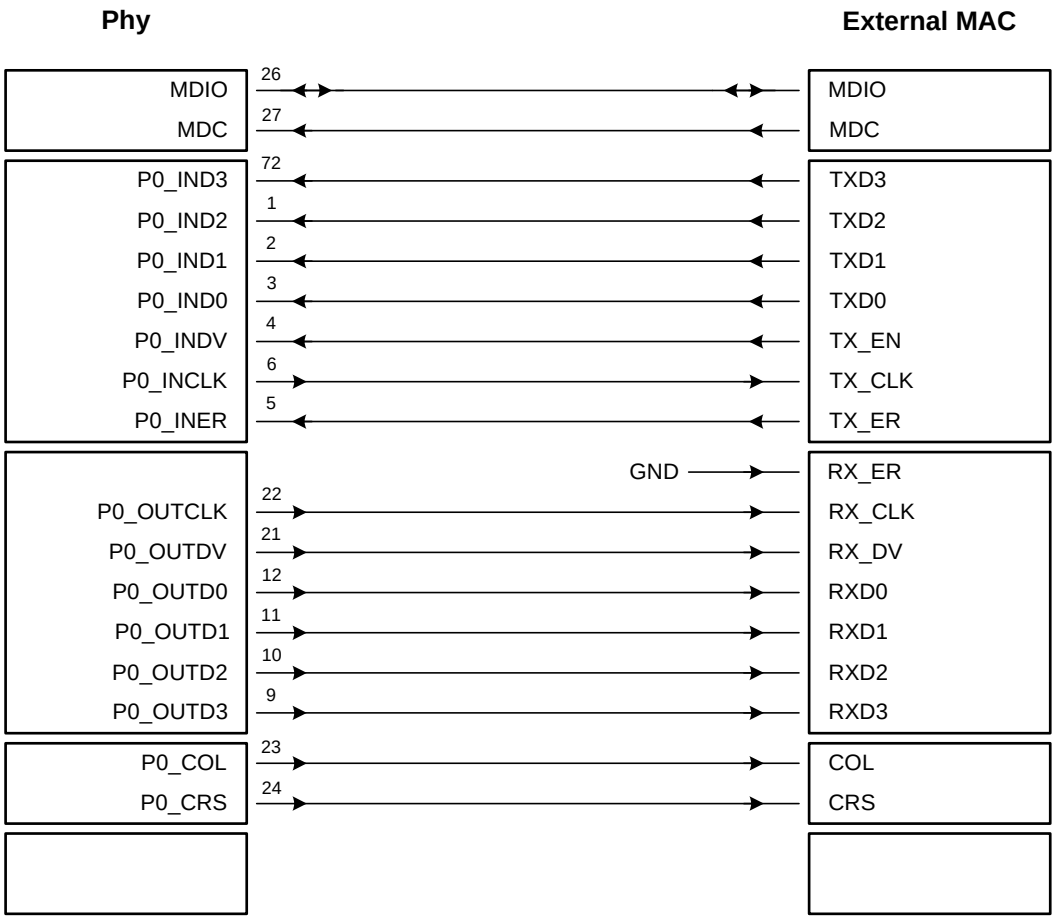


Figure 3 LAN9303M MII Phy Mode

The TX_CLK and RX_CLK clocks are supplied to the external MAC from the LAN9303M.

Port 0 RMII Phy Mode:

The following diagram shows each of the pins on the Port 0 RMII Phy Interface of the LAN9303M device. The design engineer should always double check his connections and make sure that outputs from the LAN9303M device are driving inputs on the target device. Also, check that inputs on the LAN9303M are being driven from outputs on the target device.

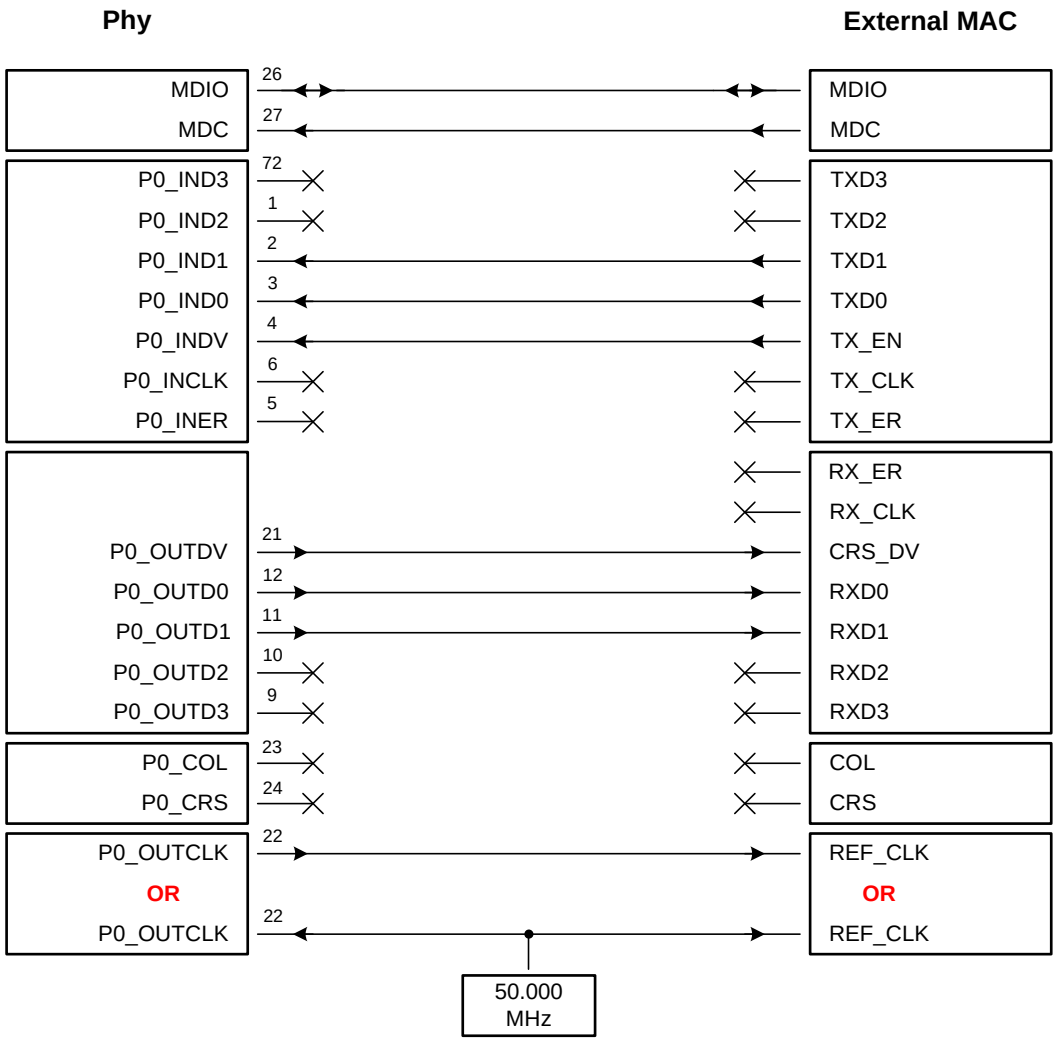


Figure 4 LAN9303M RMII Phy Mode

The 50.000 MHz RMII Reference Clock can be configured in one of two ways. An external 50.000 MHz clock oscillator can be supplied to both the LAN9303M and the target MAC. The other option is to have the LAN9303M output the 50.000 MHz Reference Clock to the target MAC.

Port 1 Configurations

Port 1 Configuration Straps:

1. P1_MODE2, P1_MODE1, P1_MODE0 (pins 39, 44 & 45), these three straps configure the mode of Port 1. These pins have weak internal pull-ups and can be driven low with an external 10.0K Ω resistor to digital ground. The possible modes for Port 1 are as follows:

Port 1 Mode Configuration Straps			
P1_MODE[2..0]	**Mode**	**Speed**	**Clock**
000	MII MAC Mode	100 Mbps	
001	MII Phy Mode	100 Mbps	
010	MII Phy Mode	200 Mbps	12 mA Output
011	MII Phy Mode	200 Mbps	16 mA Output
100	RMII Phy Mode	100 Mbps	12 mA Output
101	RMII Phy Mode	100 Mbps	16 mA Output
110	RMII Phy Mode	100 Mbps	Input
111	Internal Phy Mode		

2. P1_DUPLEX (pin 35), this input sets the Duplex operation of Port 1. The value can be changed at any time (live value) and can be overridden by disabling the Auto Negotiation (VPHY_AN) bit in the Virtual PHY Basic Control register. In MAC mode, this pin is typically tied to the duplex indication from the external Phy. In PHY mode, this signal is typically held high or low as required. The polarity of this signal depends upon the DUPLEX_POL_1 pin. If the DUPLEX_POL_1 pin is zero, a P1_DUPLEX value of zero indicates Full Duplex and a one indicates Half Duplex operation. If DUPLEX_POL_1 is one, a P1_DUPLEX value of one indicates Full Duplex and a zero indicates Half Duplex operation. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

3. DUPLEX_POL_1 (pin 38), this strap selects the default of the duplex polarity strap for Port 1 MII (duplex_pol_strap_1). If the strap value is zero, a zero on P1_DUPLEX means full duplex, while a one indicates half duplex. If the strap value is one, then a one on P1_DUPLEX means full duplex, while a zero indicates half duplex. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Port 1 MII MAC Mode:

The following diagram shows each of the pins on the Port 1 MII MAC Interface of the LAN9303M device. The design engineer should always double check his connections and make sure that outputs from the LAN9303M device are driving inputs on the target device. Also, check that inputs on the LAN9303M are being driven from outputs on the target device.

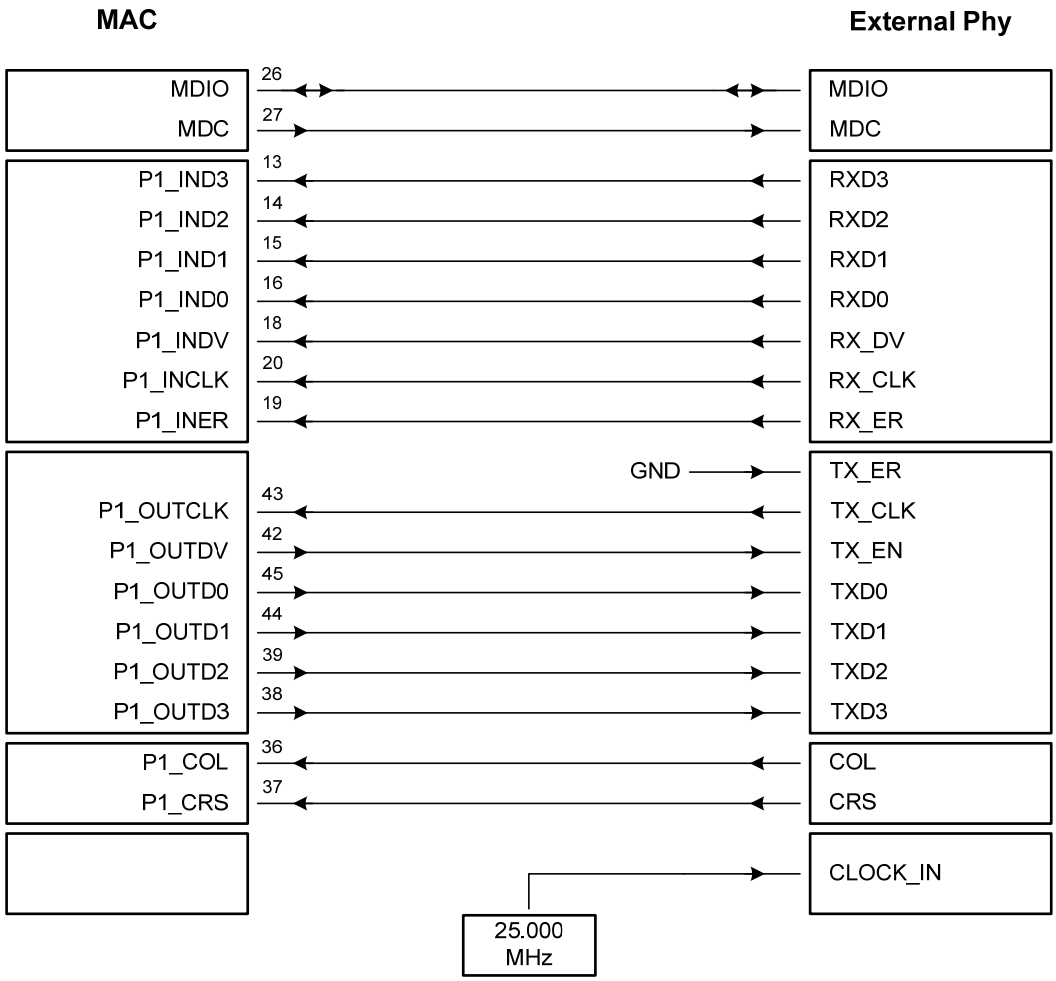


Figure 5 LAN9303M MII MAC Mode

The 25.000 MHz clock supplied to the external Phy provides the TX_CLK and RX_CLK clocks to the MAC in the LAN9303M.

Port 1 MII Phy & MII Turbo Phy Mode:

The following diagram shows each of the pins on the Port 1 MII Phy Interface of the LAN9303M device. The design engineer should always double check his connections and make sure that outputs from the LAN9303M device are driving inputs on the target device. Also, check that inputs on the LAN9303M are being driven from outputs on the target device.

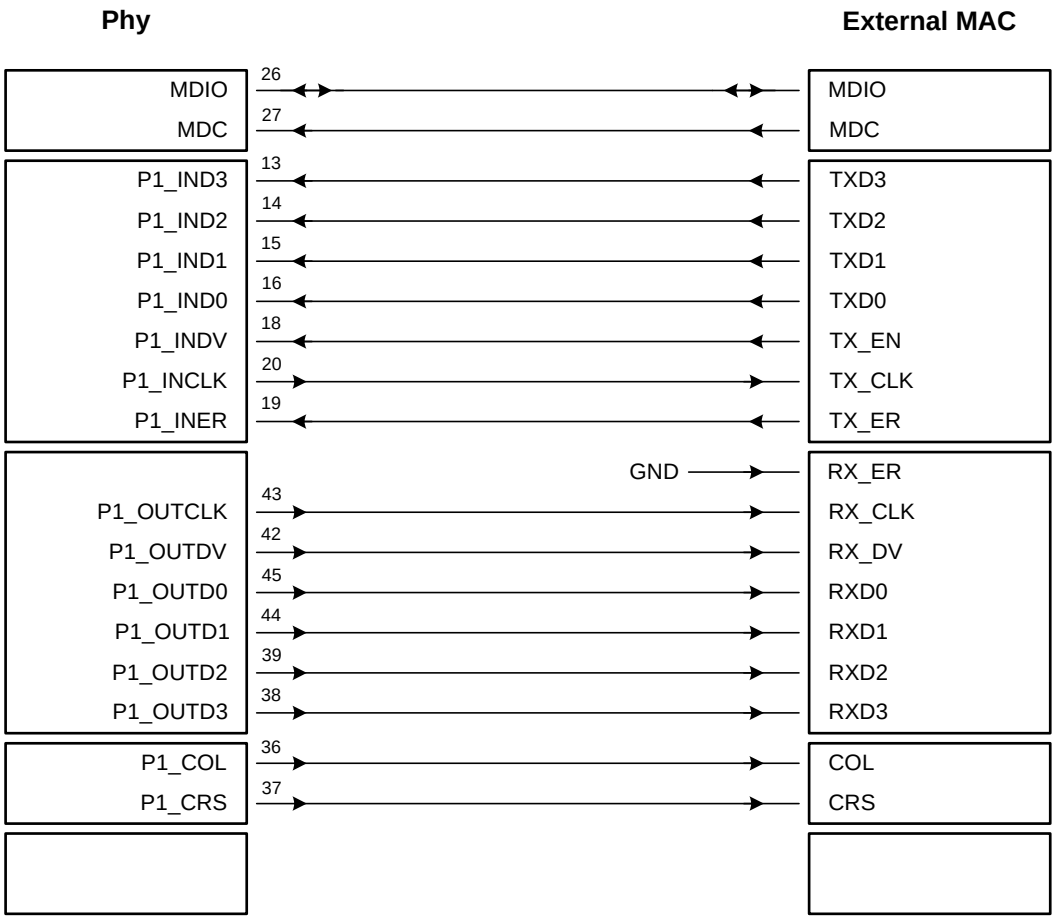


Figure 6 LAN9303M MII Phy Mode

The TX_CLK and RX_CLK clocks are supplied to the external MAC from the LAN9303M.

Port 1 RMII Phy Mode:

The following diagram shows each of the pins on the Port 1 RMII Phy Interface of the LAN9303M device. The design engineer should always double check his connections and make sure that outputs from the LAN9303M device are driving inputs on the target device. Also, check that inputs on the LAN9303M are being driven from outputs on the target device.

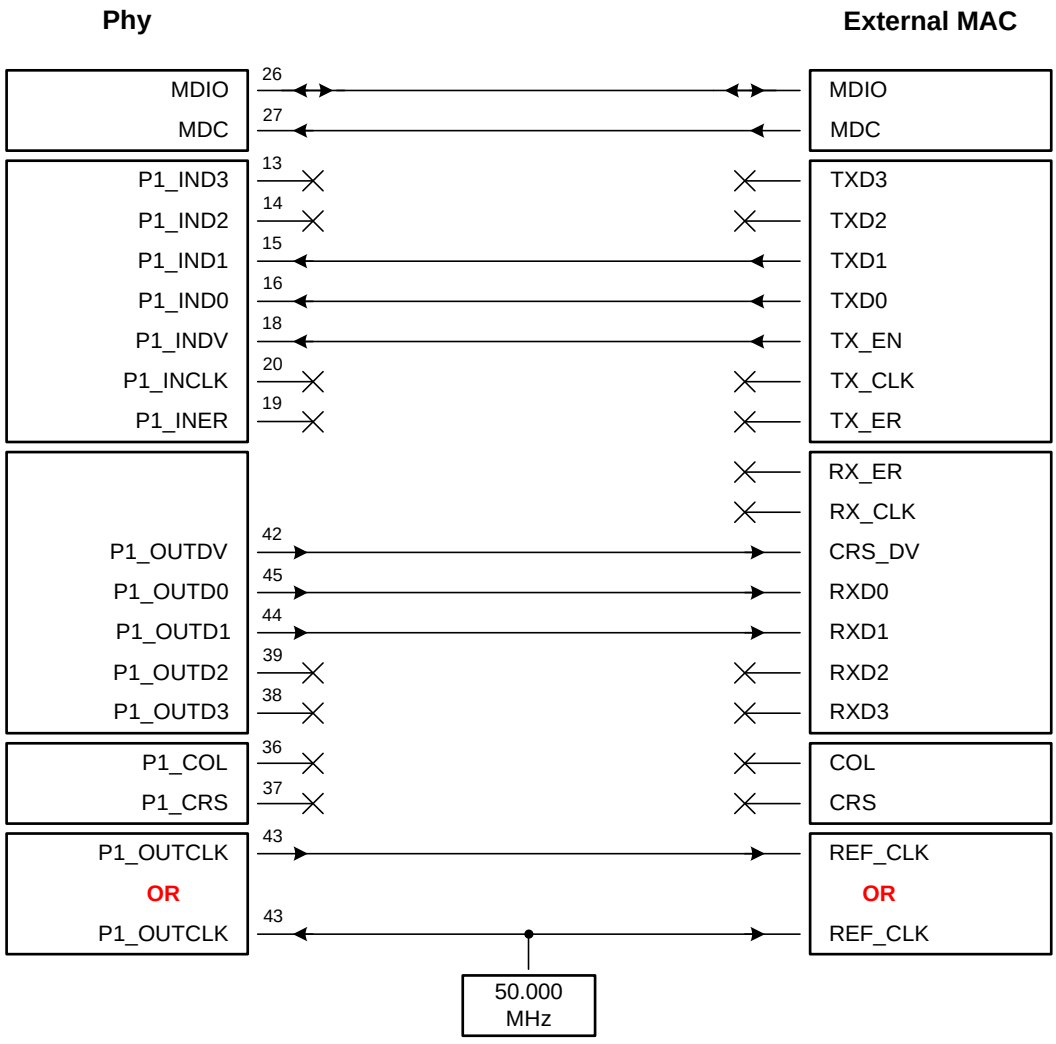


Figure 7 LAN9303M RMII Phy Mode

The 50.000 MHz RMII Reference Clock can be configured in one of two ways. An external 50.000 MHz clock oscillator can be supplied to both the LAN9303M and the target MAC. The other option is to have the LAN9303M output the 50.000 MHz Reference Clock to the target MAC.

LAN9303M QFN Phy No. 1 Interface:

1. TXP1 (pin 57); This pin is the transmit twisted pair output positive connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.

2. TXN1 (pin 56); This pin is the transmit twisted pair output negative connection from the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the transmit channel of the primary magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 8.

4. RXP1 (pin 60); This pin is the receive twisted pair input positive connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.

5. RXN1 (pin 59); This pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A1 (created from +3.3V). This pin also connects to the receive channel of the primary magnetics.

6. For Receive Channel connection and termination details, refer to Figure 9.

LAN9303M QFN Phy No. 2 Interface:

1. TXP2 (pin 70); This pin is the transmit twisted pair output positive connection from the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.

2. TXN2 (pin 71); This pin is the transmit twisted pair output negative connection from the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the transmit channel of the secondary magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 8.

4. RXP2 (pin 67); This pin is the receive twisted pair input positive connection to the secondary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.

5. RXN2 (pin 68); This pin is the receive twisted pair input negative connection to the primary internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A2 (created from +3.3V). This pin also connects to the receive channel of the secondary magnetics.

6. For Receive Channel connection and termination details, refer to Figure 9.

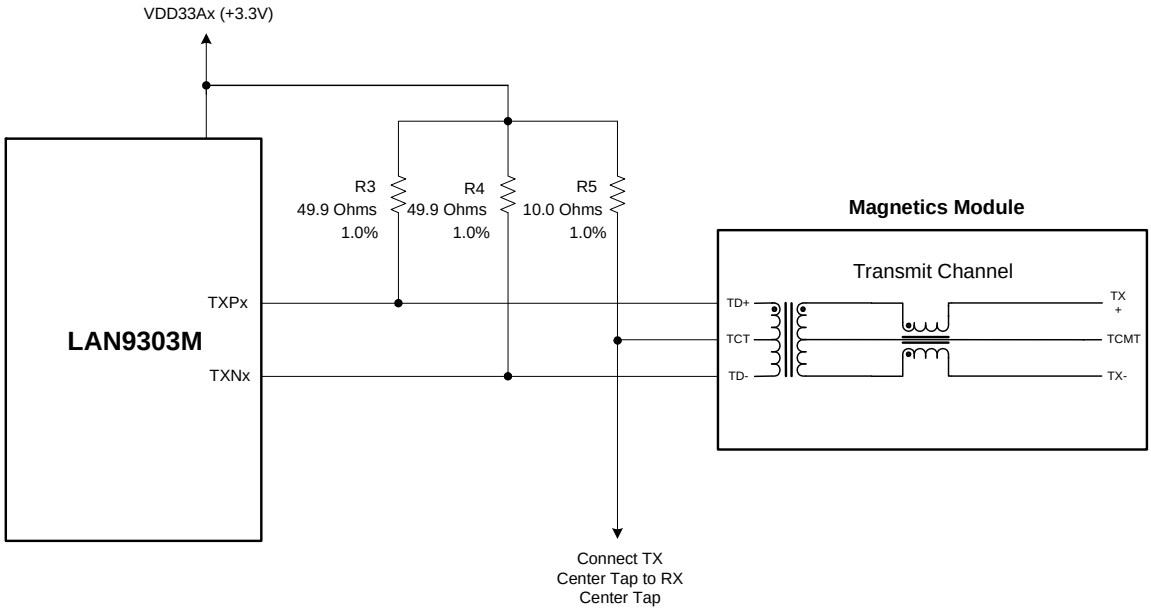


Figure 8 – Transmit Channel Connections and Terminations

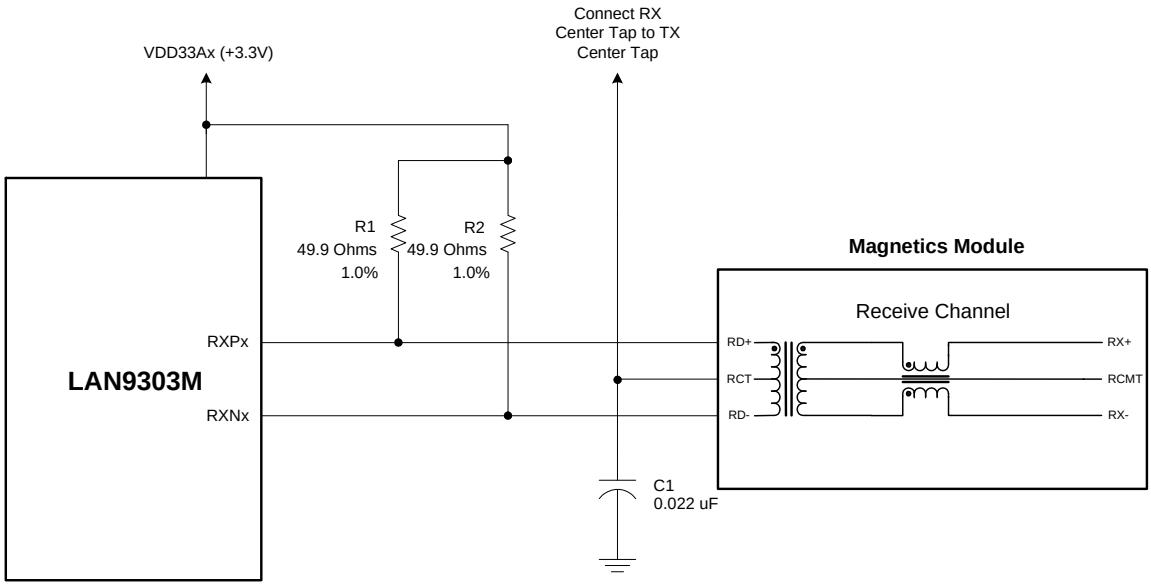


Figure 9 - Receive Channel Connections and Terminations

LAN9303M QFN Magnetic No. 1:

1. The center tap connection on the LAN9303M side for the transmit channel must be connected to VDD33A1 (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the primary magnetics also connects to the receive channel center tap of the primary magnetics.

2. The center tap connection on the LAN9303M side for the receive channel is connected to the transmit channel center tap on the primary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the primary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the primary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the primary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP1 (pin 57) of the LAN9303M QFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN1 (pin 56) of the LAN9303M QFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP1 (pin 60) of the LAN9303M QFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN1 (pin 59) of the LAN9303M QFN.

10. When using the SMSC LAN9303x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required.

LAN9303M QFN Magnetic No. 2:

1. The center tap connection on the LAN9303M side for the transmit channel must be connected to VDD33A2 (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the secondary magnetics also connects to the receive channel center tap of the secondary magnetics.

2. The center tap connection on the LAN9303M side for the receive channel is connected to the transmit channel center tap on the secondary magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the secondary magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the secondary transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the secondary receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP2 (pin 70) of the LAN9303M QFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN2 (pin 71) of the LAN9303M QFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP2 (pin 67) of the LAN9303M QFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN2 (pin 68) of the LAN9303M QFN.

10. When using the SMSC LAN9303x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required.

RJ45 Connector No. 1 & No. 2:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The digital supply (VDD33IO) pins on the LAN9303M QFN are 7, 17, 28, 40 & 46. They require a connection to +3.3V.

2. Each VDD33IO power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9303M. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33A1) pins for Phy No. 1 on the LAN9303M QFN are pins 58 & 61. They require a connection to +3.3V through one ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD33A1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9303M. The capacitor size should be SMD_0603 or smaller.

5. The analog supply (VDD33A2) pins for Phy No. 2 on the LAN9303M QFN are pins 66 & 69. They require a connection to +3.3V through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

6. Each VDD33A2 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9303M. The capacitor size should be SMD_0603 or smaller.

7. VDD33BIAS (pin 64), this pin serves as the master bias voltage supply for the LAN9303M. This pin requires a connection to +3.3V through a third ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

8. The VDD33BIAS pin should have one .01 μF (or smaller) capacitor to decouple the LAN9303M. The capacitor size should be SMD_0603 or smaller.

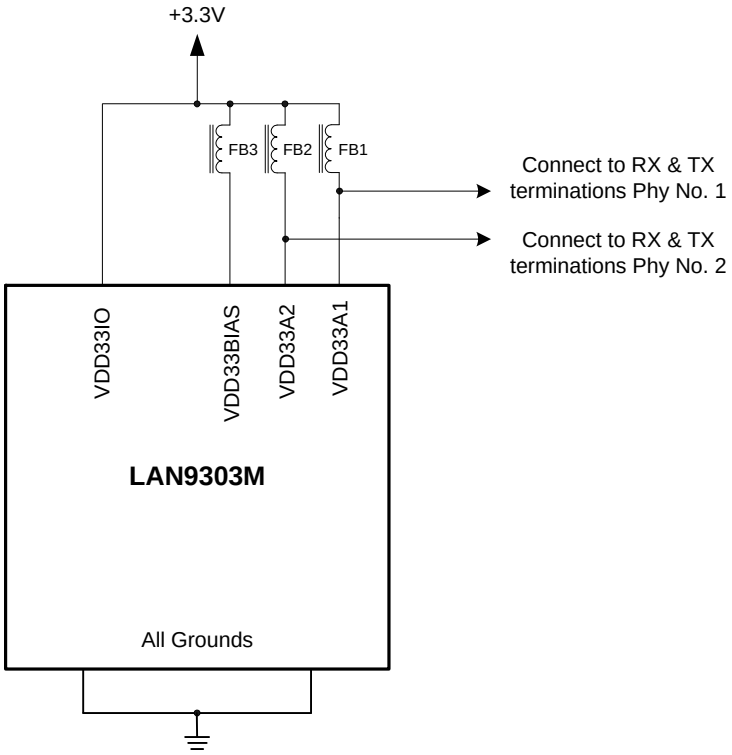


Figure 10 – LAN9303M +3.3V Power Connections

VDD18CORE:

1. VDD18CORE (pins 8 & 41), these two pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF bypass capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 41 requires a bulk capacitor placed as close as possible to pin 41. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 1.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9303M use only. **Do Not** power other circuits or devices with this supply.

2. VDD18PLL (pin 55), this pin supplies power for the core PLL. This pin must be connected to VDD18CORE through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD18PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN9303M. The capacitor size should be SMD_0603 or smaller.

4. **Do Not**, under any circumstances, connect VDD18CORE to VDD18TX2. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9303M.

5. **Do Not**, under any circumstances, use either VDD18CORE or VDD18TX2 to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9303M only.

VDD18TX2:

1. VDD18TX2 (pin 65), this pin is used to provide bypassing for the +1.8V PHY regulator. This pin requires a 0.01 μF bypass capacitor. This capacitor should be located as close as possible to its pin without using vias. In addition, pin 65 requires a bulk capacitor placed as close as possible to pin 65. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 1.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only and LAN9303M use only. **Do Not** power other circuits or devices with this supply.

2. VDD18TX1 (pin 62), this pin supplies power to both PHY transmitters. This pin must be connected directly to the VDD18TX2 (pin 65) pin.

3. The VDD18TX1 pin should have one .01 μF (or smaller) capacitor to decouple the LAN9303M. The capacitor size should be SMD_0603 or smaller.

4. **Do Not**, under any circumstances, connect VDD18TX2 to VDD18CORE. Even though they are both +1.8V potentials, they must remain separate, as they are two independent, internal voltage regulators of the LAN9303M.

5. **Do Not**, under any circumstances, use either VDD18TX2 or VDD18CORE to supply other circuits or devices. These two separate, internal voltage regulators are designed to supply internal logic of the LAN9303M only.

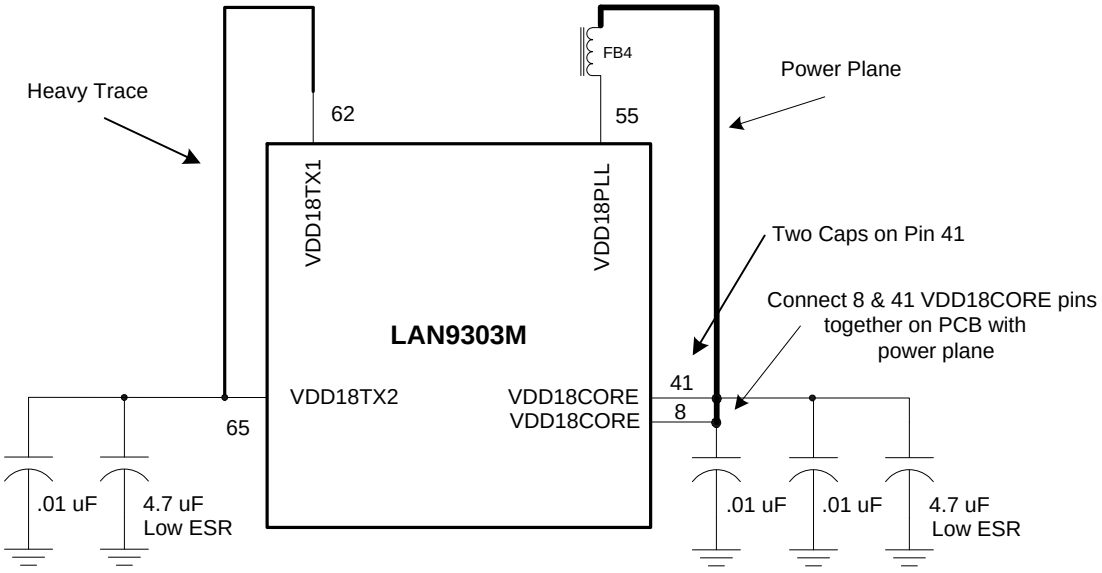


Figure 11 LAN9303M +1.8V Power Connections

Ground Connections:

1. Both the digital ground pins (VSS) and the GND_CORE pins on the LAN9303M QFN are all connected internally to the exposed die paddle ground. The EDP Ground pad on the underside of the LAN9303M must be connected directly to a solid, contiguous digital ground plane.

2. We recommend that the Digital Ground pins and the EDP pin be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9303M QFN. For exact specifications and tolerances refer to the latest revision LAN9303M data sheet.

2. XI (pin 53) on the LAN9303M QFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 54) on the LAN9303M QFN is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

EEPROM Interfaces:

The LAN9303M supports only one type of external EEPROM interface. The Philips I^2C EEPROM format is supported.

I^2C (2-wire) EEPROM Interface:

1. EE_SCL (pin 50) on the LAN9303M QFN connects to the external I^2C EEPROM's serial clock pin.

2. EE_SDA (pin 49) on the LAN9303M QFN connects to the external I^2C EEPROM's Data In/Out pin.

3. Be sure to select a 2-wire style EEPROM that matches the organization and size as determined by the configuration pin.

EXRES Resistor:

1. EXRES (pin 63) on the LAN9303M QFN should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

Required External Pull-ups/Pull-downs:

1. IRQ (pin 52) may require an external pull-up resistor if this output is programmed as an Open Drain type.

2. EE_SDA (pin 49) requires a 10.0K ohm pull-up resistor in order to guarantee proper operation in the I^2C mode. This pull-up is required even if the I^2C bus is not used on the LAN9303M.

3. EE_SCL (pin 50) requires a 10.0K ohm pull-up resistor in order to guarantee proper operation in the I^2C mode. This pull-up is required even if the I^2C bus is not used on the LAN9303M.

4. MDIO (pin 26) requires a 1.5K ohm pull-up resistor to +3.3V in order to guarantee proper operation on the SMI.

5. LED0/GPIO0 (pin 34) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

6. LED1/GPIO1 (pin 33) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

7. LED2/GPIO2 (pin 32) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

8. LED3/GPIO3 (pin 31) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

9. LED4/GPIO4 (pin 30) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

10. LED5/GPIO5 (pin 29) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed as a LED, the pin functionality is fully programmable. Refer to the latest copy of the data sheet for details.

Serial Management Modes:

1. MNGT1_LED4P (pin 30) & MNGT0_LED3P (pin 31), these two pins configure the serial management mode of the LAN9303M. The modes are as follows:

   00 = Reserved
   01 = SMI Managed Mode
   10 = I^2C Managed Mode
   10 = Unmanaged Mode (I^2C Mode with pins 49 & 50 left as no-connects)
   11 = Reserved

   See the latest version of the LAN9303M data sheet for complete details. These pins have weak internal pull-ups and can be driven low with an external 1.0K Ω resistor to digital ground.

Management I^2C Slave Mode:

1. SDA (pin 49), I^2C Slave Serial Data Input/Output pin. This pin is an open-drain output in I^2C mode and connects to an external master. This pin requires an external 10K Ω pull-up resistor.

2. SCL (pin 50), I^2C Slave Serial Clock pin. This pin is an input in I^2C mode and connects to an external master.

Dedicated Configuration Strap Pins:

1. All configuration strap values are latched in on power-on reset or nRST de-assertion. For more detailed information of each bit and functionality, consult the latest version of LAN9303M data sheet.

2. PHYADDR_LED5P (pin 29), functions as a configuration input and is used to establish the default MII Management address values for the three internal PHYs. See the LAN9303M data sheet for further details on PHY addressing. Upon the deassertion of reset, this pin selects the functionality depending upon what state it is in.

   With this pin low, the PHY addressing will start with 00h. This mode can be achieved with a 1.0K Ω pull-down resistor added to this pin.

   0 = Virtual PHY Address = 00
   Port 1 PHY Address = 01
   Port 2 PHY Address = 02

   If this pin is high, the PHY addressing will start with 01h. This mode can be achieved by leaving this pin as a no-connect as this pin has an internal pull-up.

   1 = Virtual PHY Address = 01
   Port 1 PHY Address = 02
   Port 2 PHY Address = 03

   See the latest version of the LAN9303M data sheet for complete details.

3. E2PSIZE_LED2P (pin 32), this strap pin configures the EEPROM size. When latched low, EEPROM sizes 16 x 8-bit through 2048 x 8-bit are supported. When latched high, EEPROM sizes 4096 x 8-bit through 65536 x 8-bit are supported. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Port 1 Configuration Straps:

1. AMDIX1_LED0P (pin 34), this strap pin configures the default for the Auto MDIX soft strap functionality on Port 1. When latched low, Auto MDIX is disabled. When latched high, Auto MDIX is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Port 2 Configuration Straps:

1. AMDIX2_LED1P (pin 33), this strap pin configures the default for the Auto MDIX soft strap functionality on Port 2. When latched low, Auto MDIX is disabled. When latched high, Auto MDIX is enabled. This pin has a weak internal pull-up and can be driven low with an external 1.0K Ω resistor to digital ground.

Miscellaneous:

1. nRST (pin 51), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9303M. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9303M will rely on its internal power-on reset circuitry.

2. TEST1 (pin 47), this pin must be connected to +3.3V.

3. TEST2 (pin 48), this pin must be connected to digital ground.

4. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

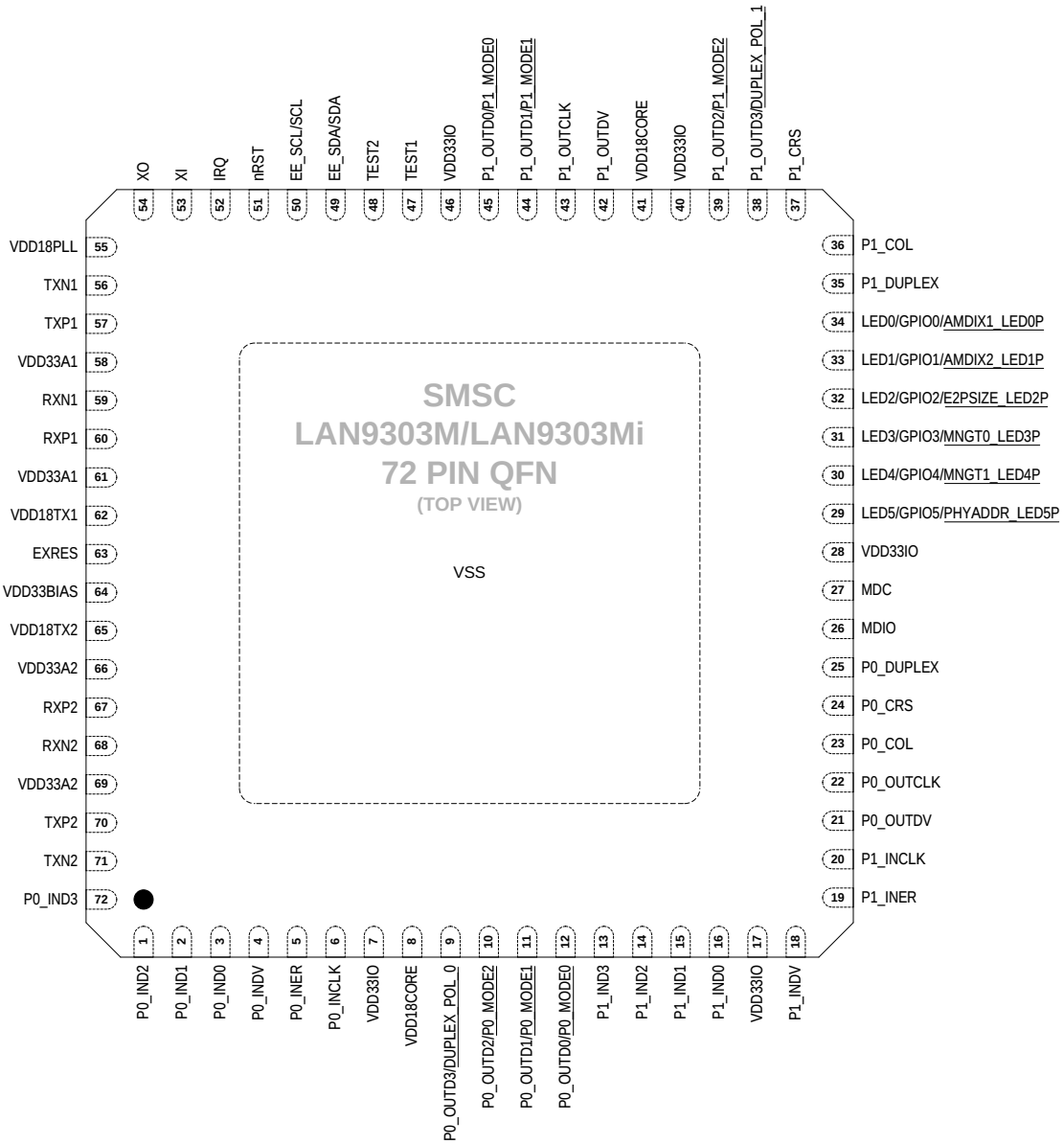
5. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

LAN9303M QFN QuickCheck Pinout Table:

Use the following table to check the LAN9303M QFN shape in your schematic.

LAN89303 QFN			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
1	P0_IND2	37	P1_CRS
2	P0_IND1	38	P1_OUTD3 / DUPLEX_POL_1
3	P0_IND0	39	P1_OUTD2 / P1_MODE2
4	P0_INDV	40	VDD33IO
5	P0_INER	41	VDD18CORE
6	P0_INCLK	42	P1_OUTDV
7	VDD33IO	43	P1_OUTCLK
8	VDD18CORE	44	P1_OUTD1 / P1_MODE1
9	P0_OUTD3 / DUPLEX_POL_0	45	P1_OUTD0 / P1_MODE0
10	P0_OUTD2 / P0_MODE2	46	VDD33IO
11	P0_OUTD1 / P0_MODE1	47	TEST1
12	P0_OUTD0 / P0_MODE0	48	TEST2
13	P1_IND3	49	EE_SDA / SDA
14	P1_IND2	50	EE_SCL / SCL
15	P1_IND1	51	nRST
16	P1_IND0	52	IRQ
17	VDD33IO	53	XI
18	P1_INDV	54	XO
19	P1_INER	55	VDD18PLL
20	P1_INCLK	56	TXN1
21	P0_OUTDV	57	TXP1
22	P0_OUTCLK	58	VDD33A1
23	P0_COL	59	RXN1
24	P0_CRS	60	RXP1
25	P0_DUPLEX	61	VDD33A1
26	MDIO	62	VDD18TX1
27	MDC	63	EXRES
28	VDD33IO	64	VDD33BIAS
29	LED5 / GPIO5 / PHYADDR_LED5P	65	VDD18TX2
30	LED4 / GPIO4 / MNGT1_LED4P	66	VDD33A2
31	LED3 / GPIO3 / MNGT0_LED3P	67	RXP2
32	LED2 / GPIO2 / E2PSIZE_LED2P	68	RXN2
33	LED1 / GPIO1 / AMDIX2_LED1P	69	VDD33A2
34	LED0 / GPIO0 / AMDIX1_LED0P	70	TXP2
35	P1_DUPLEX	71	TXN2
36	P1_COL	72	P0_IND3
73		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

LAN9303M QFN Package Drawing:



NOTE: When HP Auto-MDIX is activated, the TXN/TXP pins can function as RXN/RXP and vice-versa

NOTE: Exposed pad (VSS) on bottom of package must be connected to ground

Reference Material:

1. SMSC LAN9303M Data Sheet; check web site for latest revision.
2. SMSC LAN9303M CEB Schematic, Assembly No. 6471; check web site for latest revision.
3. SMSC LAN9303M CEB PCB, Assembly No. 6471; order PCB from web site.
4. SMSC LAN9303M CEB PCB Bill of Materials, Assembly No. 6471; check web site for latest revision.
5. CEB stands for Customer Evaluation Board.
6. SMSC LAN9303M Reference Design, check web site for latest revision.
7. SMSC Reference Designs are schematics only; there are no associated PCBs.
8. For Qualified / Suggested Magnetics, use these two links to the SMSC LANCheck website:

https://www2.smsc.com/mkt/web_lancheck.nsf/MagList?OpenForm

https://www2.smsc.com/mkt/web_lancheck.nsf/MagCheck?OpenForm