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Microchip LAN9252 Power Management

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INTRODUCTION

The LAN9252 is a 2/3-port EtherCAT® Slave Controller (ESC) with dual integrated Ethernet PHYs. The LAN9252 is typically implemented in Industrial Automation solutions and includes the following main features:

- Integrated high-performance 100Mbps Ethernet transceivers
- 3 FMMUs, 4 SyncManagers, Distributed clock support, 4K bytes of DPRAM
- 8/16-bit host bus interface allowing connection to most 8/16/32-bit embedded controllers
- SPI / SQI slave interface
- Support for 5 different main configurations:
  - Digital I/O (DIGIO)
  - HBI
  - SPI with GPIO
  - SPI with MII - 3 port mode
  - SPI with MII - back to back
- 3rd port for flexible network configurations
- Comprehensive power management features
- Low pin count and small package size

The purpose of this document is to provide details on the various power management modes of the device.

References

- Microchip LAN9252 Datasheet
- Microchip EVB-LAN9252-HBI-SPI-SQI-GPIO Evaluation Board User's Guide
- Microchip PIC32MX7xx Datasheet

Terms and Abbreviations

TABLE 1: TERMS AND ABBREVIATIONS

Term	Definition
DA	Destination Address
ESC	EtherCAT® Slave Controller
EDPD	Energy Detect Power Down
EVB	Engineering Validation Board
HBI	Host Bus Interface
IDE	Integrated Development Environment
SPI	Serial Protocol Interface
SSC	Slave Stack Code

POWER MANAGEMENT

The LAN9252 supports numerous power management and wakeup features. The LAN9252 can be placed in a reduced power mode and programmed to issue an external wake signal via several methods, including “Magic Packet”, “Wake on LAN”, wake on broadcast, wake on perfect DA, and “Link Status Change”. This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command or one of the wake events. The main modes of power management are listed below, and detailed in the following sub-sections:

- Wake-up Event Detection
- Wake-up (PME) Notification
- Block-level Power Management
- Chip-level Power Management

Wake-up Event Detection

Wake-up Event Detection can be categorized into two groups:

- PHY A & B Energy Detect Power Down (EDPD) Mode
- PHY A & B Wake on LAN (WoL)

PHY A & B ENERGY DETECT POWER DOWN (EDPD) MODE

Energy Detect Power Down Mode reduces PHY power consumption. In Energy Detect Power Down Mode, the PHY will resume from power-down when energy is seen on the cable (typically from link pulses). EDPD Mode is entered as follows:

- Enable the Energy detect power down mode by setting bit 13 of the PHY x Mode Control/Status Register (17 in decimal)
- Enable the Energy detect interrupt by setting INT7_MASK (bit 7) of the PHY x Interrupt Mask Register (30 in decimal)
- When the energy is received via link pulses or packets, ENERGYON (bit 1) of the PHY x Mode Control/Status Register (17 in decimal) goes high
- The transceiver automatically resets itself to the state prior to power down and asserts INT7 (bit 7) of the PHY x Interrupt Source Flags Register (29 in decimal)

When in EDPD mode, the device's NLP characteristics may be modified (for green switch interoperability). The device can be configured to transmit NLPs as follows:

- Set EDPD TX NLP ENABLE (bit 15) of the PHY x EDPD NLP Configuration Register (16 in decimal)
- Configure the TX NLP time interval via the EDPD TX NLP INTERVAL TIMER SELECT field (bits 14:13) of the PHY x EDPD NLP Configuration Register (16 in decimal)
- Set the EDPD RX Single NLP Wake Enable (bit 12) of the PHY x EDPD NLP Configuration Register (16 in decimal)
- If the EDPD RX Single NLP Wake Enable bit is cleared, the maximum interval for detecting reception of two NLPs is made via the EDPD RX NLP Max Interval Detect Select field (bits 11:10) of the PHY x EDPD NLP Configuration Register (16 in decimal)

PHY A & B WAKE ON LAN (WOL)

PHY A and B provide the following types of WoL event detection:

- Perfect DA (Destination Address) Detection
- Broadcast Detection
- Magic Packet Detection
- Wakeup Frame Detection

Perfect DA (Destination Address) Detection

When enabled, the Perfect DA detection mode allows the detection of a frame with the destination address matching the address stored in the PHY x MAC Receive Address x Registers. To configure Perfect DA Detection:

- Set the desired MAC address to cause the wake event in the PHY x MAC Receive Address A Register (PHY_RX-_ADDRA_x), PHY x MAC Receive Address B Register (PHY_RX_ADDRB_x), and PHY x MAC Receive Address C Register (PHY_RX_ADDRC_x)
- Set the Perfect DA Wakeup Enable (PFDA_EN) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) to enable Perfect DA detection
- Set bit 8 (WoL event indicator) in the PHY x Interrupt Mask Register (PHY_INTERRUPT_MASK_x) to enable WoL events
- When a match is triggered, bit 8 of the PHY x Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x) will be set, and the Perfect DA Frame Received (PFDA_FR) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) will be set.

Broadcast Detection

When enabled, the Broadcast detection mode allows the detection of a frame with the destination address value of FF FF FF FF FF FF. The frame must also pass the FCS and packet length check. To configure Broadcast Detection:

- Set the Broadcast Wakeup Enable (BCST_EN) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) to enable Broadcast detection
- Set bit 8 (WoL event indicator) in the PHY x Interrupt Mask Register (PHY_INTERRUPT_MASK_x) to enable WoL events
- When a match is triggered, bit 8 of the PHY x Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x) will be set, and the Broadcast Frame Received (BCAST_FR) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) will be set

Magic Packet Detection

When enabled, the Magic Packet detection mode allows the detection of a Magic Packet frame. A Magic Packet is a frame addressed to the device - either a unicast to the programmed address, or a broadcast - which contains the pattern 48'h FF_FF_FF_FF_FF_FF after the destination and source address field, followed by 16 repetitions of the desired MAC Address (loaded into the PHY x MAC Receive Address A Register (PHY_RX_ADDRA_x), PHY x MAC Receive B Register (PHY_RX_ADDRB_x), and PHY x MAC Receive Address C Register (PHY_RX_ADDRC_x)) without any breaks or interruptions. To configure Magic Packet Detection:

- Set the desired MAC address to cause the wake event in the PHY x MAC Receive Address A Register (PHY_RX-_ADDRA_x), PHY x MAC Receive Address B Register (PHY_RX_ADDRB_x), and PHY x MAC Receive Address C Register (PHY_RX_ADDRC_x)
- Set the Magic Packet Enable (MPEN) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) to enable Magic Packet detection
- Set bit 8 (WoL event indicator) in the PHY x Interrupt Mask Register (PHY_INTERRUPT_MASK_x) to enable WoL events
- When a match is triggered, bit 8 of the PHY x Interrupt Source Flags Register (PHY_INTERRUPT_SOURCE_x) will be set, and the Magic Packet Received (MPR) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) will be set

Wakeup Frame Detection

When enabled, the Wakeup Frame detection mode allows the detection of a pre-programmed Wakeup Frame. Wakeup Frame detection provides a way for system designers to detect a customized pattern within a packet via a programmable wake-up frame filter. The filter has a 128-bit byte mask that indicates which bytes of the frame should be compared by the detection logic. A CRC-16 is calculated over these bytes. The result is then compared with the filter's respective CRC-16 to determine if a match exists. When a wake-up pattern is received, the Remote Wakeup Frame Received (WUFR) bit of the PHY x Wakeup Control and Status Register (PHY_WUCSR_x) is set.

If enabled, the filter can also include a comparison between the frame's destination address and the address specified in the PHY x MAC Receive Address A Register (PHY_RX_ADDRA_x), PHY x MAC Receive Address B Register (PHY_RX_ADDRB_x), and PHY x MAC Receive Address C Register (PHY_RX_ADDRC_x). The specified address can be a unicast or a multicast. If address matching is enabled, only the programmed unicast or multicast address will be

considered a match. Non-specific multicast addresses and the broadcast address can be separately enabled. The address matching results are logically OR'd (i.e., specific address match result OR any multicast result OR broadcast result).

Wake-up (PME) Notification

The PME module handles the latching of the following bits in the Power Management Control Register (PMT_CTRL):

- PHY B Energy-Detect / WoL Status Port B (ED_WOL_STS_B) bit
- PHY A Energy-Detect / WoL Status Port A (ED_WOL_STS_A) bit

This module also masks the status bits ED_WOL_STS_B and ED_WOL_STS_A with the corresponding enable bits and combines the results together to generate the Power Management Interrupt. The Power Management Interrupt, combined with interrupts sources, drives the IRQ output pin.

Block-level Power Management

The device supports software controlled clock disabling of the following modules in order to reduce power consumption:

- Disabling EtherCAT Core
- PHY Power Down
- LED Pins Power Down

DISABLING ETHERCAT CORE

- The Entire EtherCAT core can be disabled by setting the ECAT_DIS (21) bit in the Power Management Control Register (0x084)
- As a safety precaution, it must be written as a 1 two consecutive times

PHY POWER DOWN

General Power Down

In this mode the entire transceiver, except the PHY management control interface is powered down. General power down mode is enabled by setting Power Down (PHY_PWR_DWN) bit of the PHY x Basic Control Register.

Energy Detect Power Down Mode

A PHY can be placed into Energy Detect Power Down Mode as described in the PHY A & B Energy Detect Power Down (EDPD) Mode section.

LED PINS POWER DOWN

All LED outputs may be disabled by setting the LED_DIS bit in the Power Management Control Register (PM_CTRL). When disabled, open-drain / open-source LEDs are undriven. Push-pull LEDs are still driven, but are set to their inactive state.

Chip-level Power Management

The device supports power-down modes to allow applications to minimize power consumption. Power is reduced by disabling the clocks as outlined in Table 2.

TABLE 2: POWER MANAGEMENT STATES

Clock Source	D0	D1	D2	D3
25 MHz Crystal Oscillator	ON	ON	ON	OFF
PLL	ON	ON	OFF (Note 2)	OFF
System Clocks (100 MHz, 50 MHz, 25 MHz and others)	ON	OFF	OFF	OFF
Network Clocks	Available (Note 1)	Available (Note 1)	Available (Note 1)	OFF (Note 3)

Note 1: If supplied by the PHYs or externally

2: PLL is requested to be turned off and will disable if both of the PHYs are in either Energy Detect or General Power Down

3: PHY clocks are off, external clocks are gated off

The power management state are defined as follows:

- D0: Normal Mode - In this mode all functionality is available.
- D1: System clocks disabled, XTAL, PLL and network clocks enabled.
- D2: System clocks disabled, PLL disable requested, XTAL enabled.
- D3: System clocks disabled, PLL disabled, XTAL disabled

ENTERING LOW POWER MODES

- Write the PM_MODE and PM_WAKE fields in the Power Management Control Register (PMT_CTRL) to the desired values
- Set the wake-up detection desired per the Wake-up Event Detection section
- Set the appropriate wake-up notification per the Wake-up (PME) Notification section
- Ensure the device is in a state where it can safely be placed into a low power mode (all packets transmitted, receivers disabled, packets processed/ flushed, etc.)
- Set PM_SLEEP_EN bit in the Power Management Control Register (PMT_CTRL)

EXITING LOW POWER MODES

- An automatic wake-up will occur based on the events described in the Wake-up Event Detection section
- Automatic wake-up is enabled with the PM_WAKE bit in the Power Management Control Register (PMT_CTRL)
- A manual wake-up is initiated by the host when:
  - An HBI write to the Byte Order Test Register occurs
  - An SPI/SQI read of the Byte Order Test Register occurs
- To determine the when the host is functional; the Byte Order Test Register should be polled until the correct pattern is read
- The device ready bit will go high once the device is returned to power savings state D0 and the PLL is re-stabilized

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001911A (03-27-15)	Document Release	

Note the following details of the code protection feature on Microchip devices:

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