

Pre-Configured Clock Generator Part Numbers for Switchtec and Data Center Applications

INTRODUCTION

This application note lists a variety of popular clocking component options for data center and storage applications. The focus is on the ZL3026x family of devices, but, for completeness, a few devices with fewer output clocks are also included.

The ZL3026x is a flexible family of synthesizer and frequency translators with multiple clock outputs. The devices are fully configurable and can be used in many applications. However, in some applications, it is preferable to have a pre-configured device that starts up in the desired mode. This application note provides a list of part numbers for factory pre-configured ZL3026x devices suitable for use in Switchtec applications. These pre-configured devices will initialize to known states and do not need to be controlled over the SPI or I²C interfaces. The part numbers all have the ZL3026x base number, followed by a 4-digit alphanumeric suffix. For details on the base device, please see <https://www.microchip.com/wwwproducts/en/ZL30265>.

PRE-CONFIGURED PART NUMBERS

The functions and part numbers are shown in the table below.

TABLE 1: PRE-CONFIGURED PART NUMBERS

Function	Part Number
One output 100 MHz LVDS MEMS 2 mm x 2.5 mm Oscillator	DSC1223DI1-100M0000
One output 100 MHz LVDS Oscillator	MX555ABB100M000
Two output 100 MHz LVDS	SM806030UMG
Two output 100 MHz HCSL	ZL30265LDG1Q05V
Two output 100 MHz HCSL with 0.3% downspread SSC	ZL30265LDG1Q05W
Two output 100 MHz HCSL with 0.5% downspread SSC	ZL30265LDG1Q05X
Four output 100 MHz LVDS with integrated crystal	MX875BB0020
Four output 100 MHz HCSL	ZL30265LDG1Q05Y
Four output 100 MHz HCSL with 0.3% downspread SSC	ZL30265LDG1Q05Z
Four output 100 MHz HCSL with 0.5% downspread SSC	ZL30265LDG1Q060
Six output 100 MHz LVDS with integrated crystal	MX875BB0021
Six output 100 MHz HCSL	ZL30265LDG1Q061
Six output 100 MHz HCSL with 0.3% downspread SSC	ZL30265LDG1Q062
Six output 100 MHz HCSL with 0.5% downspread SSC	ZL30265LDG1Q063
Four output 100 MHz LVDS	ZL30265LDG1Q066
Multi Output Config used on PM5461-Kit	ZL30265LDG1Q01G
Multi Output Config used on PM5461-Kit	ZL30267LDG1Q031
Multi Output Config used on PM5461-Kit	ZL30263LDG1Q01F
PM40000 Series PCIe Gen 4 Reference Design	ZL30265LDG1Q033
PCIe Gen 5 Retimer Designs	ZL30265LDG1Q03V
PM8502 PCIe Gen 4 SAS Controller Ref Designs	ZL30265LDG1Q03V
PM8502 PCIe Gen 4 SAS Controller Ref Designs	ZL30267LDG1Q03W
PM8596 OpenCAPI to DDR	ZL30267LDG1Q04V
PM50000 Series PCIe Gen 5 Switch Reference Design	ZL30265LDG1Q05N

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If your required start-up configuration is not in this list, please contact your Microchip Timing ESE to assist with generating a custom configured device for your application.

The figures in the following sections depict the pre-configured part numbers graphically.

Note that the Enable pins are implemented on GPIO[0:3].

Microchip recommends the VXM7-1362-50M000000 crystal for these applications.

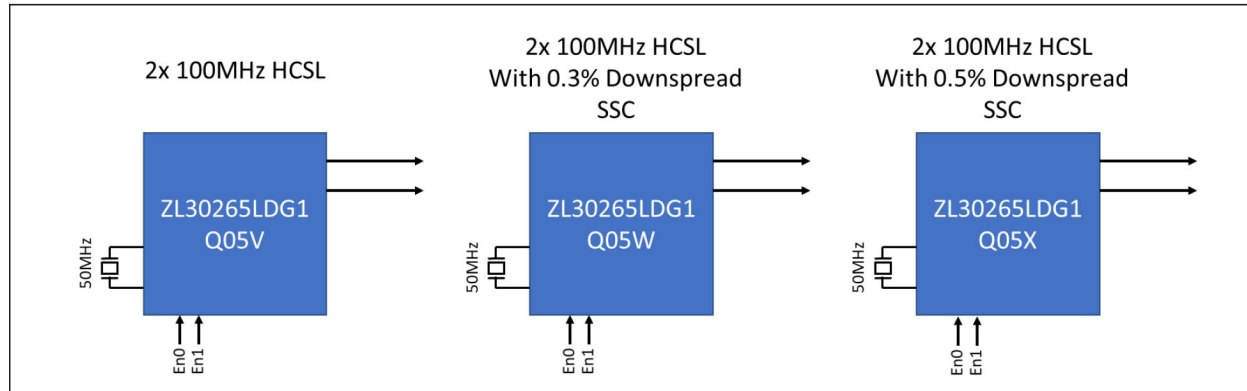


FIGURE 1: Pre-Configured Part Numbers with Two 100 MHz HCSL Outputs.

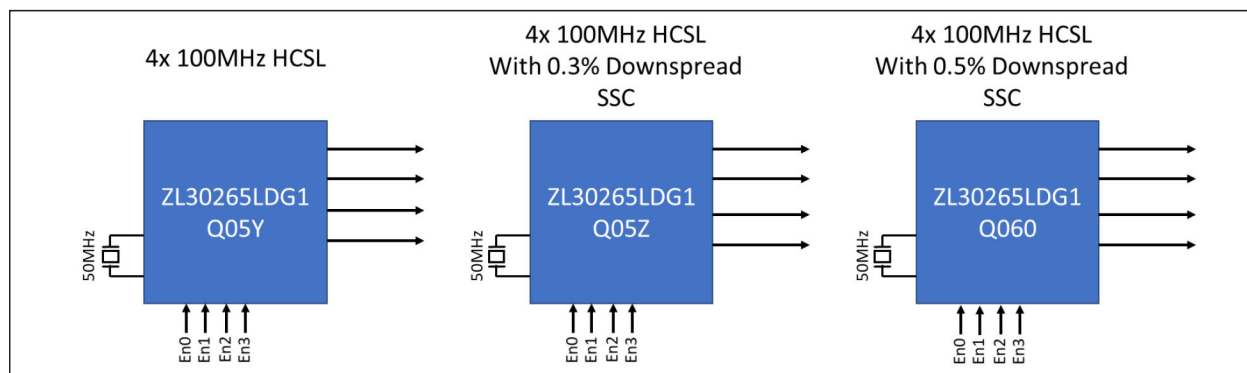


FIGURE 2: Pre-Configured Part Numbers with Four 100 MHz HCSL Outputs.

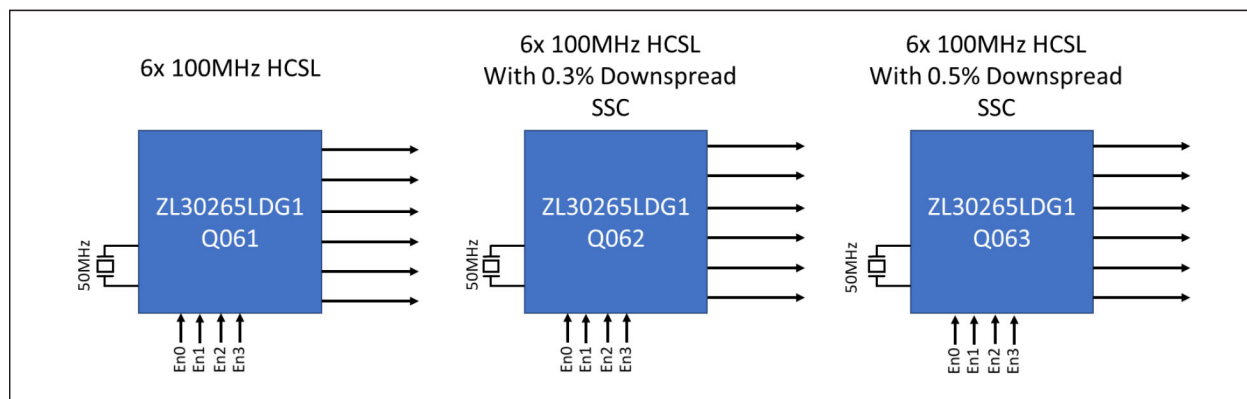


FIGURE 3: Pre-Configured Part Numbers with Six 100 MHz HCSL Outputs.

Note that on six-output devices, only the first four outputs are controlled by the Enable signals because there are only four GPIOs. The other two outputs are always enabled.

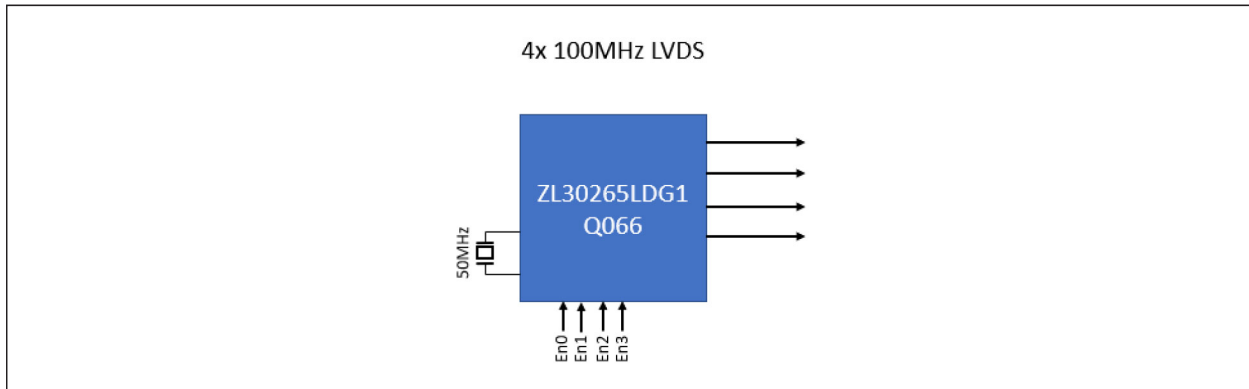


FIGURE 4: Pre-Configured Part Numbers with Four 100 MHz LVDS Outputs.

DEVICE CONFIGURATIONS FOR DEVICES USED IN PM5641-KIT FOR PCIe GEN 3 SWITCHES

The devices shown in this section are used in the PM5641 Evaluation Kit (PSX/PFX 96/80/64xG3 PCIe Switch HD Board). The following block diagrams illustrate the primary function of each of the configuration options. Configurations are selected by driving the config pins AC2/AC1/AC0 at reset. For example, setting AC2/AC1/AC0 to 101 and driving RSTN from low to high will result in Config 101 being selected.

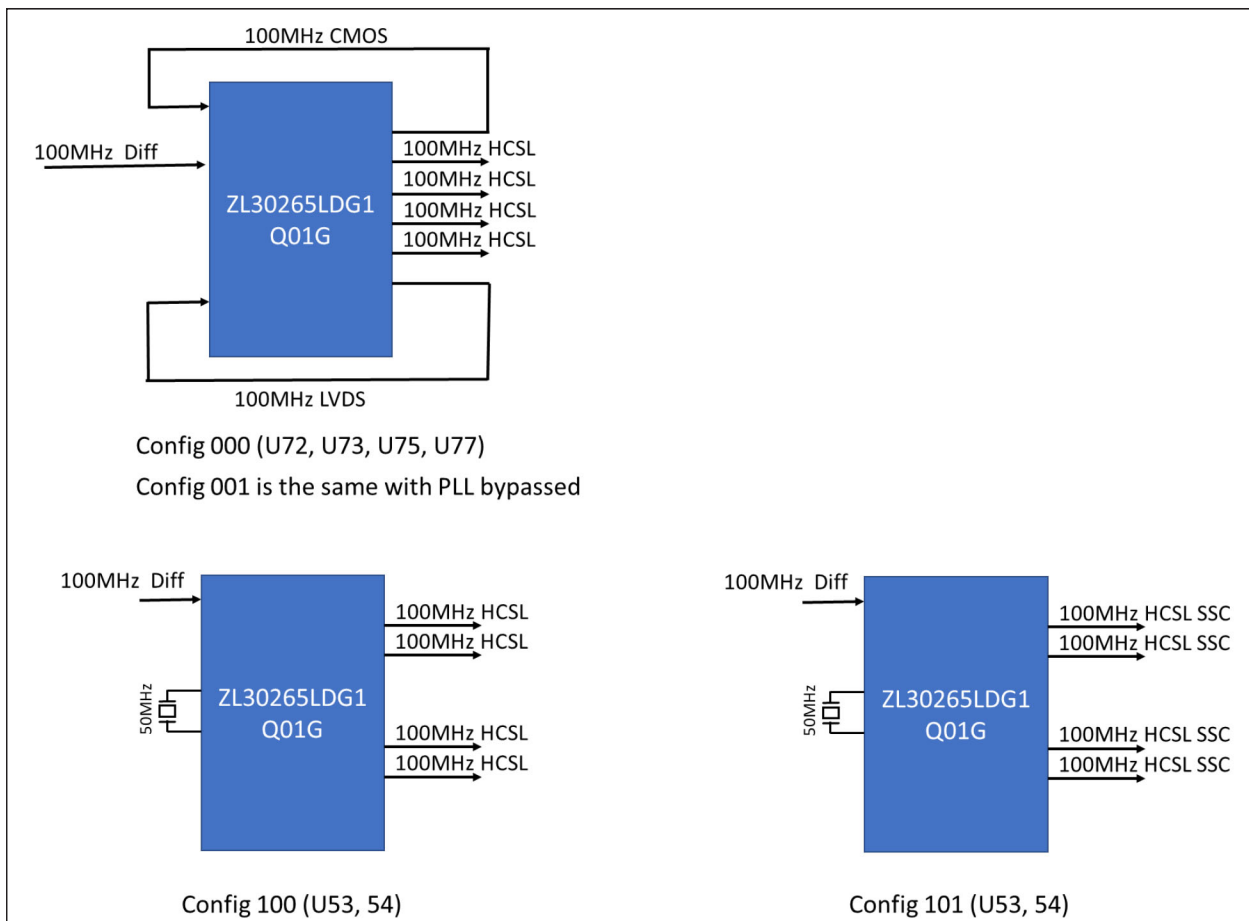


FIGURE 5: ZL30265LDG1Q01G.

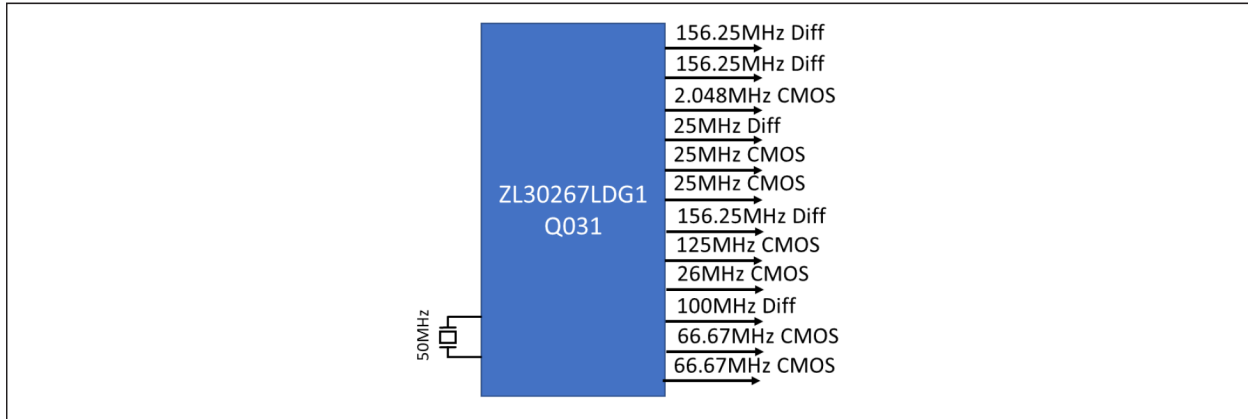


FIGURE 6: ZL30267LDG1Q031.

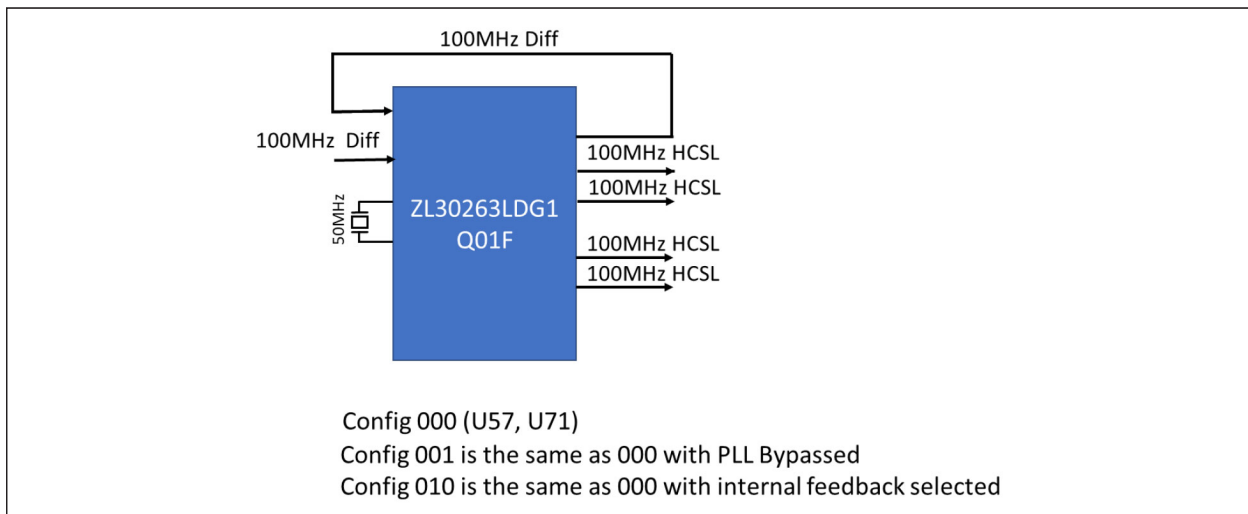


FIGURE 7: ZL30263LDG1Q01F.

DEVICE CONFIGURATIONS FOR DEVICES USED IN PM40000 SERIES PCIe GEN 4 REFERENCE DESIGN

The ZL30265LDG1Q033 is used in the PM40000 Series of references designs. The following block diagrams illustrate the primary function of each of the configuration options. Configurations are selected by driving the config pins AC2/AC1/AC0 at reset. For example, setting AC2/AC1/AC0 to 101 and driving RSTN from low to high will result in Config 101 being selected.

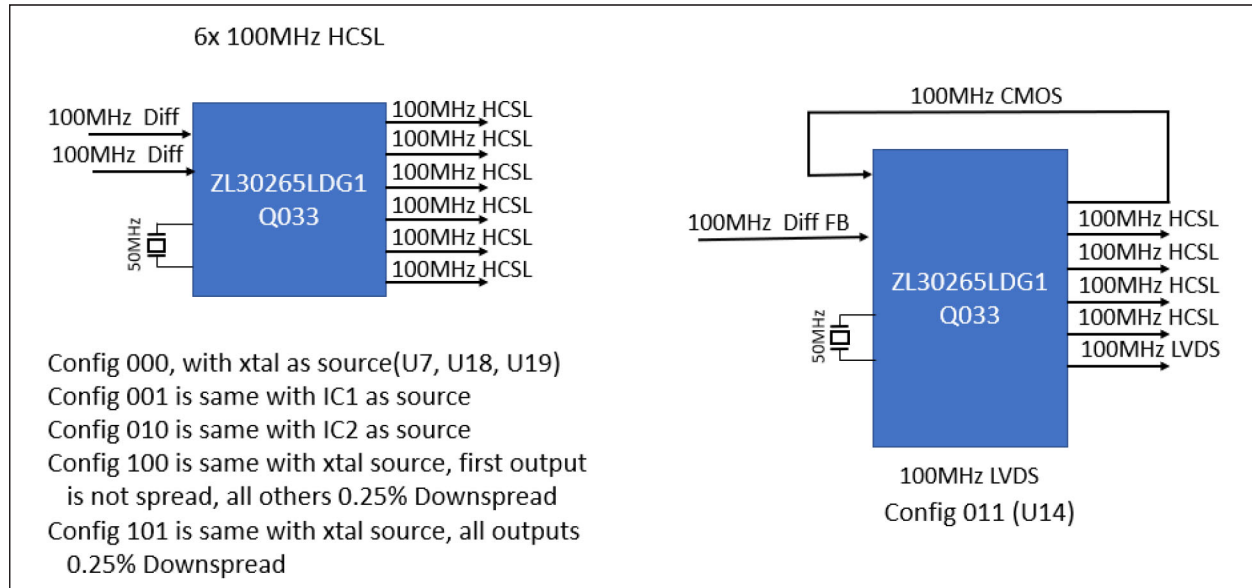


FIGURE 8: ZL30265LDG1Q033.

DEVICE CONFIGURATIONS FOR PCIe GEN 4 SAS CONTROLLER DESIGNS

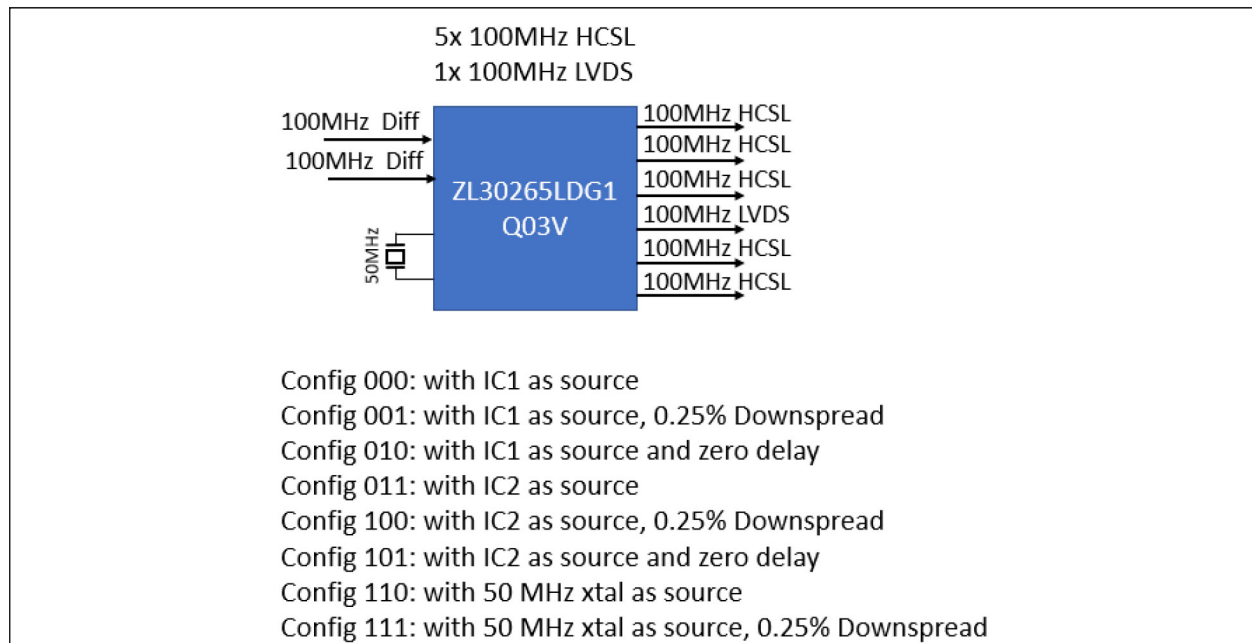


FIGURE 9: ZL30265LDG1Q03V.

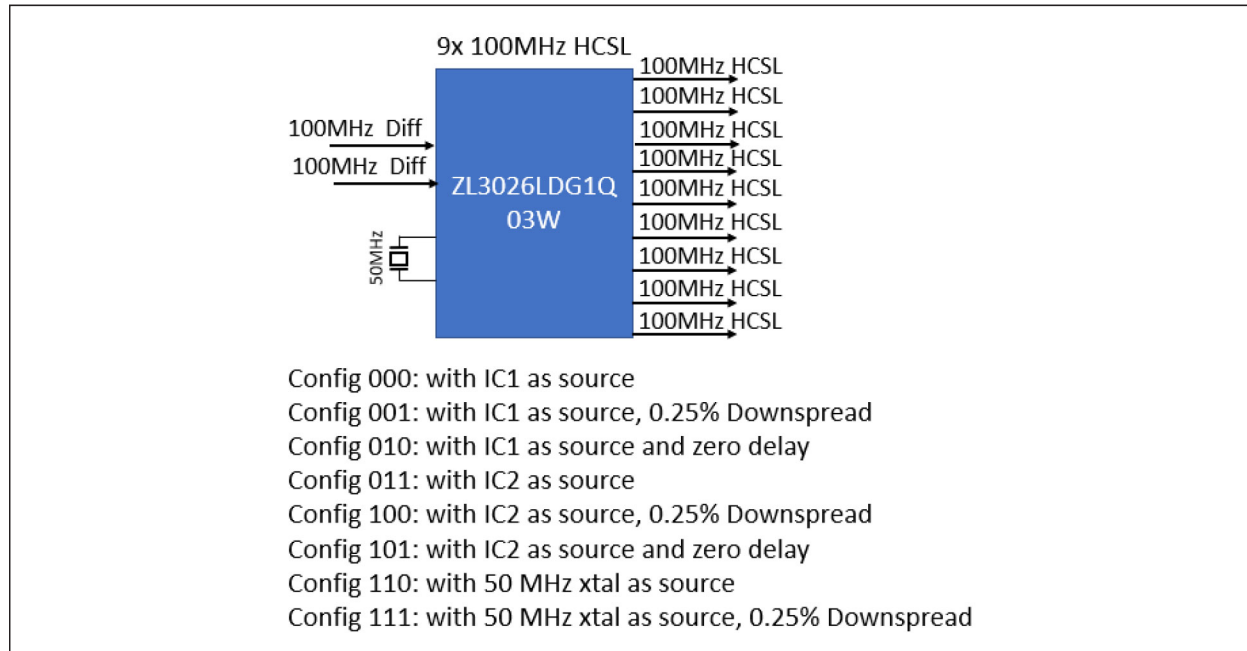


FIGURE 10: ZL3026LDG1Q03W.

DEVICE CONFIGURATIONS FOR PCIe GEN 5 RETIMER DESIGNS

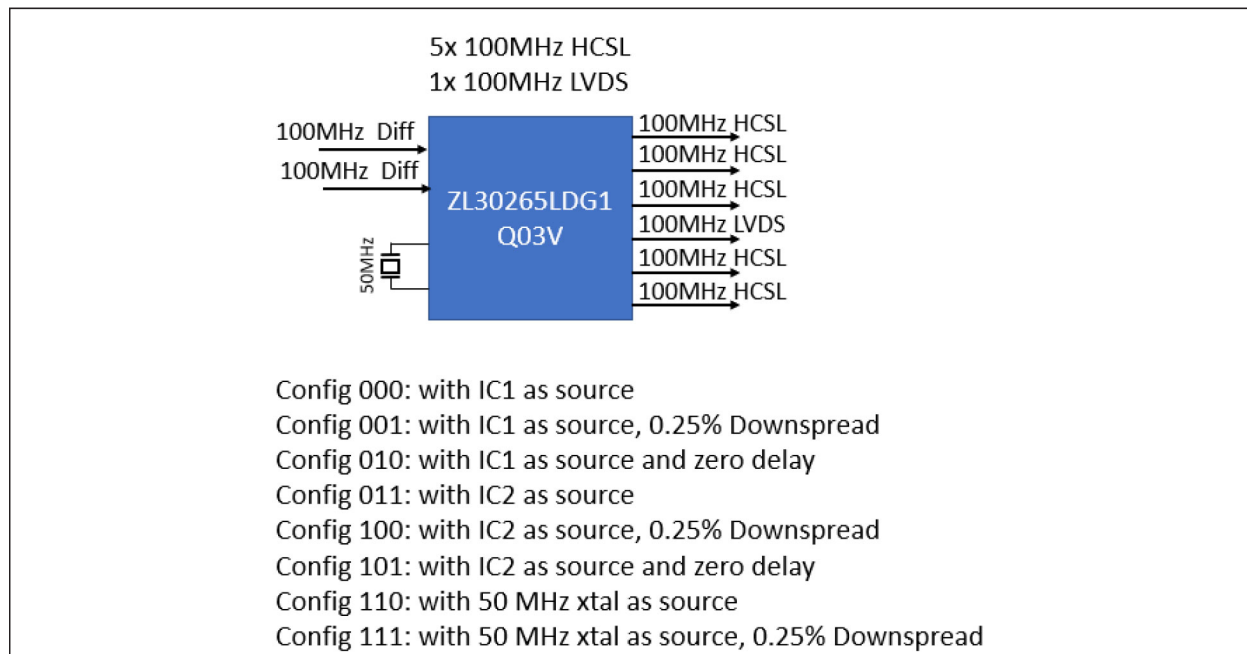


FIGURE 11: ZL30265LDG1Q03V.

DEVICE CONFIGURATIONS FOR DDR OpenCAPI DESIGNS

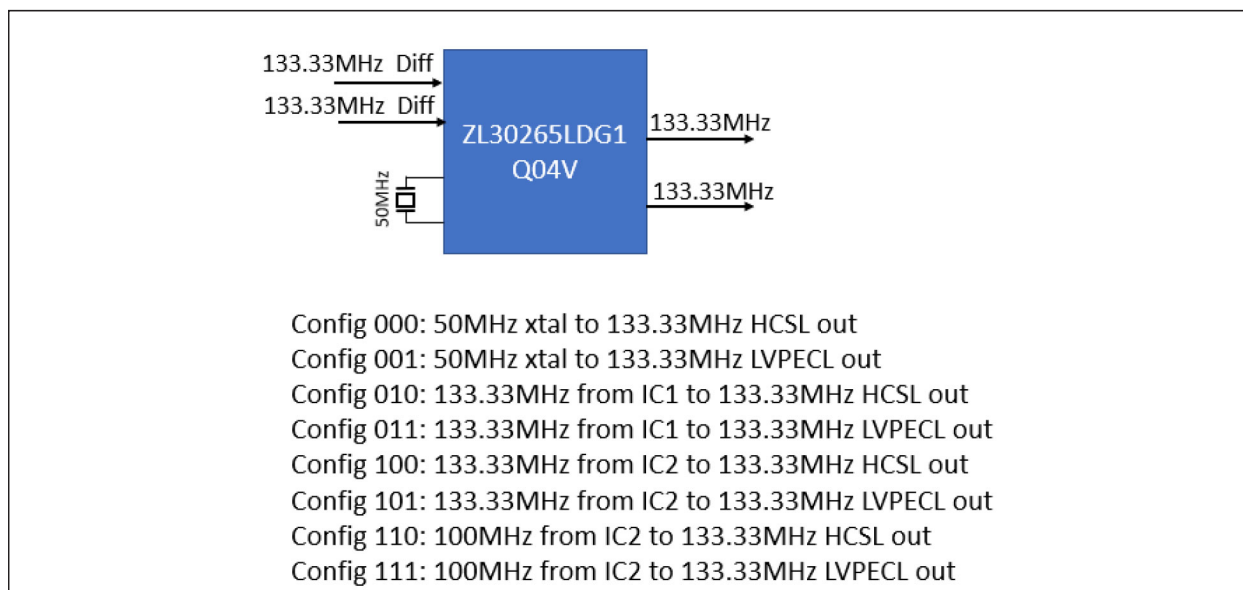


FIGURE 12: ZL30267LDG1Q04V.

DEVICE CONFIGURATIONS FOR DEVICES USED IN PM50000 SERIES PCIe GEN 5 SWITCH REFERENCE DESIGN

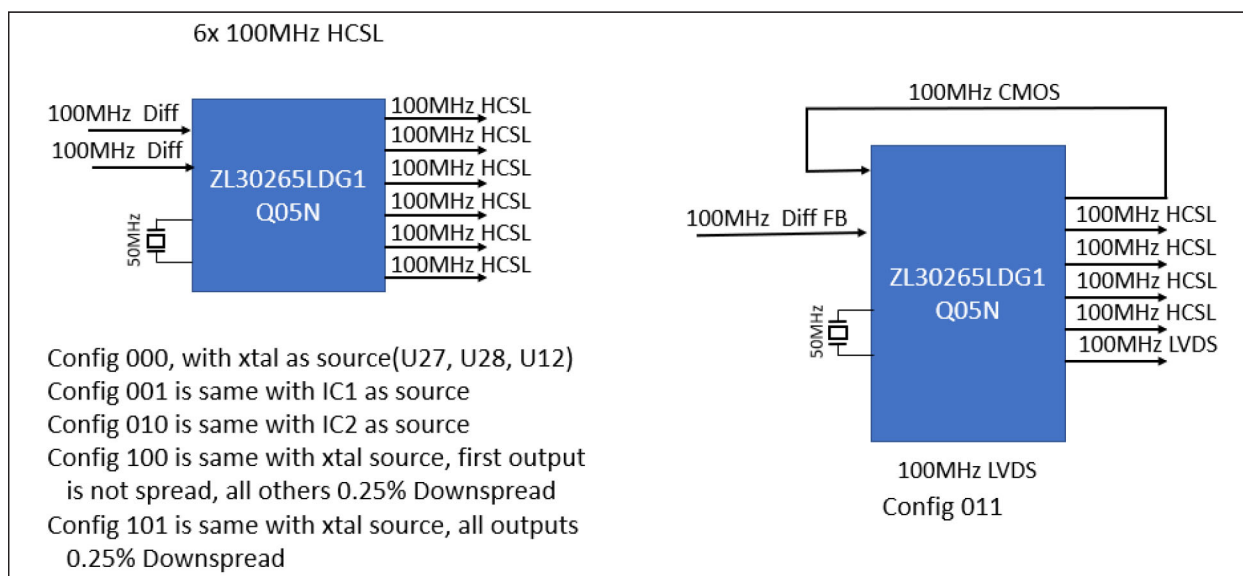


FIGURE 13: ZL30265LDG1Q05N.

TERMINATIONS AND BIASING

Examples of interface and biasing circuits that can be used to connect timing devices to the Switchtec devices can be found in [Application Note ZLAN-703: Interfacing Timing Devices to Switchtec Devices](#).

CONCLUSION

The application note lists a set of pre-configured ZL3026x part numbers that are suitable for PCIe applications and, in particular, for data center applications and applications using the Switchtec family of devices.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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