

KSZ8051 to KSZ8081/KSZ8091 (32-QFN) -- Hardware Differences

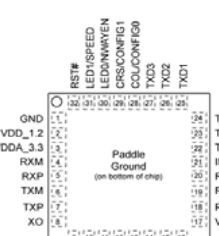
Hardware Pin Differences: Tabulated are only pin differences between parts (pins common to all parts are not shown)
Internal pull-up/pull-down values for the strapping pins are indicated after table

Rev 1.0 Created

KSZ8051MNL (0.13um)				KSZ8081MNX (0.11um)				KSZ8091MNX (0.11um)				KSZ8051RNL (0.13um)				KSZ8081RNB (0.11um)				KSZ8091RNB (0.11um)			
Pin #	Name	Type	Function	Name	Type	Function		Name	Type	Function		Name	Type	Function		Name	Type	Function		Name	Type	Function	
21	INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset.	INTRP / NAND_Tree#	Ipu/Opu	Sames as KSZ8091MNL (0.13um)		INTRP / PME_N2 / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output PME_N Output: Programmable PME_N Output (pin option 2) This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset.		INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset.		INTRP / PME_N2 / NAND_Tree#	Ipu/Opu	Sames as KSZ8091RNL (0.13um)		INTRP / PME_N2 / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output PME_N Output: Programmable PME_N Output (pin option 2) This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND_Tree# at the de-assertion of reset.	
22	TXC	IO	MI Mode: MI Transmit Clock Output MI Back-to-Back Mode: MI Transmit Clock Input	TXC	IO	Sames as KSZ8091MNL (0.13um)		TXC / PME_EN	Ipu/O	MI Mode: MI Transmit Clock Output MI Back-to-Back Mode: MI Transmit Clock Input Config Mode: The pull-up/pull-down value is latched as PME_EN at the de-assertion of reset.		NC	O	No connect. It is recommended to tie this unused pin directly to ground.		NC	O	Sames as KSZ8091RNL (0.13um)		PME_EN	Ipd/O	Config Mode: The pull-up/pull-down value is latched as PME_EN at the de-assertion of reset.	
30	LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset.	LED0 / NWAYEN	Ipu/O	Sames as KSZ8091MNL (0.13um)		LED0 / PME_N1 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / PME_N Output: Programmable PME_N Output (pin option 1) In this mode, this pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset.		LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset.		LED0 / PME_N1 / NWAYEN	Ipu/O	Sames as KSZ8091RNL (0.13um)		LED0 / PME_N1 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / PME_N Output: Programmable PME_N Output (pin option 1) In this mode, this pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset.	
31	LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset.	LED1 / SPEED	Ipu/O	Sames as KSZ8091MNL (0.13um)		TXER	Ipd	MI Mode: MI Transmit Error Input		LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset.		LED1 / SPEED	Ipu/O	Sames as KSZ8091RNL (0.13um)		LED1 / SPEED	Ipu/O	Sames as KSZ8091RNL (0.13um) and KSZ8081RNB (0.11um)	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
KSZ8051RNL: All Pull-Up / Pull-Down Pins (including Strapping Pins)						
BU	Internal Pull-up Resistance	V _{DD} =3.3V	30	45	75	kΩ
		V _{DD} =2.5V	37	59	102	kΩ
		V _{DD} =1.8V	57	100	187	kΩ
pD	Internal Pull-down Resistance	V _{DD} =3.3V	27	43	76	kΩ
		V _{DD} =2.5V	35	60	110	kΩ
		V _{DD} =1.8V	55	100	190	kΩ

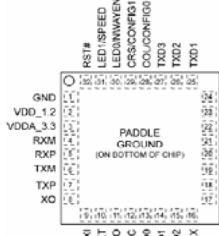
Pin Configuration – KSZ8051MNL



32-Pin (5mm x 5mm) QFN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
KSZ8081MNX: All Pull-Up/Pull-Down Pins (including Strapping Pins)						
BU	Internal Pull-Up Resistance	V _{DD} =3.3V	30	45	75	kΩ
		V _{DD} =2.5V	39	61	102	kΩ
		V _{DD} =1.8V	48	99	178	kΩ
pD	Internal Pull-Down Resistance	V _{DD} =3.3V	26	43	79	kΩ
		V _{DD} =2.5V	34	59	113	kΩ
		V _{DD} =1.8V	53	99	200	kΩ

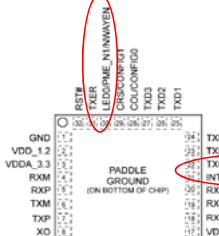
Pin Configuration– KSZ8081MNX



32-Pin (5mm x 5mm) QFN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
KSZ8091MNX: All Pull-Up/Pull-Down Pins (including Strapping Pins)						
BU	Internal Pull-Up Resistance	V _{DD} =3.3V	30	45	75	kΩ
		V _{DD} =2.5V	39	61	102	kΩ
		V _{DD} =1.8V	48	99	178	kΩ
pD	Internal Pull-Down Resistance	V _{DD} =3.3V	26	43	79	kΩ
		V _{DD} =2.5V	34	59	113	kΩ
		V _{DD} =1.8V	53	99	200	kΩ

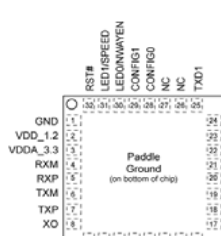
Pin Configuration – KSZ8091MNX



32-Pin (5mm x 5mm) QFN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
KSZ8051RNL: All Pull-Up / Pull-Down Pins (including Strapping Pins)						
BU	Internal Pull-Up Resistance	V _{DD} =3.3V	30	45	75	kΩ
		V _{DD} =2.5V	37	59	102	kΩ
		V _{DD} =1.8V	57	100	187	kΩ
pD	Internal Pull-down Resistance	V _{DD} =3.3V	27	43	76	kΩ
		V _{DD} =2.5V	35	60	110	kΩ
		V _{DD} =1.8V	55	100	190	kΩ

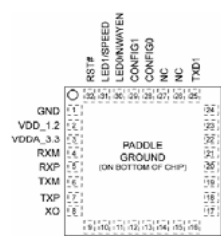
Pin Configuration – KSZ8051RNL



32-Pin (5mm x 5mm) QFN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
KSZ8081RNB: All Pull-Up/Pull-Down Pins (including Strapping Pins)						
BU	Internal Pull-Up Resistance	V _{DD} =3.3V	30	45	75	kΩ
		V _{DD} =2.5V	39	61	102	kΩ
		V _{DD} =1.8V	48	99	178	kΩ
pD	Internal Pull-Down Resistance	V _{DD} =3.3V	26	43	79	kΩ
		V _{DD} =2.5V	34	59	113	kΩ
		V _{DD} =1.8V	53	99	200	kΩ

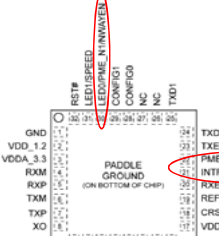
Pin Configuration – KSZ8081RNB



32-Pin (5mm x 5mm) QFN

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
KSZ8091RNB: All Pull-Up/Pull-Down Pins (including Strapping Pins)						
BU	Internal Pull-Up Resistance	V _{DD} =3.3V	30	45	75	kΩ
		V _{DD} =2.5V	39	61	102	kΩ
		V _{DD} =1.8V	48	99	178	kΩ
pD	Internal Pull-Down Resistance	V _{DD} =3.3V	26	43	79	kΩ
		V _{DD} =2.5V	34	59	113	kΩ
		V _{DD} =1.8V	53	99	200	kΩ

Pin Configuration – KSZ8091RNB



32-Pin (5mm x 5mm) QFN

KSZ8051 to KSZ8081/KSZ8091 (32-QFN) -- Software Differences

Software Register Differences Tabulated are only register/bit differences between parts (registers/bits common to all parts are not shown)

* Register Access

KSZ8051MNL/IRNL: have Direct PHY registers only

KSZ8081MNX/IRNB: have Direct PHY registers only

KSZ8091MNX/IRNB: have Direct PHY registers and Indirect MMD PHY registers (primarily for Energy Efficient Ethernet and Wake-on-LAN functions)

Rev 1.0 Created

Address		KSZ8051MNL (0.13um)		KSZ8081MNX (0.11um)		KSZ8091MNX (0.11um)		KSZ8051IRNL (0.13um)		KSZ8081IRNB (0.11um)		KSZ8091IRNB (0.11um)	
Register (hex)	Bit	Name	Function	Name	Function	Name	Function	Name	Function	Name	Function	Name	Function
3h	[9:4]	Model Number	Six bit manufacturer's model number, 01_0101	Model Number	Six bit manufacturer's model number, 01_0110	Model Number	Six bit manufacturer's model number, 01_0110	Model Number	Six bit manufacturer's model number, 01_0101	Model Number	Six bit manufacturer's model number, 01_0110	Model Number	Six bit manufacturer's model number, 01_0110
3h	[3:0]	Revision Number	Four bit manufacturer's revision number (depends on silicon revision)	Revision Number	Four bit manufacturer's revision number (depends on silicon revision)	Revision Number	Four bit manufacturer's revision number (depends on silicon revision)	Revision Number	Four bit manufacturer's revision number (depends on silicon revision)	Revision Number	Four bit manufacturer's revision number (depends on silicon revision)	Revision Number	Four bit manufacturer's revision number (depends on silicon revision)
Dh	[15:0]					Function DEVAD	MMD Access Control <indirect register access - primarily for EEE & WoL>					Function DEVAD	MMD Access Control <indirect register access - primarily for EEE & WoL>
Eh	[15:0]					MMD Register Address / Data	MMD Access Register Address / Data <indirect register access - primarily for EEE & WoL>					MMD Register Address / Data	MMD Access Register Address / Data <indirect register access - primarily for EEE & WoL>
10h	[15:0]			Reserved PULL off	Digital Reserved Control (see Name)	Reserved PULL off	Digital Reserved Control (see Name)			Reserved PULL off	Digital Reserved Control (see Name)	Reserved PULL off	Digital Reserved Control (see Name)