

Power Supply Rejection Ratio of Low Dropout Voltage Regulators

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INTRODUCTION

This application note introduces the Power Supply Rejection Ratio (PSRR) and illustrates how to measure and correctly evaluate the PSRR of a low dropout voltage regulator.

PSRR AND OUTPUT NOISE

The Power Supply Rejection Ratio is the ability of a device, such as a Low Dropout Voltage regulator, to reject the various perturbations that can be found in its input supply rail by providing a greatly attenuated signal at the output. Generally, the main source of the perturbation will be the output ripple of the DC/DC converters that typically power LDOs.

High PSRR LDOs are recommended for powering line ripple sensitive devices such as: RF applications, ADCs/DACs, FPGAs, MPUs, and audio applications.

One important clarification must be made: PSRR is **NOT** the same with output noise. PSRR is a measure of rejection. It shows what the part will output based on the given input.

Output NOISE is typically referred to in a data sheet as e_N . This is the sum of all the noise sources developed internally by the part and some of the external noise sources. Internal noise sources are flicker or $1/f$ noise, burst noise, shot noise and thermal noise. External noise can either be electromagnetically induced noise or generated by mechanical stress that causes the piezoelectric effect.

Figure 1 displays a side-by-side comparison of the two distinct specifications. The Output Noise, plotted as a graph of spectral noise density, indicates how much “noise” or output ripple is internally generated by the part itself over a given frequency range, while being powered from an ideal DC power supply or battery. To ensure that the noise measurement obtained is accurate, it should be carried out in a shielded environment, that in turn blocks most of the external noise sources from interfering with the measurement. The PSRR graph in **Figure 1** indicates the amount of attenuation the LDO provides at different frequencies.

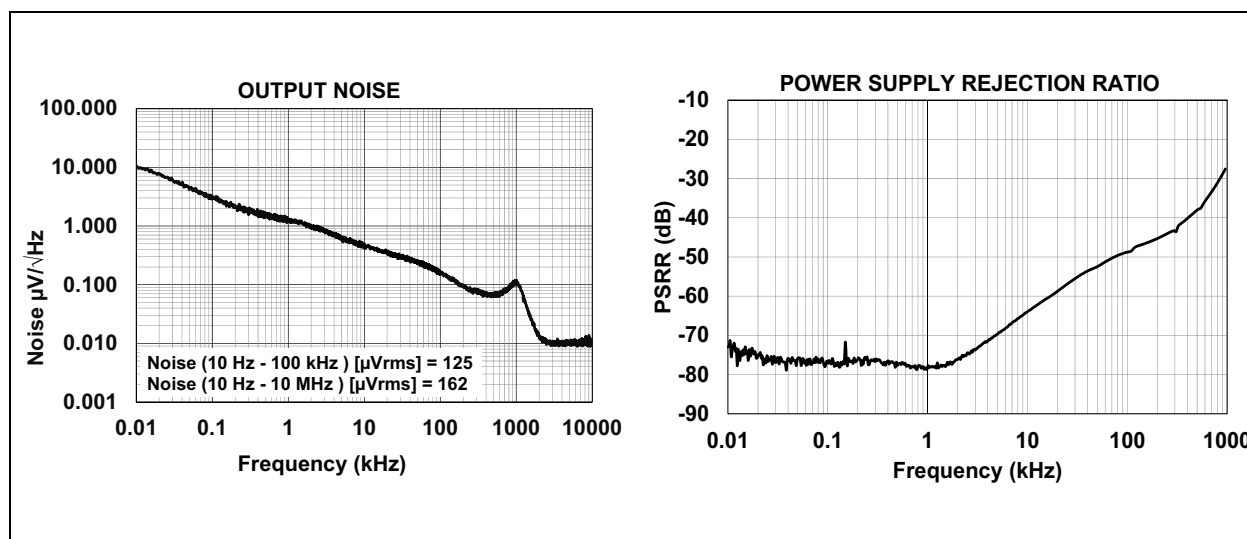


FIGURE 1: Output Noise and PSRR Graphics.

PSRR SHORT INTRODUCTION

There are two common ways to mathematically express the PSRR value. The first is based on the definition itself, which measures rejection:

EQUATION 1: PSRR AS A MEASURE OF REJECTION RATIO

$$PSRR = 20 \times \log \frac{V_{IN}}{V_{OUT}}$$

The second method expresses the value as a measure of gain:

EQUATION 2: PSRR AS A MEASURE OF GAIN RATIO

$$PSRR = 20 \times \log \frac{V_{OUT}}{V_{IN}}$$

This can be used in order to better explain PSRR.

It should be noted that V_{OUT} and V_{IN} from Equation 1 and Equation 2 are AC values.

Figure 2 shows the functional blocks of the LDO.

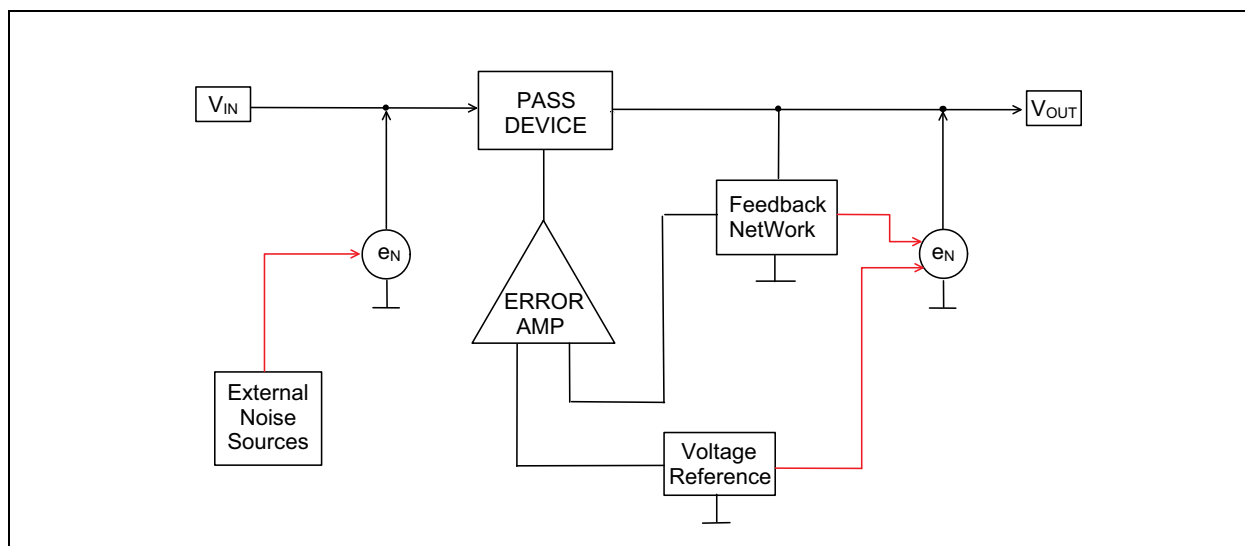


FIGURE 2: LDO Block Diagram.

One of the elements which determine the PSRR of an LDO is the AC gain of the error amplifier.

It can be considered that the PSRR curve follows the gain curve as shown in **Figure 3**, until the closed loop gain reaches the crossover frequency.

The AC and DC gain of the error amplifier is similar until the error amplifier reaches the rolloff frequency. This is why the PSRR degradation usually occurs at higher frequencies. When the gain reaches the crossover frequency, the operational amplifier can no longer control the loop and, as a result, no longer has an impact on the PSRR value.

Although the PSRR is largely controlled by the operational amplifier, it is also determined by other elements which impact the curve at its extremities. The voltage reference has an impact from 0 Hz to around a couple of tens of Hz. In this range, the PSRR is mostly controlled by the band gap reference as well as the control loop. For frequencies that are higher than the crossover frequency, the PSRR is influenced by the output capacitor (as long as the crossover frequency is lower than the resonance frequency of the capacitor)

and by the parasitic elements that can be found from the input to the output of the LDO in the final assembled package.

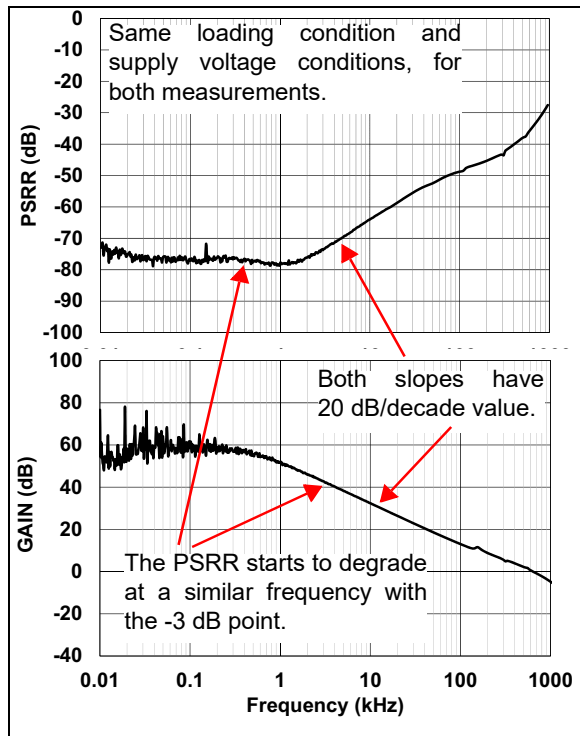


FIGURE 3: PSRR vs. GAIN (MIC47050 Example).

The PSRR value of an LDO generally degrades as a function of output current, meaning that the worst value of the PSRR can be seen for maximum output current.

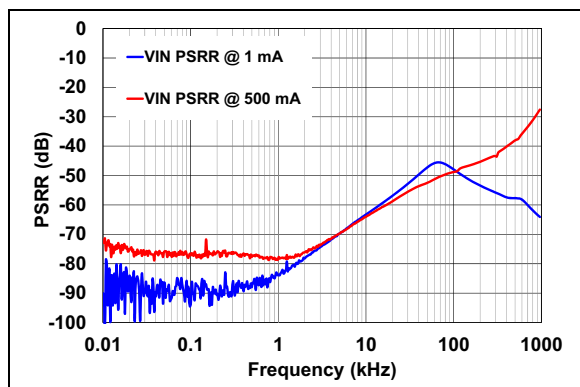


FIGURE 4: PSRR vs. Output Current (MIC47050 Example).

Another factor that impacts the PSRR is the value of the output capacitor. Even if in some cases the PSRR value can be improved by using a higher capacitance, this value is not considerable, given that most LDOs have been optimized to work with the typical recommendations of the output capacitor.

PSRR MEASUREMENT

PSRR can be measured at a specific frequency or a determined frequency range. The typical range is 10 Hz to 1 MHz. It can, however, be extended to 10 MHz for parts that have a superior PSRR, such as the Ripple Blocker™ product line. Adequate hardware is needed to supply the LDO under test, which makes it necessary to over-impose a sinusoidal signal with the DC offset required to power the part.

The supply voltage used for powering the LDO during the PSRR test must meet the following conditions:

EQUATION 3: SUPPLY VOLTAGE

$$V_{IN} = DC_{COMPONENT} + AC_{COMPONENT}$$

EQUATION 4: SUPPLY VOLTAGE TYPICAL VALUE

$$V_{IN} = \left(V_R + V_{HEADROOM} + \frac{V_{PKPK}}{2} \right) + V_{PKPK}$$

EQUATION 5: SUPPLY VOLTAGE FOR MINIMUM SUPPLY VOLTAGE CONSTRAINT

$$V_{IN} = \left(V_{IN(MIN)} + \frac{V_{PKPK}}{2} \right) + V_{PKPK}$$

V_R is the output voltage of the LDO.

$V_{HEADROOM}$ is typically 1V for some LDOs or for linear voltage regulators this value can be higher than 1V so it needs to be adjusted accordingly). $V_{HEADROOM}$ is composed from the value given by the dropout voltage of the pass transistor and an additional saturation voltage that is needed to prevent the pass transistor from entering triode region of operation. When the pass transistor goes from saturation region of operation to triode, this transition will cause the loop gain to drop which in turn will cause the PSRR to degrade.

$V_{IN(MIN)}$ is the minimum input voltage required by an LDO. When $V_R + V_{HEADROOM}$ is lower than the $V_{IN(MIN)}$, the constraint for the input voltage is then calculated using [Equation 5](#).

For example: if there is an LDO with the minimum input voltage of 2.5V and a $V_R = 1V$, then using [Equation 4](#) is not sufficient to meet the minimum input supply condition and, as a result, the part might not even start.

V_{PKPK} is the AC signal amplitude and generally has a value of 0.5V. The value can be adjusted to accommodate the required value as long as the operating conditions are met.

When powering the part, the LDO must be prevented from entering the dropout region of operation. Consequently, the proper operating conditions, as noted in the respective product's data sheet, must be assured.

For example: the LDO has a dropout of 1V, the amplitude of the sinusoidal signal used is 500 mV_{PKPK} and V_R is set to 5V with a value for the DC offset of 6V.

The supply needs to be 250 mV higher to prevent the part from entering in dropout when the negative swing of the sine occurs.

Alongside the aforementioned factors that impact the PSRR of the part, not having the correct input supply voltage degrades the PSRR as well. For this reason, it must be ensured that the LDO never operates in dropout.

To generate the V_{IN} supply, special hardware is used. The block diagram is illustrated in [Figure 5](#).

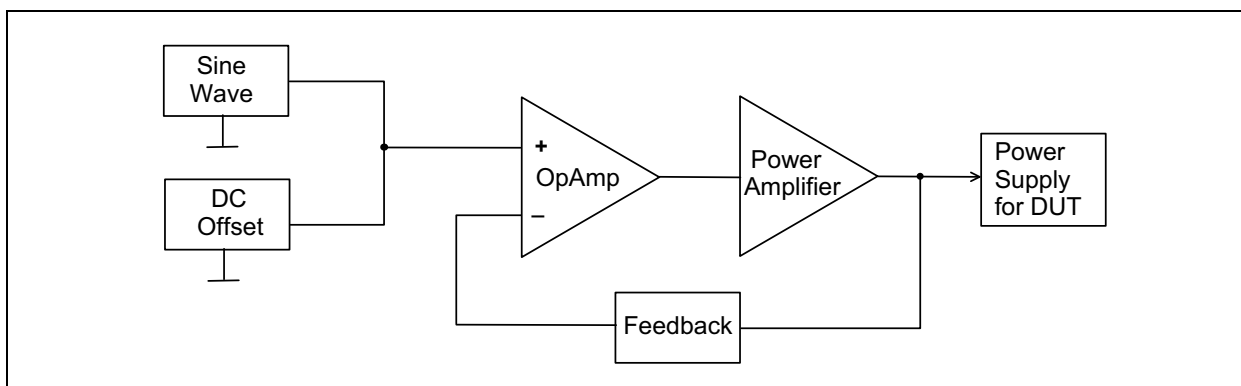


FIGURE 5: PSRR Supply Board.

The general structure of the supply system required to carry out the PSRR test is displayed in [Figure 5](#). The board adds the sine wave signal to the DC Offset, with a secondary power stage amplifier being required to ensure that adequate power is delivered to the DUT (Device Under Test). A control loop is required to have the required input voltage powering the DUT.

Before starting the measurement, the input capacitor should be removed from the DUT. This measure applies to most LDOs and voltage regulators and is required to prevent the distortion and/or attenuation of the sinusoidal signal used to drive the board. This also allows the PSRR measurement to be performed strictly with respect to the rejection ability of the LDO.

For the aforementioned power supply board, the source of the sinusoidal signal determines how the PSRR is being measured. Depending on the source used, the PSRR can be measured in two ways:

- using a signal generator and an oscilloscope
- using a network analyzer

The first method utilizes a signal generator and an oscilloscope. The method will enable the analysis of the PSRR for a single frequency point. However, this method is not accurate for high PSRR values. This is limited by the dynamic range of the oscilloscope, which is not as high as the range of the network analyzer. (note that there are high-end solutions for oscilloscopes, which have the capability to perform the PSRR in a similar way to a network analyzer).

For information on how to set up and probe the DUT in order to have greater measurement accuracy, see [Appendix A: "Setup probing and connections"](#).

The PSRR measurement is then performed by setting the signal generator to output a constant frequency signal with the required amplitude and using the oscilloscope to measure the difference between the input and output signals.

The second method involves the use of a network analyzer. The network analyzer is configured to perform the measurement required and the calculations in [Equation 2](#). This is done by selecting the corresponding channels and making the appropriate connections to the input and output of the DUT (the configuration and/or the labeling is done separately for each device, so the user has to identify and make the connection required for their setup). [Figure 6](#) illustrates a typical setup for the PSRR measurement.

By using the network analyzer, there is no need for an additional signal generator, given that the device outputs a sine wave in the specific bandwidth (10 Hz to 10 MHz) required to connect to the PSRR supply board.

While configuring the network analyzer care must be taken in choosing Intermediate Filter (IF) bandwidth required for the measurement. If the measurement is done at the typical starting frequency of 10 Hz, the value of the IF filter must be lower than 10 Hz to accurately measure the PSRR up to hundreds of Hertz.

If the first measurement displays too many artifacts, then it is advised to use an averaged measurement to obtain a much cleaner graph.

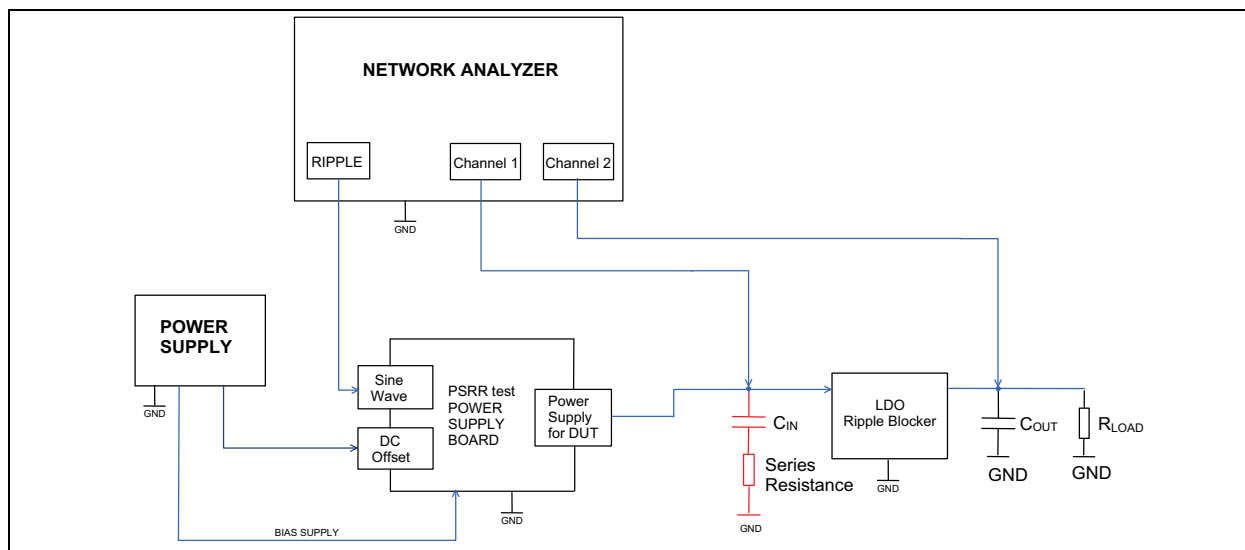


FIGURE 6: PSRR Measurement Setup.

PSRR MEASUREMENT FOR RIPPLE BLOCKERS

The Ripple Blocker family of linear regulators provides excellent PSRR. However, the measurement of the PSRR may pose problems. This is due to the architecture having stability problems when an input capacitor is not used during transitory events. As a result, the PSRR measurement needs to be performed by using an input capacitor with additional series resistance of around $5\ \Omega$. This not only applies to Ripple Blockers, but other LDOs that have stability problems when an input capacitor is not present.

Adding the additional series resistance to the capacitor reduces the distortion and attenuation that occurs at high frequencies. The attenuation itself is caused by the capacitor shorting all high-frequency signals to ground.

Figure 7 and **Figure 9** illustrate orders of magnitude and the differences between two types of LDO, a low I_Q LDO and a high PSRR LDO. The figures do not imply that the values used apply as presented for all the parts that are assigned to the two categories (note that this is a worst case scenario; it is the system designer duty to decide if the results are affecting the application and/or the system requirements needed).

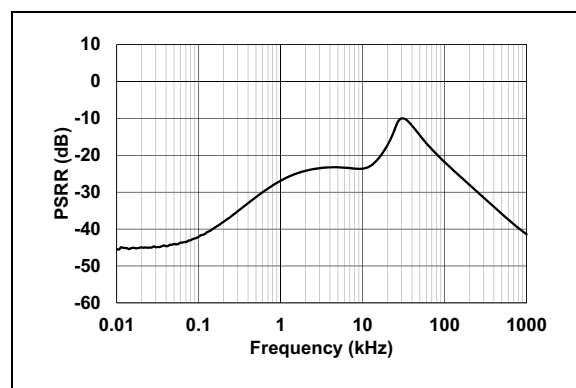


FIGURE 7: PSRR of Low I_Q LDO.

Figure 7 shows a typical PSRR curve for a very low I_Q part. This part is not intended to filter the extremely noisy input supplies and is to be directly powered from batteries.

The following case will be considered: for a generic low I_Q part which at 100kHz provides only 10 dB of attenuation, meaning that if a $1\ V_{PKPK}$ sinusoidal signal is applied to its input then around $300\ mV_{PKPK}$ of sinusoidal oscillations still persist. For more details, see **Figure 8**.

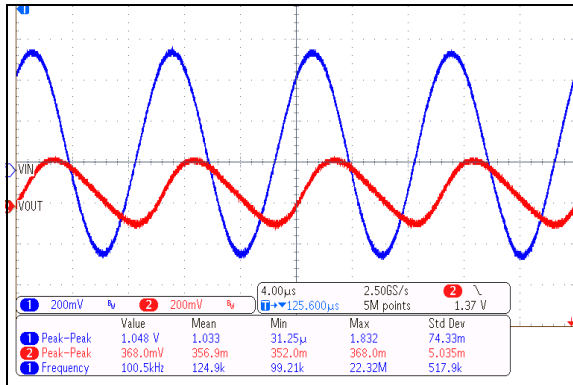


FIGURE 8: Inadequate LDO PSRR for the Application.

The same scenario can be analyzed with the low I_Q LDO replaced with a Ripple Blocker or another LDO with superior PSRR. For this scenario, see the curve in [Figure 9](#).

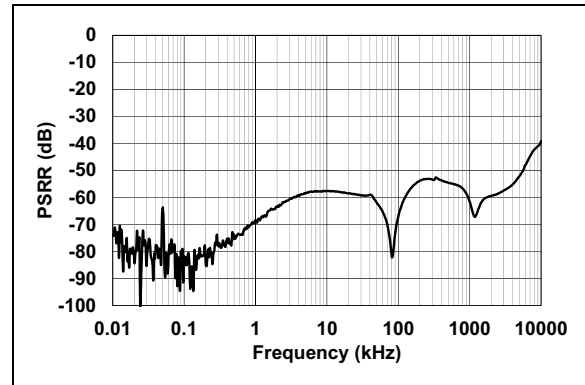


FIGURE 9: PSRR for Ripple Blockers or LDOs with Superior PSRR.

For this example, the PSRR generated at 100 kHz is better than the -60 dB. As a result, for a 1 V_{PKPK} sinusoidal signal on its input, the output will only have around 1 mV $_{PKPK}$ sinusoidal oscillations on the output.

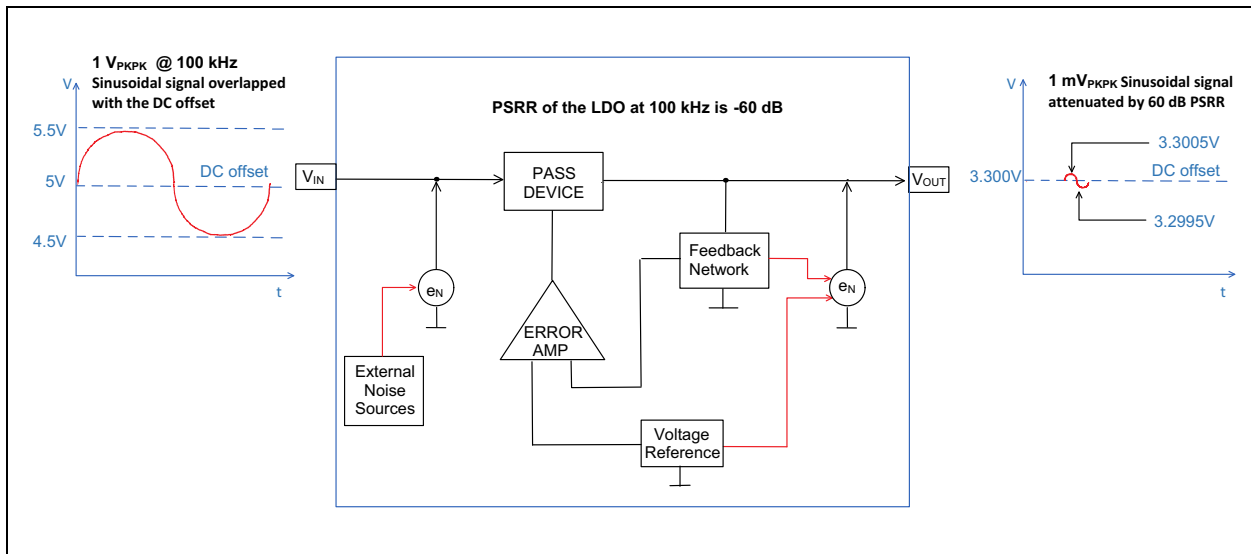


FIGURE 10: PSRR Attenuation Visual Aid.

CONCLUSIONS

PSRR needs to be considered when looking at an LDO and when doing a large power delivery architecture for systems, especially if the application is sensitive to line ripple. Taking into account the variation of the PSRR at different operating points will enable the desired functionality in the final system.

APPENDIX A: SETUP PROBING AND CONNECTIONS

When probing high-frequency signals or signals which can easily be corrupted by ambient noise, certain methods of good practice must be employed.

If an oscilloscope probe is used to measure the output and input signals from the DUT, the length of the ground connection between the oscilloscope probe and the chosen test point must be as short as possible.

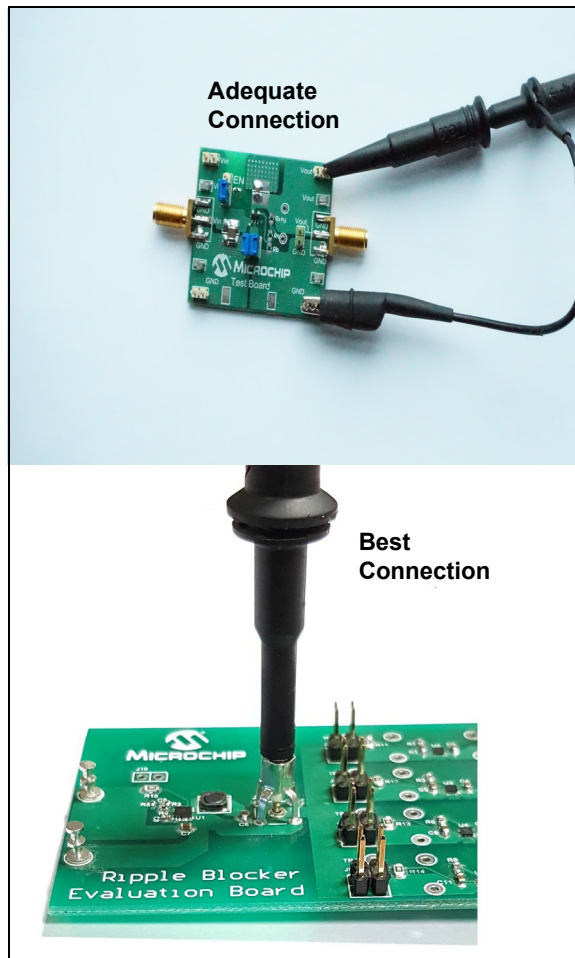


FIGURE 11: Oscilloscope Probe Connection.

The impact of this change is displayed in [Figure 12](#).

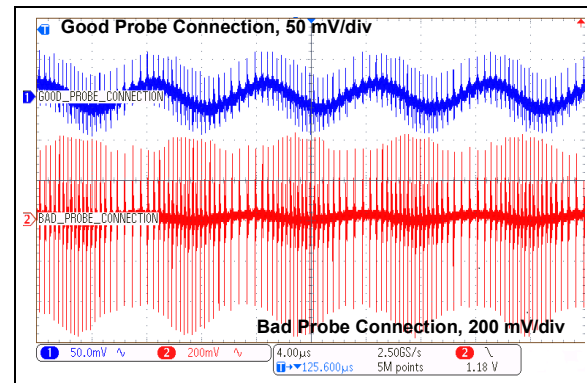


FIGURE 12: Signal Integrity for the Connections with Both Channels at 300 MHz Bandwidth and Probing the Same Signal.

The connection between the PSRR supply board and the DUT should be as short as possible, made by using shielded cables. The cables used should not be longer than needed to avoid unnecessary losses. If coaxial cables and SMA type connectors are used, it is the user's duty to ensure that the power level that is driven through the cables and connectors does not exceed their ratings.

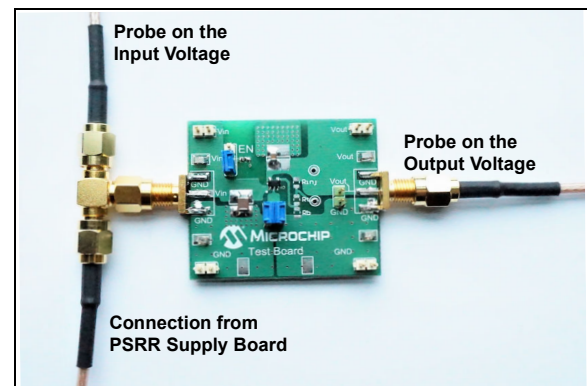


FIGURE 13: Shielded Cable Connection.

If this type of setup is not available, a coaxial cable with a very short ground lead, using a 2.54 mm pin header and socket, is sufficient. See [Figure 14](#) for more details. For both setups, a limited number of connections can be made before the quality of the contact starts degrading and can cause unwanted interferences with the measurements.

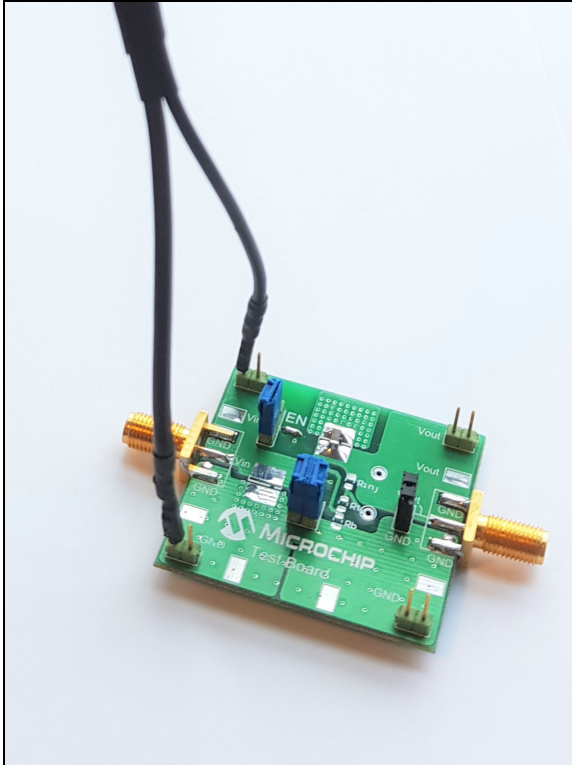


FIGURE 14: *Shielded Cable Connection 2.*

Another efficient way to allow for probing an existing design is the use of U.FL connectors and ferrite beads or 0 Ω resistors between the input supply of the DUT and the existing PDN (Power Delivery Network). This allows the decoupling of the DUT from the PDN.

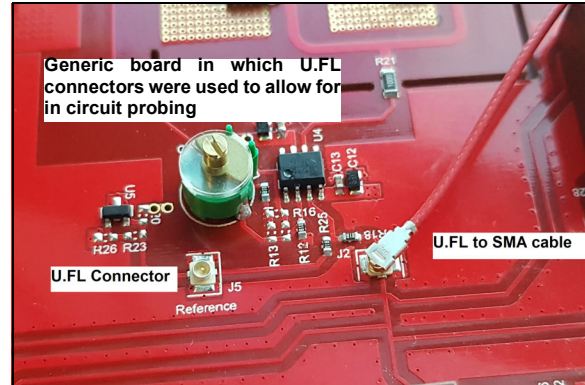


FIGURE 15: *Circuit Probing for Final Circuit.*

Additionally, when choosing a load type, it is best to use a resistive load instead of an electronic load. Doing so prevents other external sources from interfering with the system under test.

REVISION HISTORY

Revision A (June 2019)

Original release of this document.

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