AN3311

SAM9X60 Hardware Design Considerations

Scope

This document is intended to facilitate the bring-up of any hardware design featuring a SAM9X60 MPU by providing a short checklist intended for the hardware designer.

Abbreviation List

- SDRAM – Synchronous Dynamic Random-Access Memory
- SDR – Single Data Rate
- DDR – Double Data Rate
- LP – Low Power
- PCB – Printed Circuit Board

References

Type	Name	Literature No.	Available
Data sheet	SAM9X60	DS60001579	https://www.microchip.com/wwwproducts/en/SAM9X60
Errata	SAM9X60 Device Silicon Errata and Data Sheet Clarification	DS80000846	https://www.microchip.com/wwwproducts/en/SAM9X60
Board design files	SAM9X60-EK board design files	–	https://www.microchip.com/DevelopmentTools/ProductDetails/PartNO/DT100126

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1. Design Checklists

1.1 Schematic Checklist

- Is the MPU supplied with the correct voltage levels?
- Does the power management IC provide enough current for the system?
- Are the correct power supply power-up and power-down sequences implemented?
- Are the decoupling capacitors adequate?
- Is the MPU configured correctly?
- Is the DDR controller configured correctly?

1.2 Layout Checklist

- Does the board feature an uninterrupted GND plane?
- Is a proper layer stack-up defined?
- Are the decoupling capacitors placed as close as possible to the IC pins?
- Are high-speed signal lengths matched and routed over continuous planes (USB, SDCARD, DDR, etc.)?

2. Schematic Checklist Description and Examples

This section describes each item in the schematic checklist and provides implementation examples.

2.1 Provide Adequate Voltage and Sufficient Current

2.1.1 Requirements

Refer to table “Recommended Operating Conditions on Power Supply Inputs”, in chapter “Electrical Characteristics” of the SAM9X60 data sheet, for the power supplies needed to power the MPU.

The MPU requires three main voltage values:

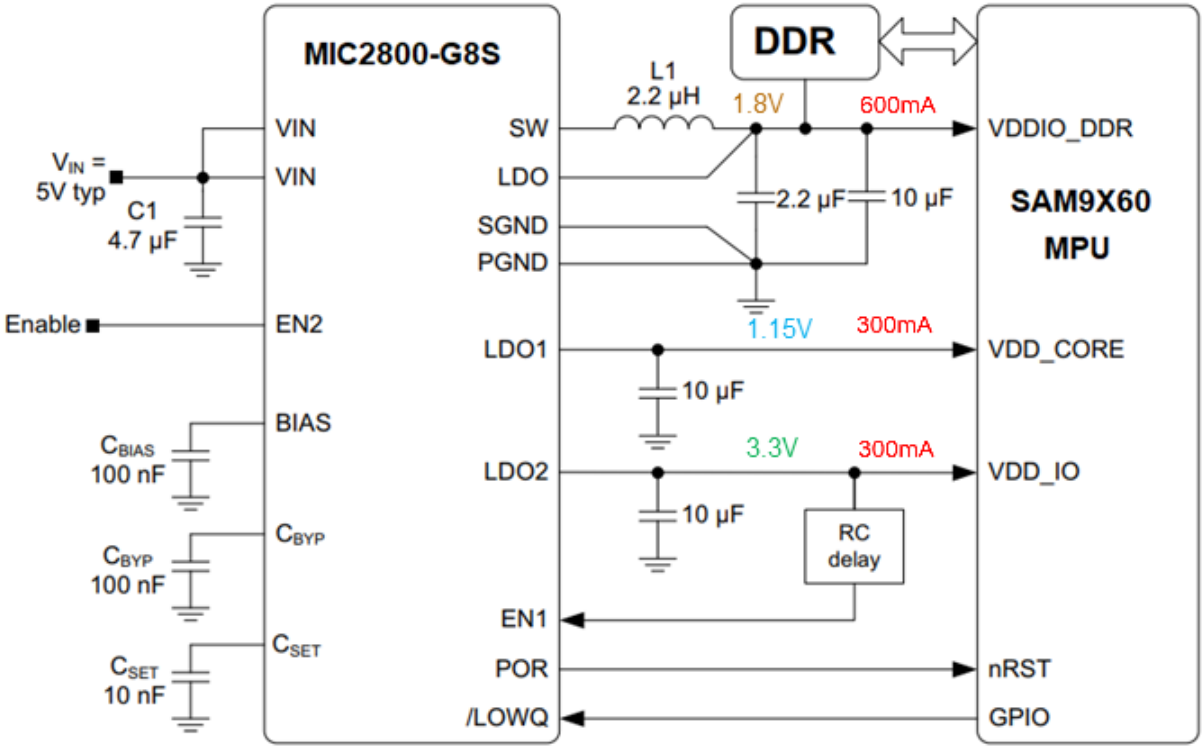
- 1.15V for VDDCORE
- 1.8V for VDDIOM*, VDDNF*, VDDQSPI*, VDDIOP[0,1]* and VDDBU*
- 3.3V for VDDIOM*, VDDNF*, VDDQSPI*, VDDIOP[0,1]*, VDDANA, VDDIN33 and VDDBU*

* These voltage rails can be connected to either 1.8V or 3.3V, depending on the application.

2.1.2 Implementation Example

The MIC2800-G8S was designed especially for this type of application, as it can output the three power supply domains required by the MPU.

Figure 2-1. MIC2800-G8S



Customers who need extra power in their design should consider the MCP16501/2, which offers four independent buck converters, each capable of outputting up to 1A of current, plus two other separate 300 mA LDOs.

2.2 Ensure Correct Power-up and Power-down Sequences

2.2.1 Requirements

Refer to figures “Recommended Power Sequence at Power-up” and “Recommended Power Sequence at Power-down” in chapter “Electrical Characteristics” of the SAM9X60 data sheet for the applicable power supply sequencing.

The “Power-up Timing Requirements” table shows that:

- VDDBU must not come after VDDIN33 later than 0.2 ms,
- VDDIN33 must be stable before (not after) all other power supplies except VDDBU,
- The NRST line must be kept low for at least 8 ms after all other power supplies have become stable.

The “Power-down Timing Requirements” table shows that:

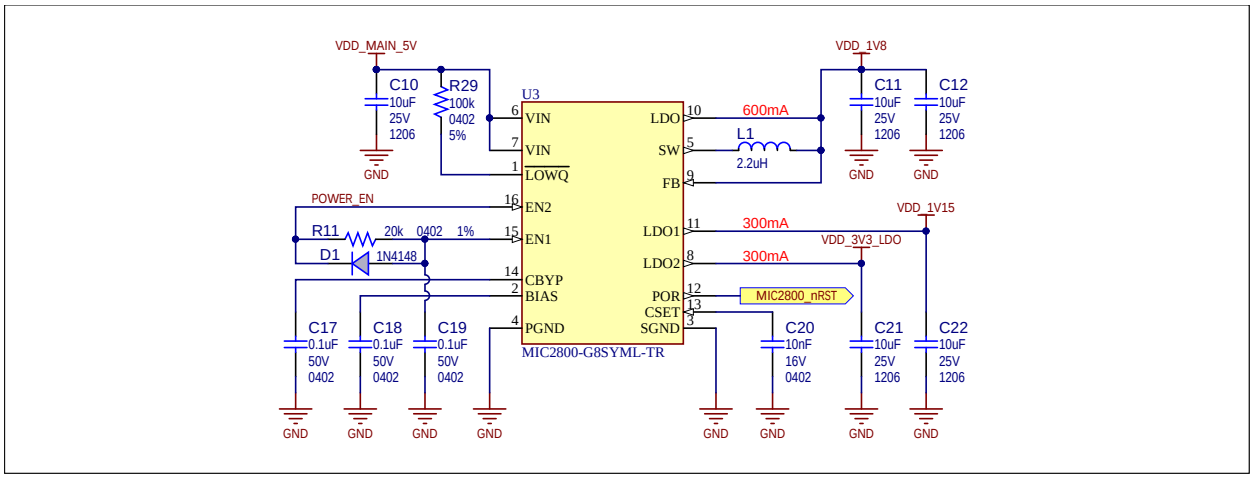
- The NRST line must be pulled low before the power supplies are powered off.

2.2.2 Implementation Example

Again, the MIC2800-G8S makes this task easy. The enable (EN) pin eases the implementation of a correct power-up sequence and the possibility of shutting down the PMIC to switch the system to a low-power consumption state, operating off a small battery.

The Power-On Reset (POR) pin with adjustable delay time keeps the MPU in reset until the power rails are stable, therefore ensuring a correct power-up sequence.

Figure 2-2. Power Management Integrated Circuit



The 20 KΩ resistor (R11) and the 0.1 µF capacitor (C19) provide a low-pass filter connected to the EN1 pin that introduces the necessary delay between the 3.3V and 1.15V rails needed for the proper operation of the MPU. The diode (D1) ensures that the capacitor discharges rapidly during the power-down sequence.

2.3 Ensure that the Power Supply Pins have Adequate Decoupling Capacitors

2.3.1 Requirements

As described in the SAM9X60 data sheet (“Electrical Characteristics”), low-impedance decoupling of the device power supply inputs must be provided. A 10 nF to 220 nF ceramic X7R (or X5R) capacitor placed very close to each power supply input is a minimum requirement.

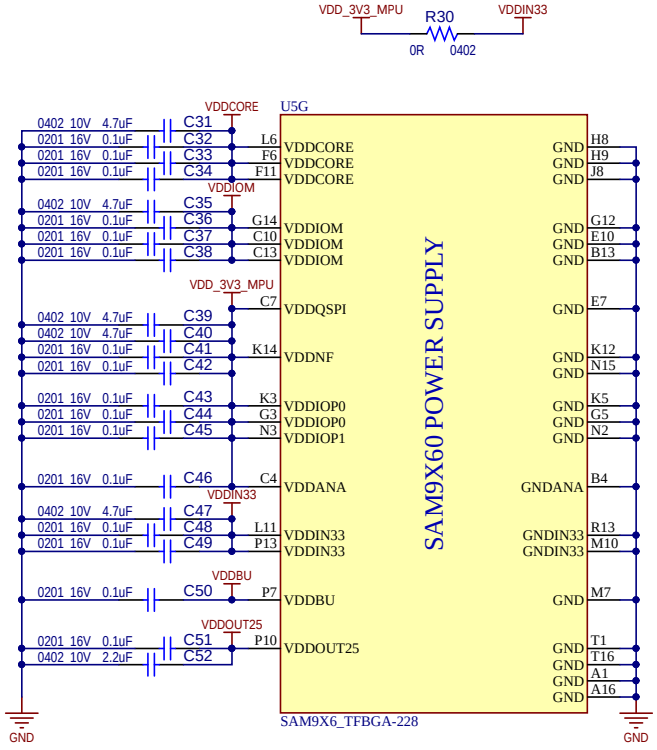
In the SAM9X60-EK, we have opted for 100 nF 0201, X5R rated at 16V multilayer ceramic capacitors with good results.

Additionally, the internal LDO that generates VDDOUT25 requires two extra capacitors. As stated in table “VDDOUT25 Voltage Regulator Characteristics” in the SAM9X60 data sheet (“Electrical Characteristics”):

- A 2.2 µF (min) capacitor should be connected at its input (at VDDIN33).
- A 2.2 µF (typ) capacitor should be connected at its output (at VDDOUT25).
- The output capacitor should have a low ESR.

2.3.2 Implementation Example

Figure 2-3. Processor Power Supplies



In addition to the 100 nF capacitors, we used several 4.7 µF 0402, X5R rated at 10V MLCCs to serve as bulk/storage elements.

While not compulsory, it is good practice to separate the input of the internal LDO (VDDIN33) from the rest with a 0R resistor. This configuration acts as a low-pass filter and is designed to attenuate any voltage spikes that can appear on the main 3.3V rail that powers the rest of the board. This helps meet the requirement stated in Note 1 of the “Recommended Operating Conditions on Power Supply Inputs” table in the SAM9X60 data sheet (”Electrical Characteristics”). The same filtering is recommended on VDDANA if the internal ADC is used.

2.4 Check MPU Configuration

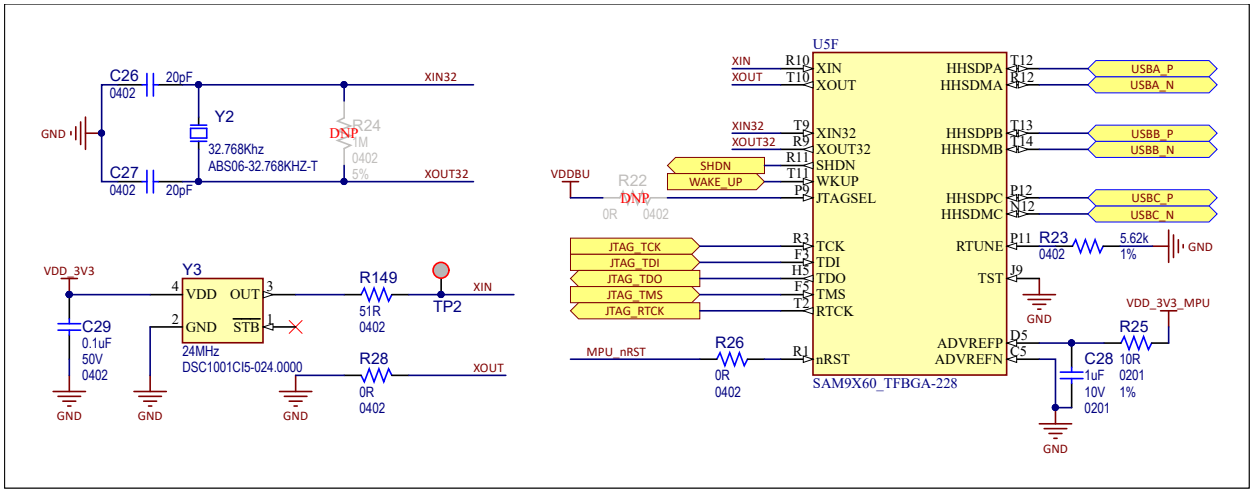
2.4.1 Requirements

- A 5.62 kΩ resistor is connected to the RTUNE pin for USB external tuning and an adequate voltage divider is placed on USB VBUS to transform the 5V into the PIO voltage.
  → Refer to section “Typical Connection” in chapters “USB High Speed Device Port (UDPHS)” and “USB Host High Speed Port (UHPHS)” of the SAM9X60 data sheet.
- The TST pin is grounded.
- The ADVREFN pin is connected to the PCB ground plane.
- If the design does not need JTAG boundary scan, tie the JTAGSEL pin to GND or leave it floating.

- A 32.768 kHz crystal is placed between XIN32 and XOUT32.
  → Refer to section “32.768 kHz Crystal Oscillator” in chapter “Electrical Characteristics” of the SAM9X60 data sheet.
- A high-frequency clock source is provided either through a crystal placed between XIN and XOUT or through an external clock generator.
- If the clock generator option is chosen, it is recommended to ground XOUT to improve stability.
  → Refer to section “Main Crystal Oscillator” in chapter “Electrical Characteristics” of the SAM9X60 data sheet.
- Clock sources should be chosen with great care.
  → Refer to section “Crystal Oscillator Design Considerations” in chapter “Electrical Characteristics” of the SAM9X60 data sheet.

2.4.2 Implementation Example

Figure 2-4. Processor Configuration



The SAM9X60-EK board features the ABS06-32.768KHZ-T crystal loaded with 20 pF capacitors to provide the 32.786 kHz slow clock and the DSC1001CI5-024.0000 MEMS oscillator to provide a 24 MHz signal to the main clock oscillator.

2.5 Check the DDR Controller Configuration

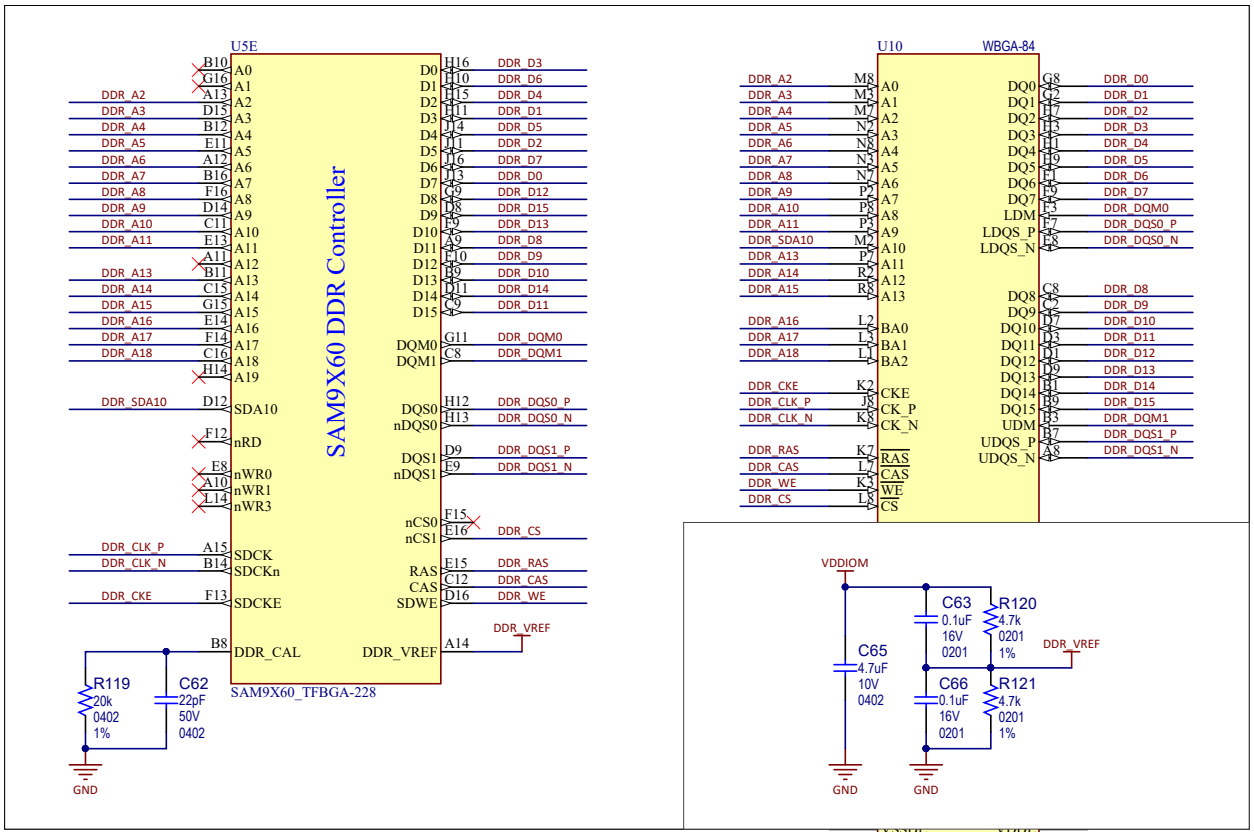
2.5.1 Requirements

- Connect the external memory chosen as required in table “EBI Pins and External Device Connections” in chapter “Electrical Characteristics” of the SAM9X60 data sheet.
- Select the correct value for DDR_CAL depending on the memory used:
  – 20 kΩ for LPSDRAM, LPDDR and DDR2
  – 16.9 kΩ for SDRAM
- Connect the DDR_VREF pin to the correct voltage:
  – VDDIOM/2 for DDR2 and LPDDR
  – GND for (LP)SDR

Refer to section “DDR/SDR I/O Calibration and DDR Voltage Reference” in chapter “Memories” of the SAM9X60 data sheet.

2.5.2 Implementation Example for DDR2

Figure 2-5. DDR Controller Configuration



In the above figure, the data bits connected to the DDR2 memory appear to be scrambled. This is called “bit swapping” and was done on purpose to ease up the layout routing. Refer to 5.1 Bit and Byte Swapping.

For other examples, refer to section “Implementation Examples” in chapter “External Bus Interface (EBI)” of the SAM9X60 data sheet.

3. Layout Checklist Description and Examples

This section describes each item in the layout checklist and provides implementation examples.

The implementation examples are based on the SAM9X60-EK (Evaluation Kit).

3.1 Check that the Board has an Uninterrupted GND Plane

3.1.1 Requirements

As described in the SAM9X60 data sheet (“Electrical Characteristics”), a PCB with a low-impedance ground plane must be provided. A single unbroken ground plane is a minimum requirement.

3.1.2 Implementation Example

Figure 3-1. Correct GND Plane

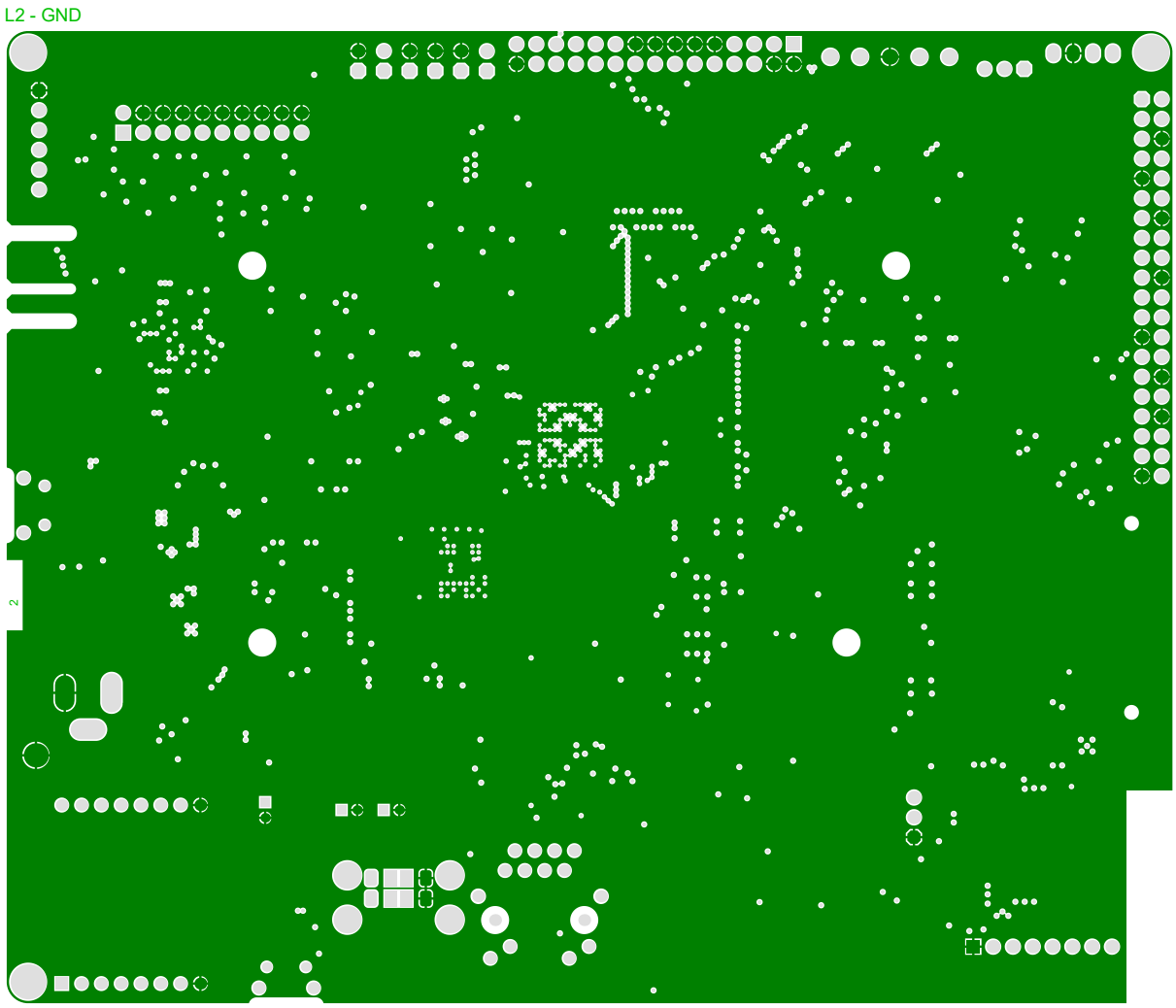
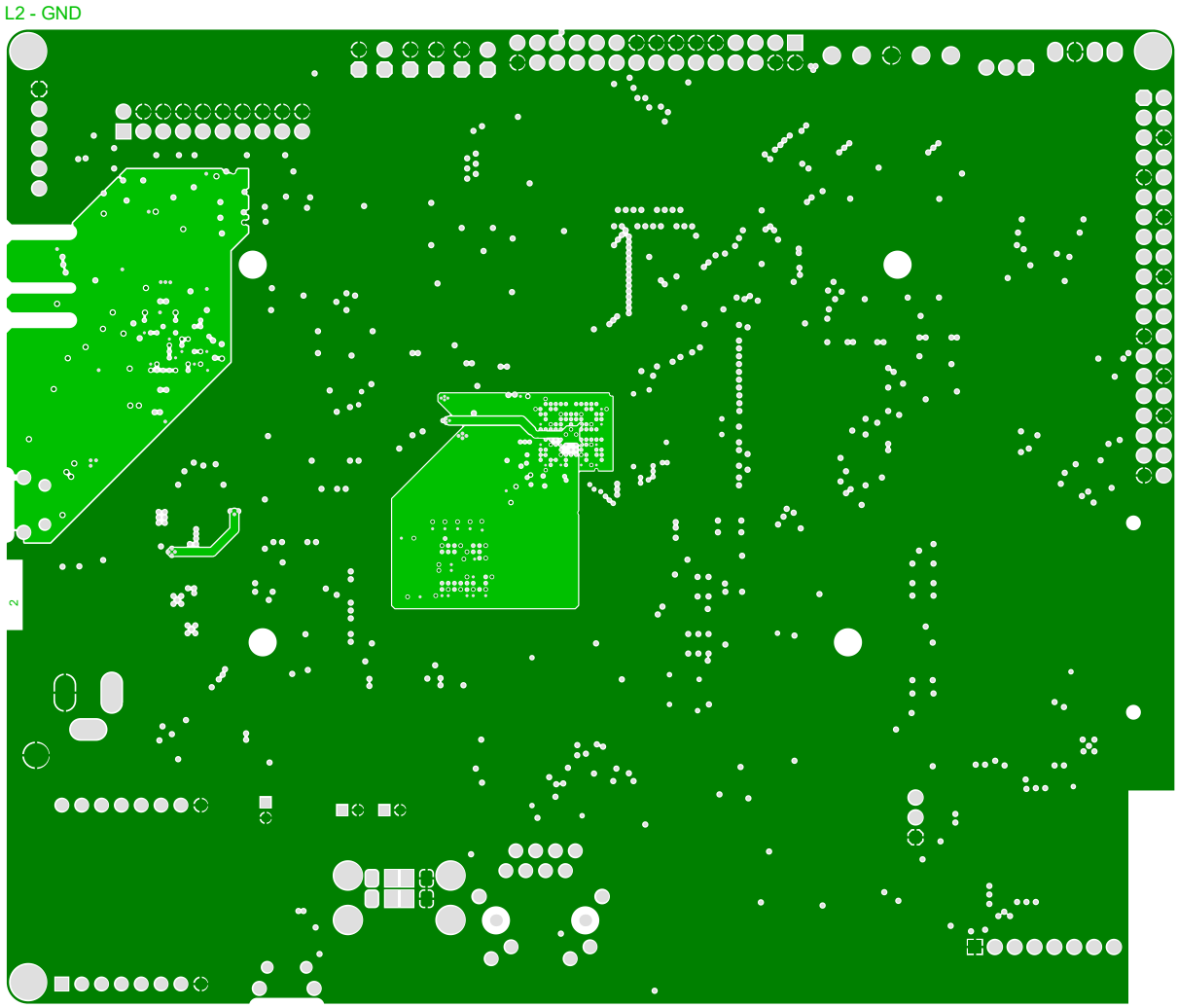


Figure 3-2. Incorrect GND Plane



The first image depicts a solid/uninterrupted GND plane that stretches all over the board. This is the ideal implementation.

The only exception to this rule can be seen in the lower right corner of the board where a small plane cut-out has been made. This is acceptable because there are no other signals routed over that area that could capture undesired external ElectroMagnetic Interference (EMI).

The second image shows several cut-outs assigned to a different power supply and also a couple of signals routed on this layer.

Such arrangement is to be avoided by all means, as it is a proven source of EMI, therefore prone to failing the EMC compliance tests.

3.2 Define a Layer Stack-up so that Line Impedances are matched to Driver Impedances

3.2.1 Requirements

Match the PCB line impedances to their corresponding driver impedances to reduce line reflections:

- Single-ended lines should have 50 Ω +/-10% single-ended impedance.

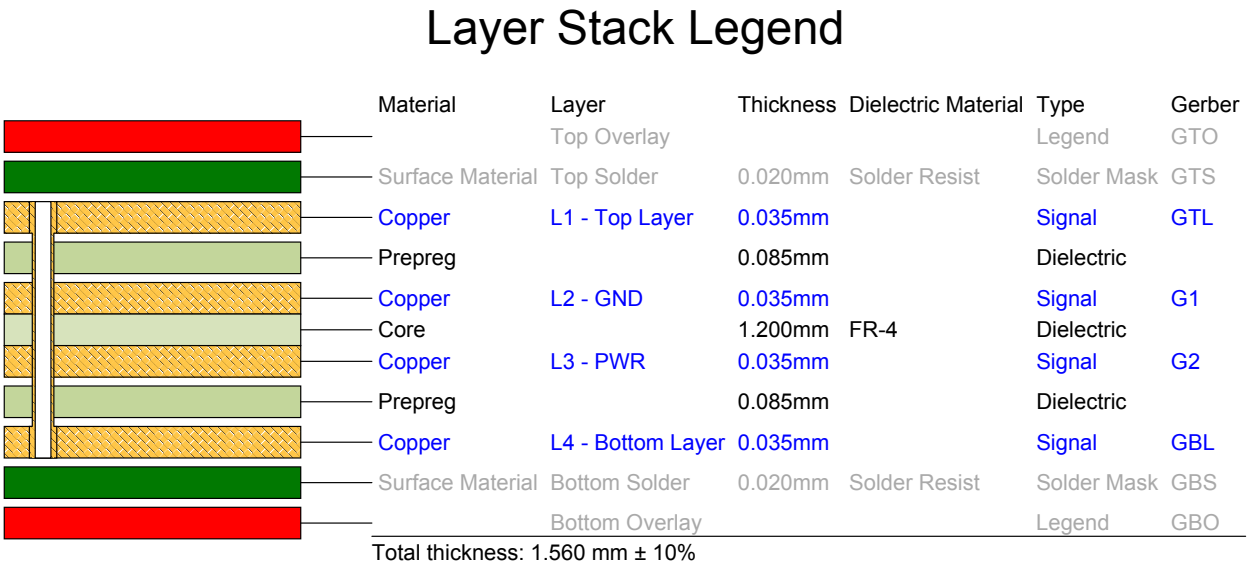
- USB lines should have 90 Ω +/-15% differential impedance.
- DDR CLOCK and STROBE should have 100 Ω +/-10% differential impedance.

3.2.2 Implementation Example

The SAM9X60 was especially engineered to be placed on a four-layer PCB.

To achieve the best performance, we recommend using the following layer stack-up and line width and clearances.

Figure 3-3. Four-Layer Stack-up



PCB Impedance Information

TYPE	IMPEDANCE	TOLERANCE	LAYER	REFERENCE	WIDTH [um]	GAP [um]
DIFF	90Ω	± 10%	L1	L2	125	200
DIFF	90Ω	± 10%	L4	L3	125	200
DIFF	100Ω	± 10%	L1	L2	100	200
DIFF	100Ω	± 10%	L4	L3	100	200
SE	50Ω	± 10%	L1	L2	125	
SE	50Ω	± 10%	L4	L3	125	

This stack-up was chosen because it can provide all the required impedances by using minimum 100 µm-wide traces.

The minimum trace width is 100 µm (~4 mil) which is relatively standard nowadays for PCB manufacturers. This also ensures that the routing does not take much space on the board.

3.2.3 Extra Tips

Important: Make sure that your PCB manufacturer can produce that specific stack-up.

The PCB manufacturer may not have the required materials in stock, and have to order it specifically, which can increase the overall production cost.

Also, the manufacturer can recommend a different layer stack-up that they can produce cheaper with the materials in stock.

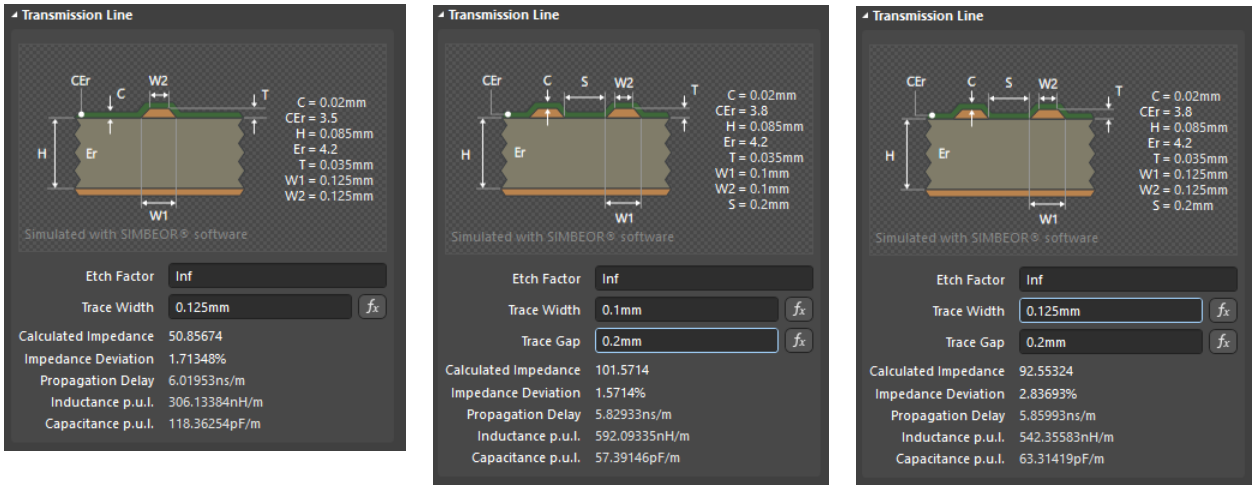
In such cases, you can easily adapt your layout to the proposed stack-up by changing the width of the traces so the required impedances are preserved. With the help of an impedance calculator tool, make sure that the recommendations previously given can still be respected (e.g. check that enlarging the traces will satisfy the impedance while not infringing the minimal spacing).

Designing proper transmission lines is easier nowadays with the help of impedance calculators available on the market.

The following example shows the Altium Designer impedance calculator.

Here, after defining the PCB stack-up, you can either use the software to compute the ideal trace width that will yield a specific impedance, or input the trace width so that the tool calculates the resulting impedance.

Figure 3-4. Impedance Calculation



The SAM9X60-EK was designed so that the final thickness of the board should be 1.6 mm. In designs that do not have this constraint, we recommend reducing the thickness of the inner core from 1.2 mm to as low as possible. This does not impact the previously calculated trace impedances, but it allows the creation of a better plane capacitor created by the close-neighboring power layer and GND layer. This plane capacitor will then be very efficient to filter high-frequency noise, as it should have a very low ESR.

3.3 Place Decoupling Capacitors as Close as Possible to IC Pins

3.3.1 Requirements

As described in the SAM9X60 data sheet (“Electrical Characteristics”), low-impedance decoupling of the device power supply inputs must be provided. A 10 nF to 220 nF ceramic X7R (or X5R) capacitor placed very close to each power supply input is a minimum requirement.

3.3.2 Implementation Example

In the following figure, capacitors are the green rectangles.

Figure 3-5. SAM9X60 Capacitor Placement

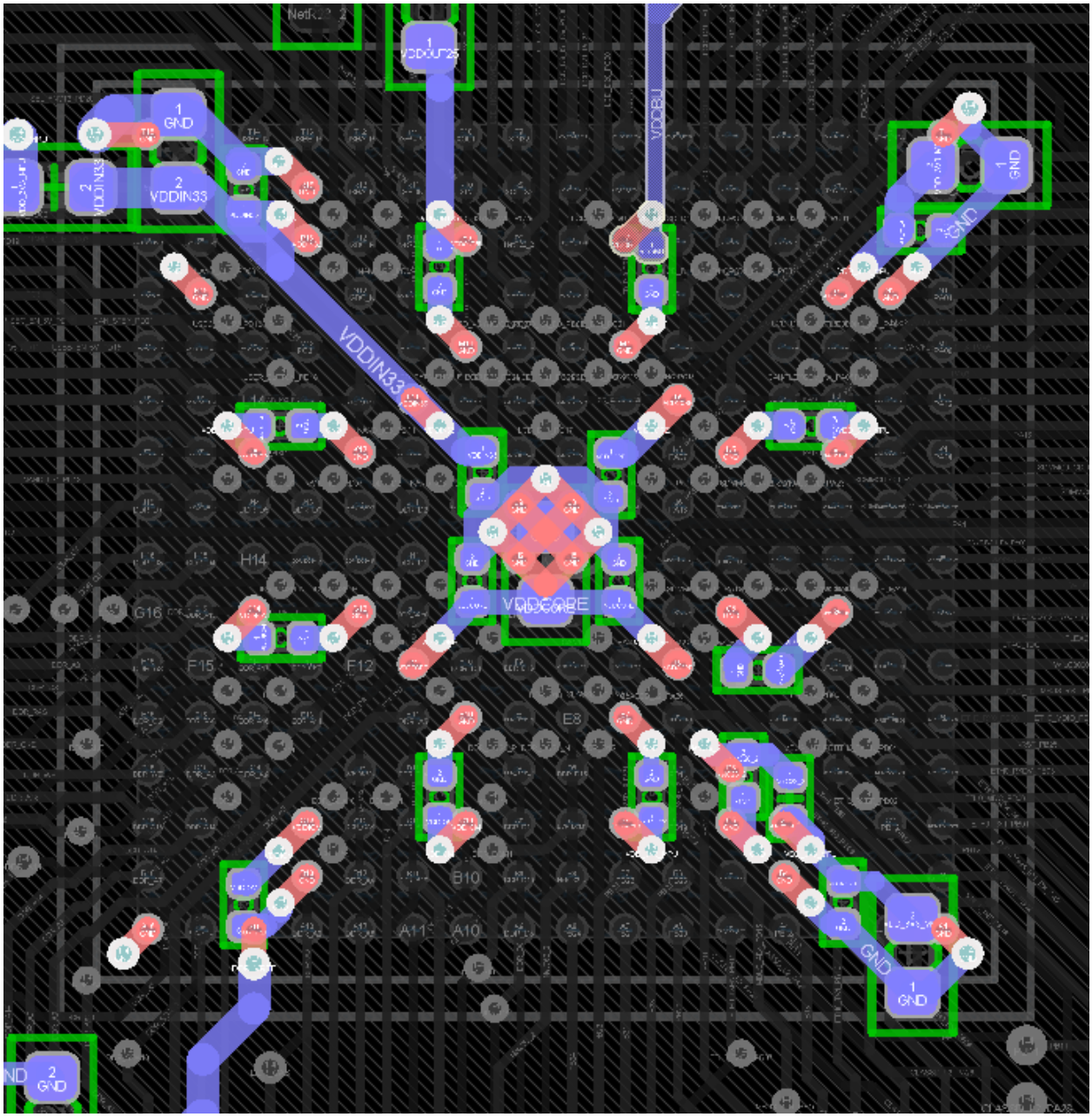
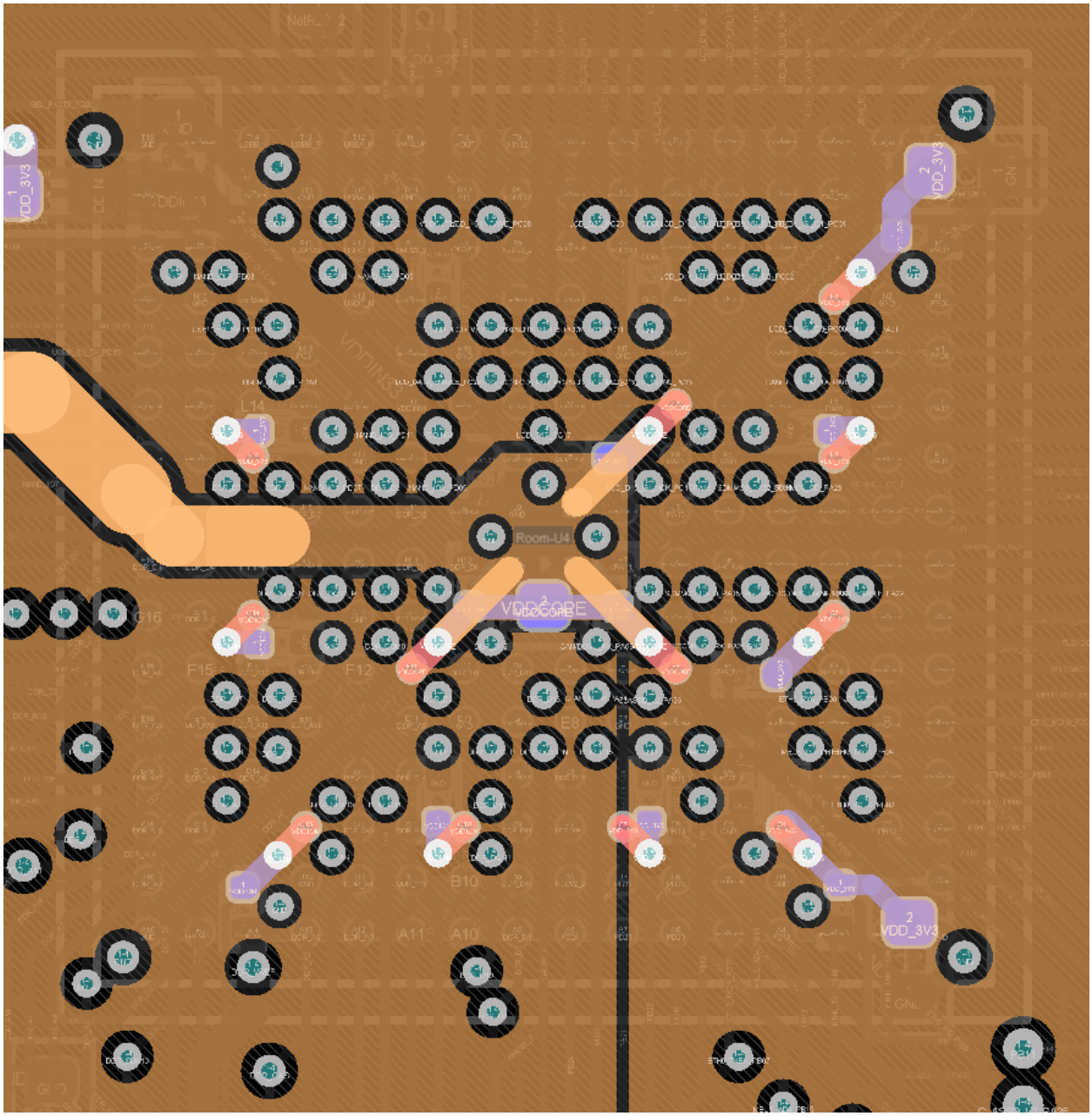


Figure 3-6. SAM9X60 Power Planes



The SAM9X60 had some of its balls strategically depopulated in order to fit 0201 decoupling capacitors on the bottom layer, right next to the power balls among the BGA array.

The power is supplied through solid copper polygons placed on the inner layer (power layer). These polygons are formed in such a way that the signals on the bottom layer have their return path through them.

In the SAM9X60-EK design files, the 3.3V plane is split to allow the user to measure the MPU power consumption. This was one of the evaluation board requirements. However, if this is not a requirement in your design, we highly recommend connecting the two planes together as depicted above.

3.4 Length-Match High-Speed Signals

3.4.1 Requirements

High-speed signals must be length-matched and routed over an uninterrupted reference plane (power or ground).

3.4.2 Implementation Example for DDR2

Figure 3-7. DDR2 Address and Control

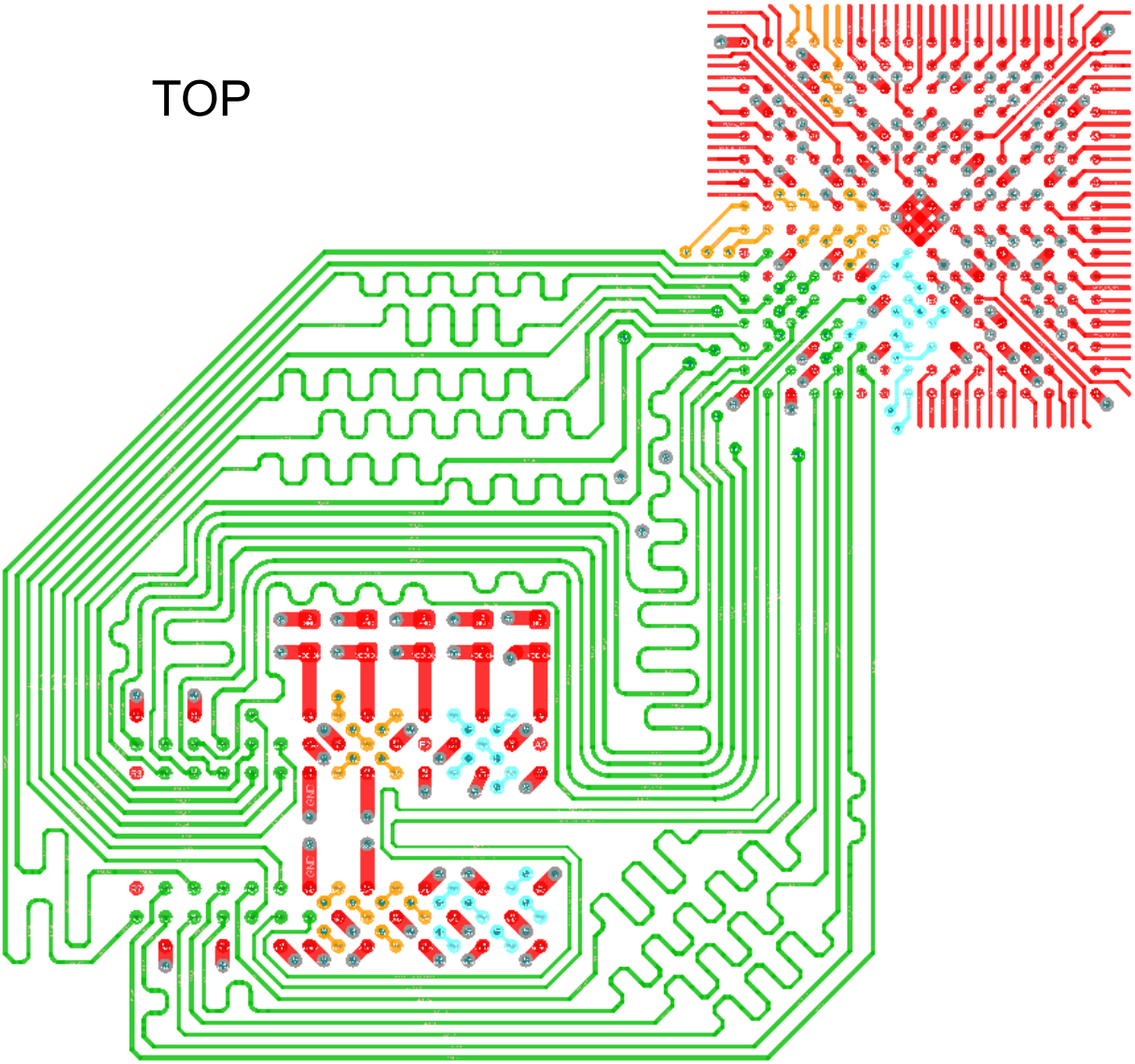
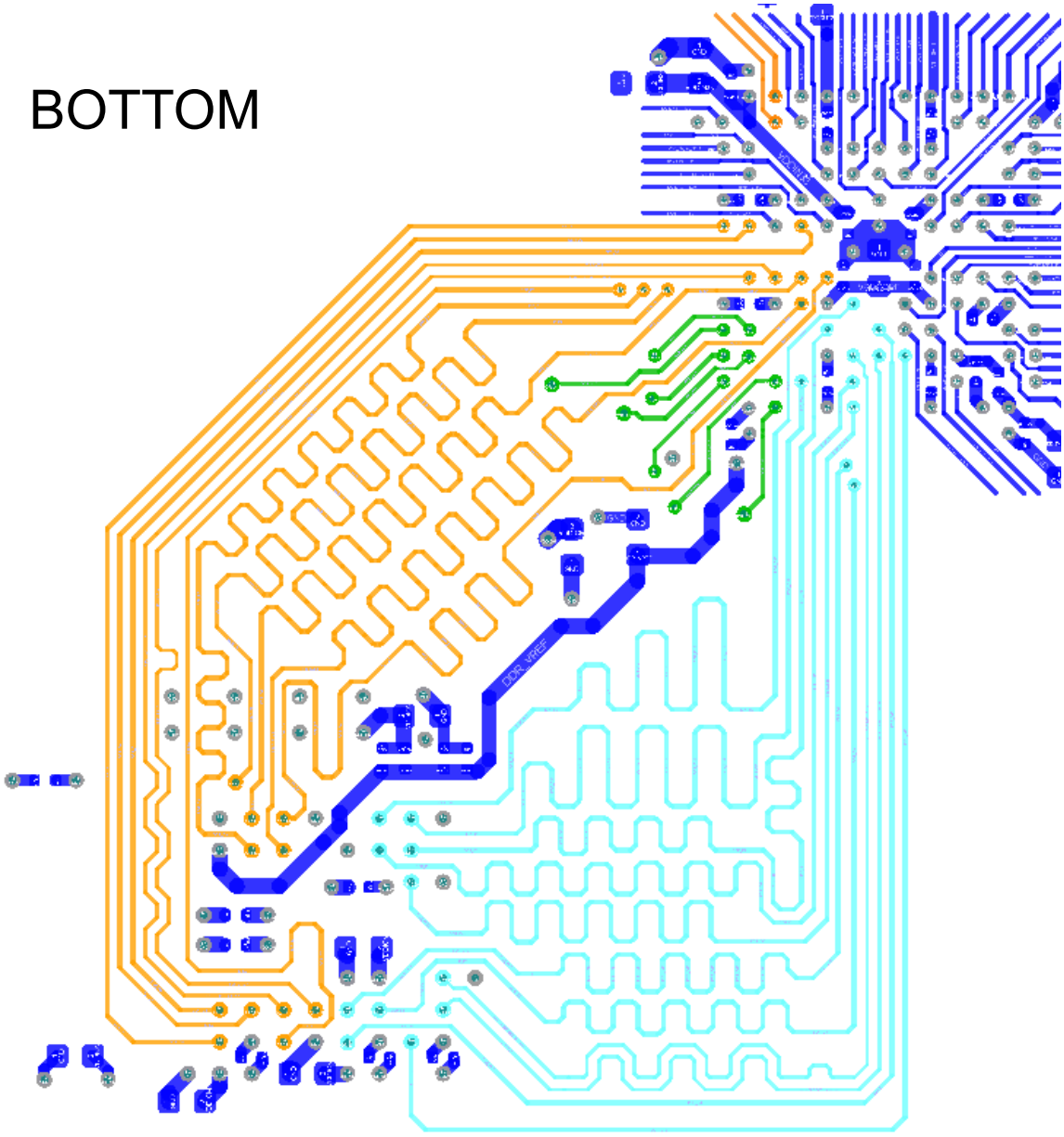


Figure 3-8. DDR2 Data Lanes



Special care was taken when designing the SAM9X60 stand-alone MPU package ball-out to ease an optimal routing path for the DDR2 memory.

It is also good practice to route signals that belong to the same group on the same layers. The above figure shows a reusable layout, where all address and control signals (green) are routed on the top layer, and all data signals (orange and light blue) are routed on the bottom layer.

4. Revision History

4.1 Rev. A - 11/2019

First issue.

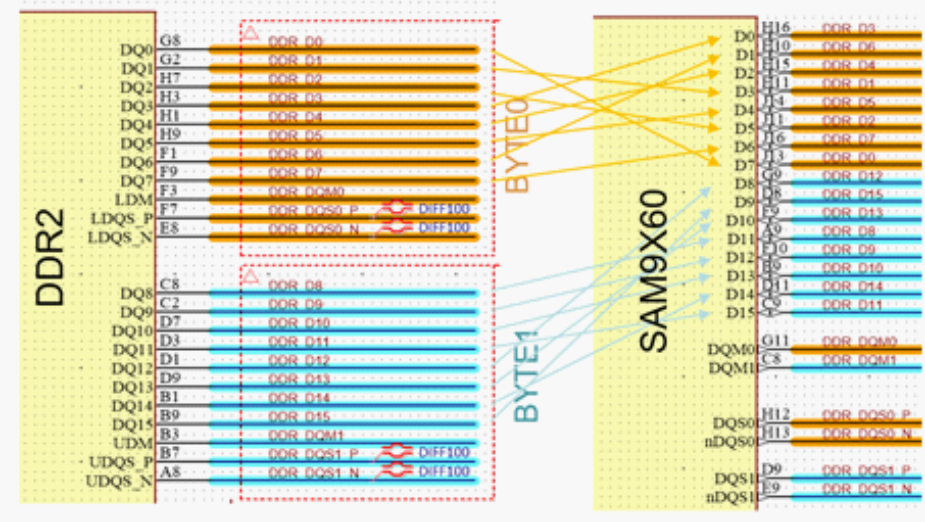
5. Appendix

5.1 Bit and Byte Swapping

DDR2 memories support **bit swapping**, a technique the designer can use to interchange data lines with one another, provided that they correspond to the same byte lane (e.g. any bits inside the D[0..7] lane). This is very useful when trying to optimize a DDR layout routing.

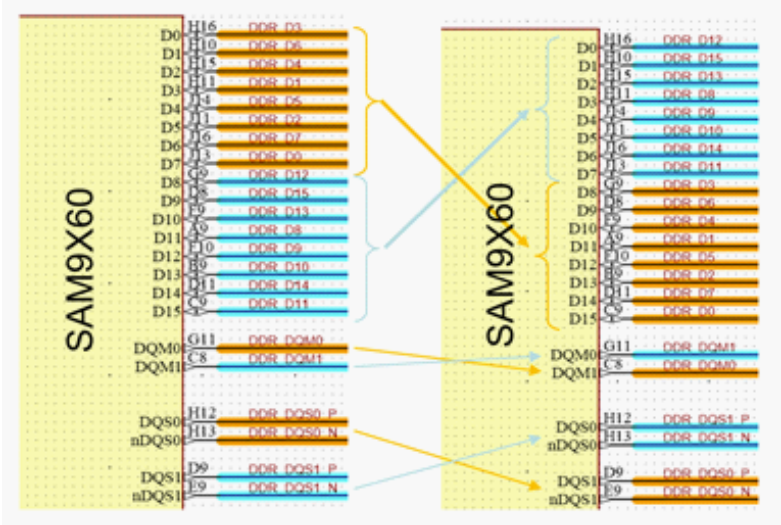
The following figure shows an example of the bit swapping technique implemented in the SAM9X60-EK board design.

Figure 5-1. DDR2 Bit Swapping



Byte swapping is another technique that can be used on DDR2 memories. It allows the designer to swap the data lanes with one another, also for the purpose of optimizing the layout. Remember to also swap the DQMx and DQSx signals corresponding to the swapped byte lanes, as illustrated below.

Figure 5-2. DDR2 Byte Swapping



5.2 Good Practices

The following is a list of suggestions for designing with high-speed signals:

- Use controlled impedance PCB traces that match the specified single-ended (50Ω) and differential (100Ω) impedance.
- Keep the trace lengths of the differential signal pairs as short as possible.
- The differential signal pair traces should be trace-length matched and the maximum trace-length mismatch should not exceed the specified values. Match each differential pair per segment.
- Maintain parallelism and symmetry between differential signals with the trace spacing required to achieve the specified differential impedance.
- Maintain maximum possible separation between the differential pairs, any high-speed clocks/periodic signals (CMOS/TTL) and any connector leaving the PCB (such as I/O connectors, control and signal headers, or power connectors).
- Route differential signals on the signal layer nearest the ground plane using a minimum of vias and corners. This will reduce signal reflections and impedance changes. Use GND stitching vias when changing layers.
- Route CMOS/TTL and differential signals on different layers, which should be isolated by the power and ground planes.
- Avoid tight bends. When it becomes necessary to turn 90°, use two 45° turns or an arc instead of a single 90° turn.
- Do not route traces under crystals, crystal oscillators, clock synthesizers, magnetic devices or ICs that use and/or generate clocks.
- Stubs on differential signals should be avoided due to the fact that stubs will cause signal reflections and affect signal quality.
- Keep the length of high-speed clock and periodic signal traces that run parallel to high-speed signal lines at a minimum to avoid crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Use a minimum of 20 mils spacing between the differential signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
- Route all traces over continuous planes (VCC or GND), avoiding cross splits or openings in those planes.
- For microstrip or stripline transmission lines, keep the spacing between adjacent signal paths at least twice the line width.
- Keep all traces at least five line widths away from the edge of the board.
- Follow the return path of each signal and keep the width of the return path under each signal path at least as wide, and preferably at least three times as wide, as the signal trace.
- To avoid EMIs, avoid routing switching signals across splits or openings in ground planes. Routing around them is preferable even if it results in longer paths.
- Minimize the loop inductance between the power and ground paths.
- Allocate power and ground planes on adjacent layers with as thin a dielectric as possible to create plane capacitance.
- Route the power and ground planes as close as possible to the surface where the decoupling capacitors are mounted.
- Supply voltages must be composed of planes only, not traces. Short connections (≈ 8 mils) are commonly used to attach vias to planes. Any connections required from supply voltages to vias for device pins or decoupling capacitors should be as short and as wide as possible to minimize trace impedance (20 mils trace width).

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