USB4715

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB4715. These checklist items should be followed when utilizing the USB4715 in a new design. A summary of these items is provided in Section 10.0, "Hardware Checklist Summary," on page 23. Detailed information on these subjects can be found in the corresponding section:

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB4715 implementor should have the following documents on hand:

- *USB4715 Data Sheet*
- *AN2651 - Configuration of Microchip USB47xx/USB49xx*
- *AN2437 - USB-to-GPIO Bridging with Microchip USB471x and USB49xx Hubs*
- *AN2438 - USB-to-I2C Bridging with USB47xx/USB49xx*
- *AN4027 - USB58xx and USB59xx FlexConnect Operation*

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connectors

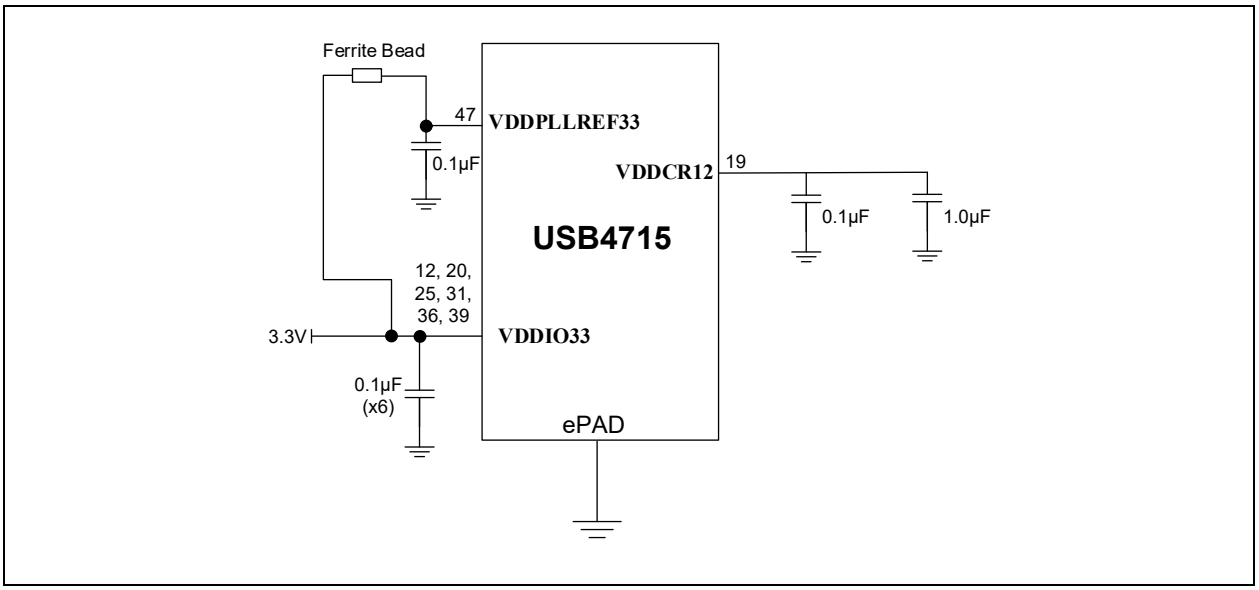
- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER

- The analog supplies (**VDDIO33**) are located on pins 12, 20, 25, 31, 36, and 39, and require a connection to a regulated 3.3V power plane.
- The **VDDIO33** pins each should include 0.1 µF capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The PLL reference supply (**VDDPLLREF33**) is located on pin 47 and requires a connection to a regulated 3.3V power plane. It is also recommended that a ferrite bead be placed between the pin and the 3.3V supply plane. Generally, a 100-220Ω (at 100 MHz) ferrite bead is used.
- Pin 19 (**VDDCR12**)is the internally generated 1.2V core power rail. Connect a 1.0 µF and 0.1 µF capacitor from pin 19 to ground using wide traces as appropriate for power distribution. Do not connect an external 1.2V source.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



Caution: This +1.2V supply is for internal logic only. ***Do not*** power other circuits or devices with this supply.

4.0 USB SIGNALS

4.1 USB PHY Interface

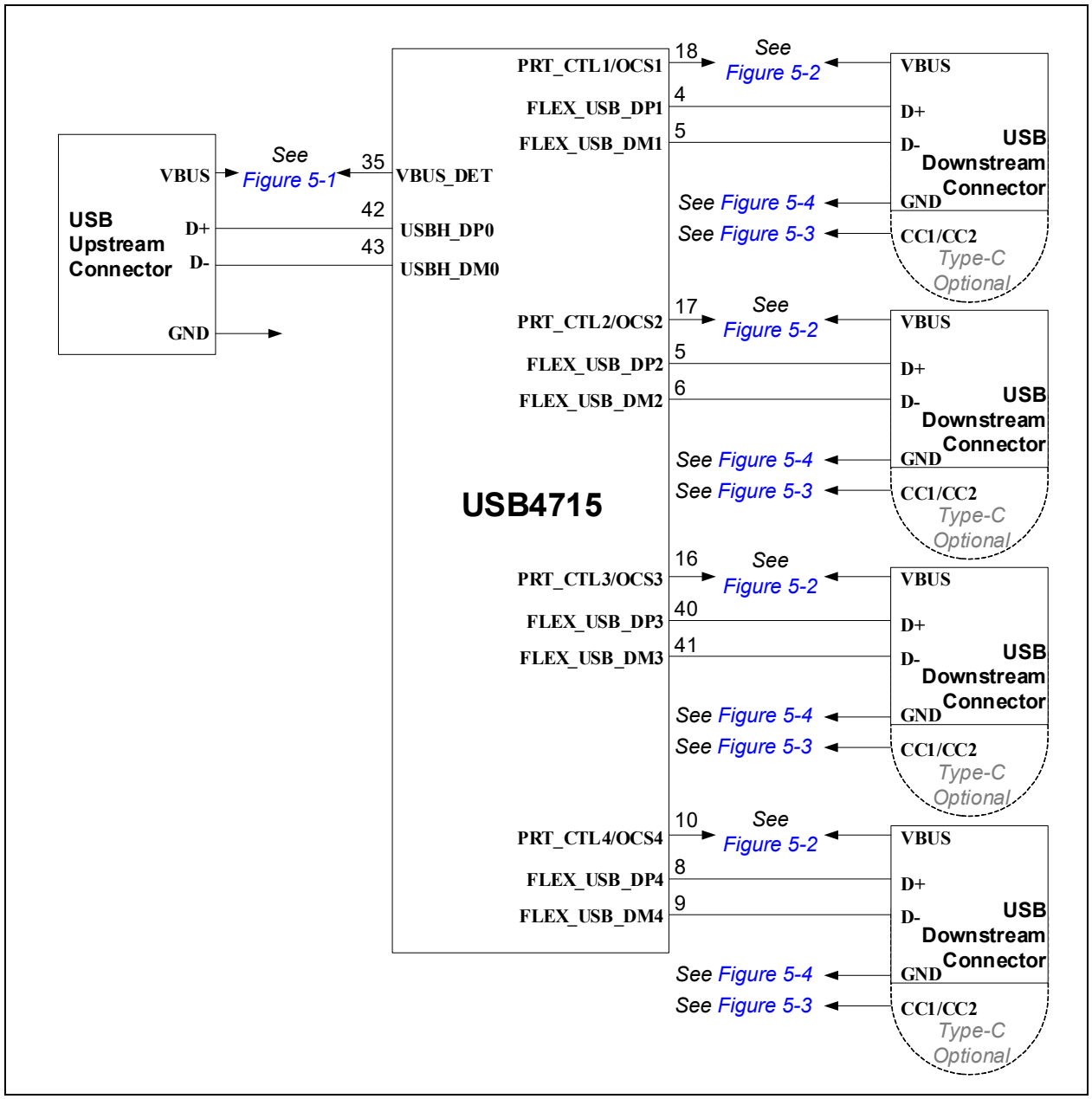
- **USBH_DP0** (pin 42): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of a USB Connector.
- **USBH_DM0** (pin 43): This pin is the negative (-) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D-/DM pin of a USB Connector.
- **FLEX_USB_DP1** (pin 4): This pin is the positive (+) signal of the downstream port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of a USB Connector.
- **FLEX_USB_DM1** (pin 5): This pin is the negative (-) signal of the downstream port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D-/DM pin of a USB Connector.
- **FLEX_USB_DP2** (pin 6): This pin is the positive (+) signal of the downstream port 2 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness. This should not be wired to a user-accessible USB port.

- **FLEX_USB_DM2** (pin 7): This pin is the negative (-) signal of the downstream port 2 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness. This should not be wired to a user-accessible USB port.
- **FLEX_USB_DP3** (pin 40): This pin is the positive (+) signal of the downstream port 3 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of a USB Connector.
- **FLEX_USB_DM3** (pin 41): This pin is the negative (-) signal of the downstream port 3 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D-/DM pin of a USB Connector.
- **FLEX_USB_DP4** (pin 8): This pin is the positive (+) signal of the downstream port 4 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness. This should not be wired to a user-accessible USB port.
- **FLEX_USB_DM4** (pin 9): This pin is the negative (-) signal of the downstream port 4 USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of an embedded device or second tier hub either directly on the PCB or through a permanently attached USB cable/wiring harness. This should not be wired to a user-accessible USB port.

  Note: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via OTP or SMBus/I^2C configuration registers.

For transmit and receive channel connections details, refer to Figure 4-1.

FIGURE 4-1: USB DATA SIGNAL CONNECTIONS



4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

If any downstream port of the USB4715 is unused, it should be disabled. This can be achieved through hub configuration (I^2C or OTP) or through a port disable strap option.

If using the port disable strap option, the FLEX_USB_DPX and FLEX_USB_DMX signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net or through a pull-up resistor.

4.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short-to-battery protection
- Common-mode chokes
  - For EMI reduction

The USB4715 can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have and to select components accordingly and follow the implementation guidelines from the manufacturer of these devices. You may also use the following general guidelines for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- Place ESD protection devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note: Microchip PHYBoost, VariSense, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help to overcome marginal failures. It is simplest to determine the appropriate setting using lab experiments, such as USB eye diagram tests, on the physical hardware.

5.0 USB CONNECTORS

5.1 Upstream Port VBUS and VBUS_DET

The upstream port VBUS line must have no more than 10 µF of total capacitance connected.

The **VBUS_DET** pin is used by the USB4715 to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft reset and reconnection of the USB4715.

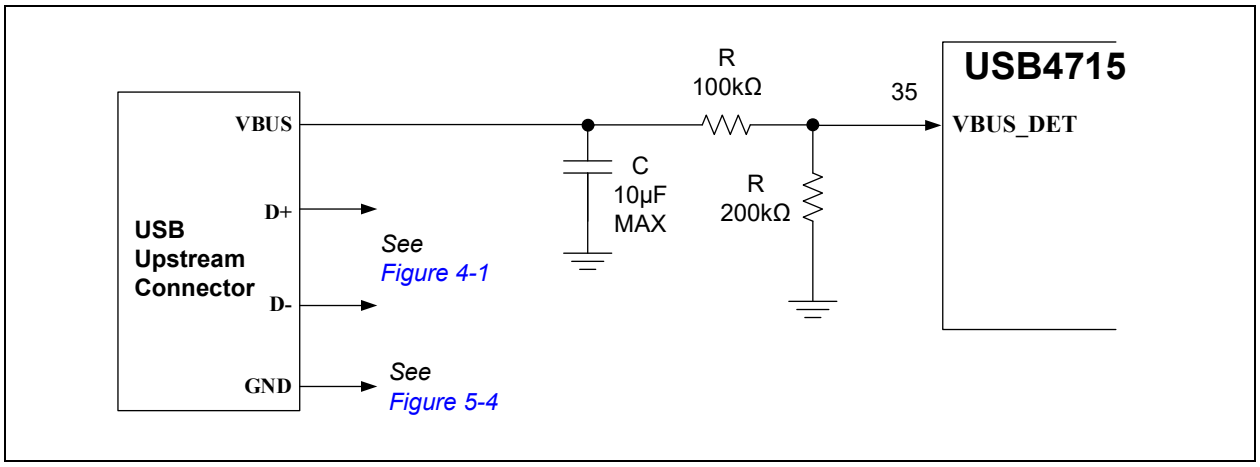
It is permissible to tie VBUS_DET directly to 3.3V. However, this is not recommended for the following reasons:

- The ability to force a hub reset from the USB host VBUS toggling is lost.
- When using the FlexConnect feature of the hub, VBUS_DET is typically used to allow the port 0 host to take back control of the hub while Flexed (port 0 host forces VBUS_DET low to revert the hub to the default state). If tied to 3.3V, this option is not available.
- When using BC1.2 Charging Downstream Port (CDP) (that is, Charging + Data) and Dedicated Charging Port (DCP) (that is, Charge-Only) features, VBUS_DET is key to indicating when the hub should switch from CDP to DCP modes, and vice versa.

The recommended implementation is shown in Figure 5-1. Note the precise resistor values are not critical and alternate values may be selected as long as:

- The impedance from the **VBUS** pin of the USB connector to the **VBUS_DET** pin is sufficiently high to minimize pin leakage when VBUS is present before the hub IC is powered on.
- A sufficient voltage level is present on the **VBUS_DET** pin for the full range of VBUS (4.5V to 5.5V).

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS



5.2 Downstream Port VBUS and PRT_CTLx

The **PRT_CTLx/OCSx** pin is a hybrid input/output (I/O) pin that has the following states:

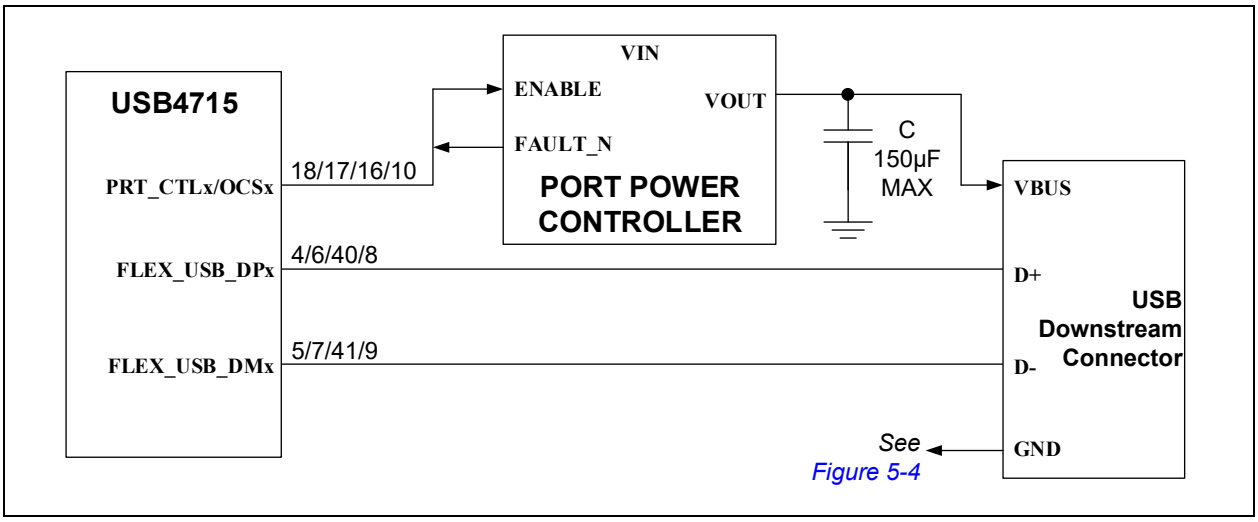
- *PORT OFF*: **PRT_CTLx/OCSx** is an output and drives low. The **PRT_CTLx/OCSx** pin will only transition to the PORT ON state through a specific command from the USB host.
- *PORT ON*: **PRT_CTLx/OCSx** is an input with an internal weak pull-up enabled. The input buffer monitors for over-current events, which are indicated by the port power controller by pulling the PRT_CTLx/OCSx line low. Once an overcurrent event is detected, the PRT_CTLx/OCSx automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **PRT_CTLx/OCSx** pin to a port power controller, the signal should be connected to both the enable and the fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

Note: The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

A typical implementation is shown in Figure 5-2.

FIGURE 5-2: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS



The implementation as shown in Figure 5-2 assumes that the port power controller has an active-high enable input, and an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 Downstream Port Type-C Support

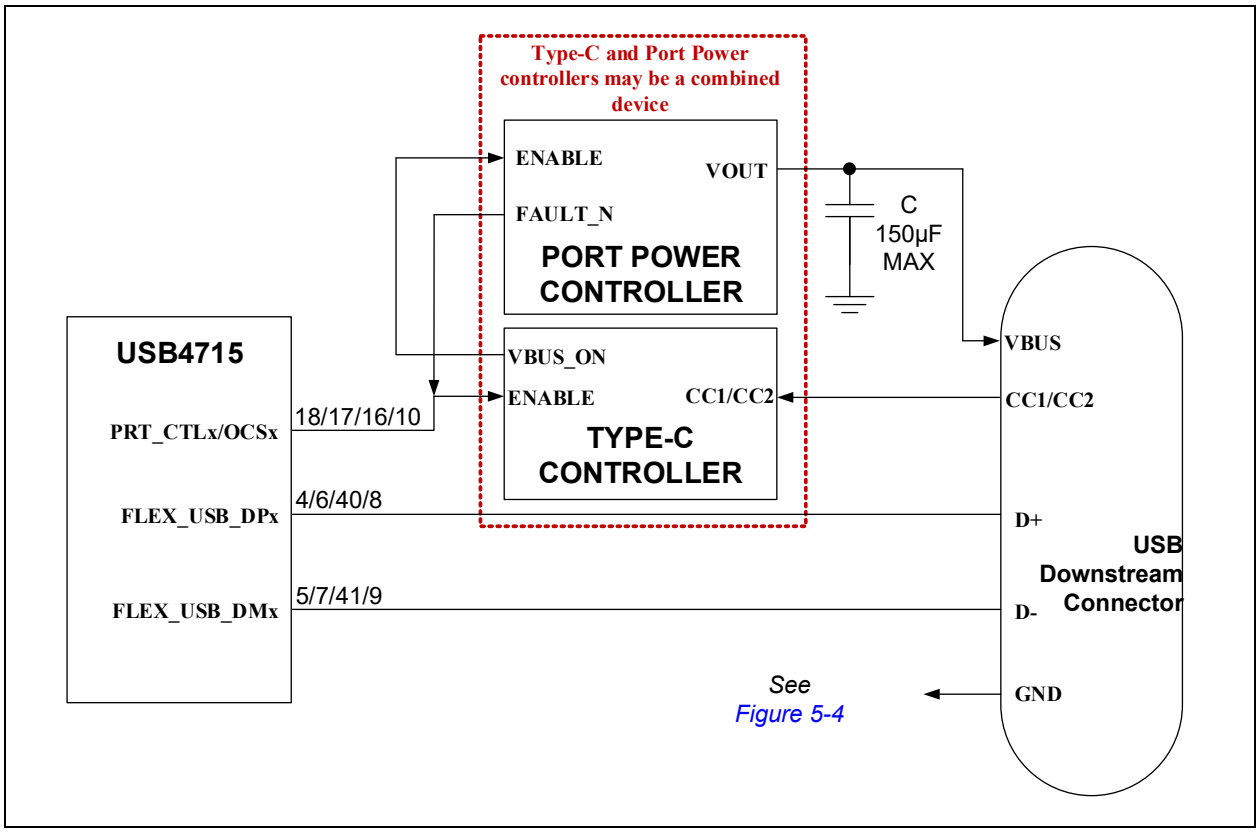
USB4715 may be used with Type-C as the downstream port. This requires a Type-C port controller or combined port power controller and Type-C port controller. The USB4715 simply controls the Type-C port controller in same way it would control a standard Type-A port power controller. The does not require any kind of Type-C port status information from the Type-C port controller.The PRTCTL1 signal should be connected to an enable pin on the Type-C controller as well as the fault indicator output of the port power controller.

If the Type-C controller and the port power controller are separate devices, the Type-C controller must control the enable pin of the port power controller. PRTCTL1 should not directly control the enable pin of the port power controller.

A Type-C controller may be configured to signal a 500 mA, 1.5A, or 3.0A port power capability. The selected port power controller should be sized accordingly.

A typical implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM VBUS AND PRTCTL1 CONNECTIONS WITH A TYPE-C PORT



The implementation as shown in Figure 5-3 assumes that the Type-C controller has an active-high enable input, and the port power controller has an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller, the port power controller, or both have different I/O characteristics.

5.4 GND and EARTH Recommendations

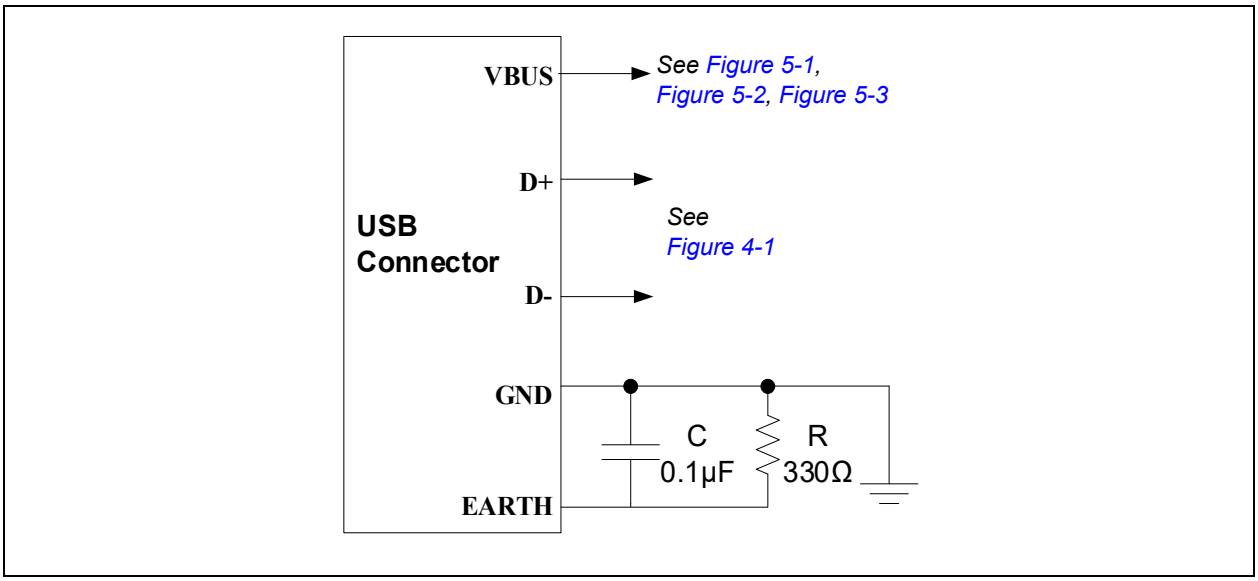
The **GND** pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (Recommended) To the GND plane through an resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Directly to the GND plane.

The recommended implementation is shown in Figure 5-4.

FIGURE 5-4: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

A 25.000 MHz (±50 ppm) reference clock is the source for the USB interface and for all other functions of the device. For exact specifications and tolerances, refer to the latest revision of the *USB4715 Data Sheet*.

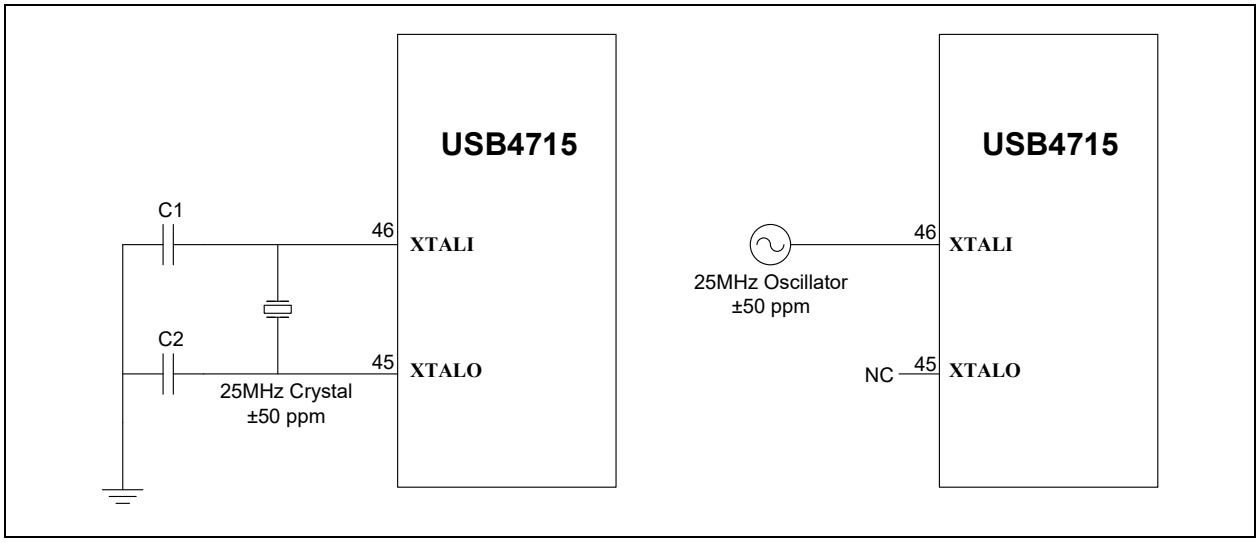
- **XTALI** (pin 38) is the clock circuit input for the USB4715. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XTALO** (pin 37) is the clock circuit output for the USB4715. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- The crystal loading capacitor values are system-dependent, based on the total C_L spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly-used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:

  $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$

  Where: C_L is the specification from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$

  Note: C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, in the 1-2 pF range, and then verified by physical experiments in the lab if PCB simulation tools are not available.
- Alternately, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the USB4715. When using a single-ended clock source, **XTALO** should be left floating as No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

RBIAS (pin 48) on the USB4715 must connect to ground through a 12 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close as possible to the IC pin, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB4715 Data Sheet*.

If a monotonic/fast power rail rise cannot be assured, then the RESET_N signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

7.2.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying sufficient power for all exposed USB ports concurrently without drooping below the minimum voltage permissible in the USB specification:

- 500 mA per-port for USB2 ports if BC1.2 is not enabled on the port
- 900 mA per-port for USB3 ports if BC1.2 is not enabled on the port
- 1.5A per BC1.2-enabled port (if BC1.2 is enabled)
- 1.5A or 3.0A per Type-C port (depending on setting of the Type-C controller)

The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized such that is able to supply the maximum power consumption specification as displayed in the *USB4715 Data Sheet*.

7.3 Reset Circuit

RESET_N (pin 34) is an active-low reset input. This signal resets all logic and registers within the USB4715. A hardware reset (RESET_N assertion) is not required following power-up. Please refer to the latest copy of the *USB4715 Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the USB4715 when reset is triggered by the power supply.The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

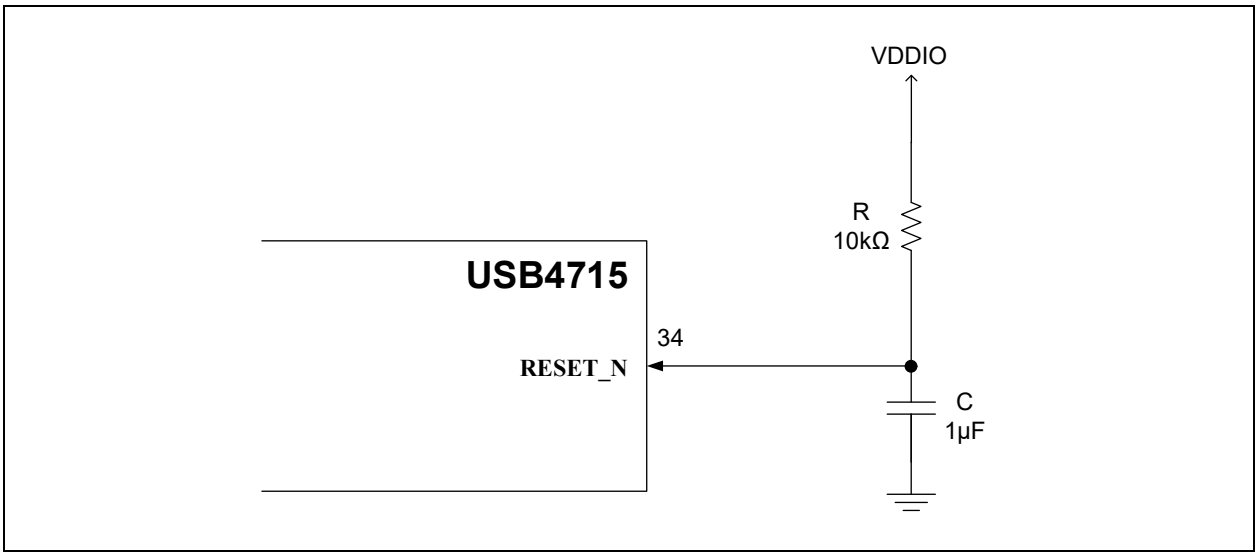
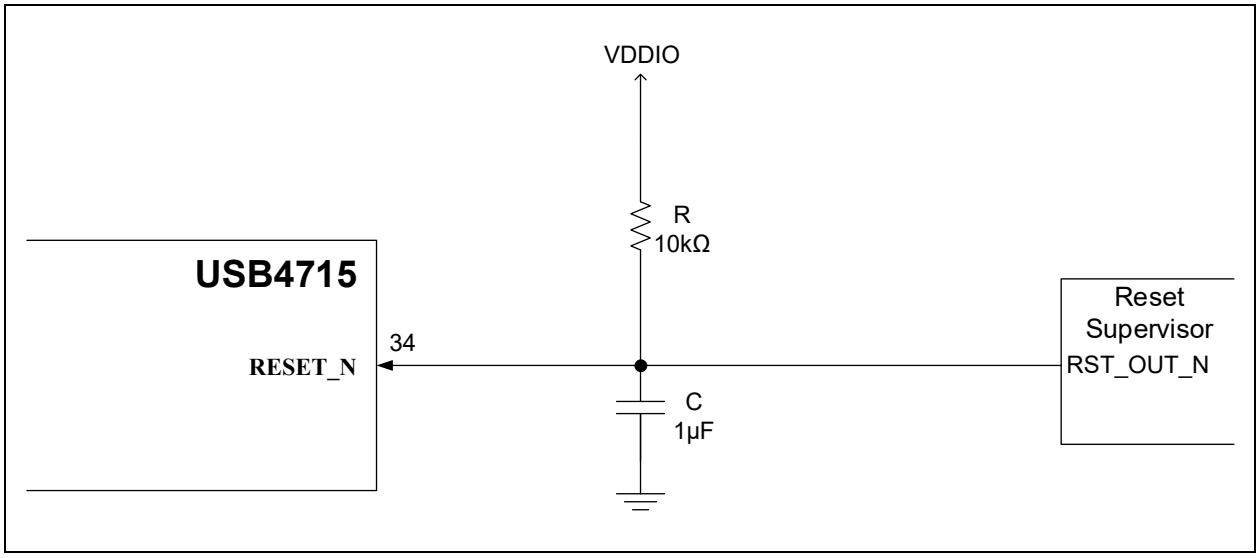


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm reset after power-up. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 EXTERNAL SPI MEMORY

8.1 SPI Operation Summary

By default, the USB4715 executes firmware from an internal read only memory (ROM). The USB4715 supports optional firmware execution from an external SPI Flash device. An SPI Flash device is only required if a custom firmware is required for the application.

The SPI interface can operate at 60 MHz or 30 MHz.

The SPI interface can operate in Dual mode or Quad mode.

The firmware image can be executed in one of two ways:

- *Execute in place*: Firmware is continuously executed directly from the SPI Flash device, and the interface is constantly active.
- *Execute in internal SRAM*: Firmware is loaded into the hub's internal SRAM and executed internally. This may only be supported if the firmware image is smaller than the hub's SRAM size.

Note: All firmware images are developed, compiled, tested, and provided by Microchip. The SPI interface speed is an OTP-configurable option and only speeds that were specifically tested with the firmware image should be selected. The execution method is configured with the firmware image itself and cannot be changed via configuration.

8.2 Compatible SPI Flash Devices

Microchip recommends SST-brand SPI Flash devices. Microchip has verified compatibility of the following list of SPI Flash devices:

- SST26VF016B
- SST26VF016
- SST26VF032B
- SST26VF064B
- SST26VF016
- SST26VF020B
- SST25VF040B
- SST25VF080B
- SST25VF040C
- SST25VF064C
- W25X30
- AT25SF041

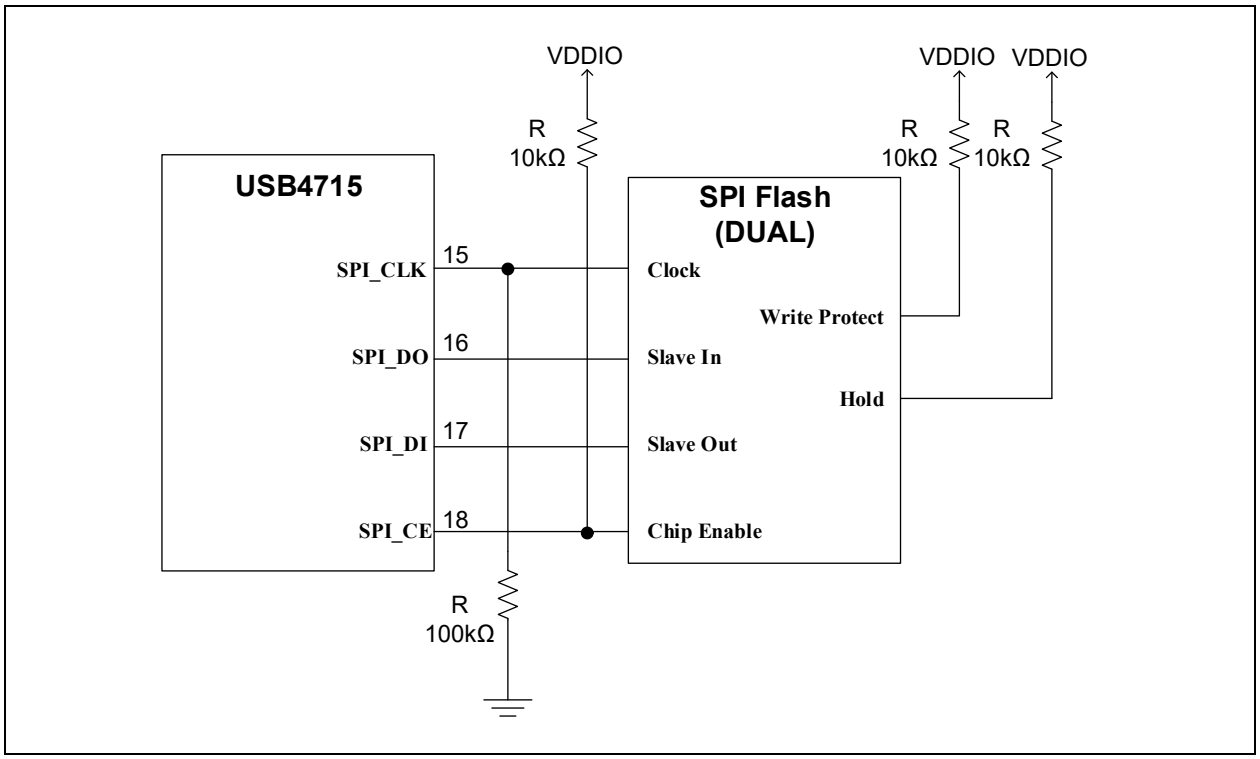
Other SPI Flash devices may be used, provided that they meet the following minimum requirements:

- 30 MHz or 60 MHz operation
- Mode 0 or Mode 3
- 256 KB or larger memory
- Utilize same OpCode commands as the devices in the above list of compatible devices
- Dual mode or Quad mode operation

8.3 SPI Connection Diagrams

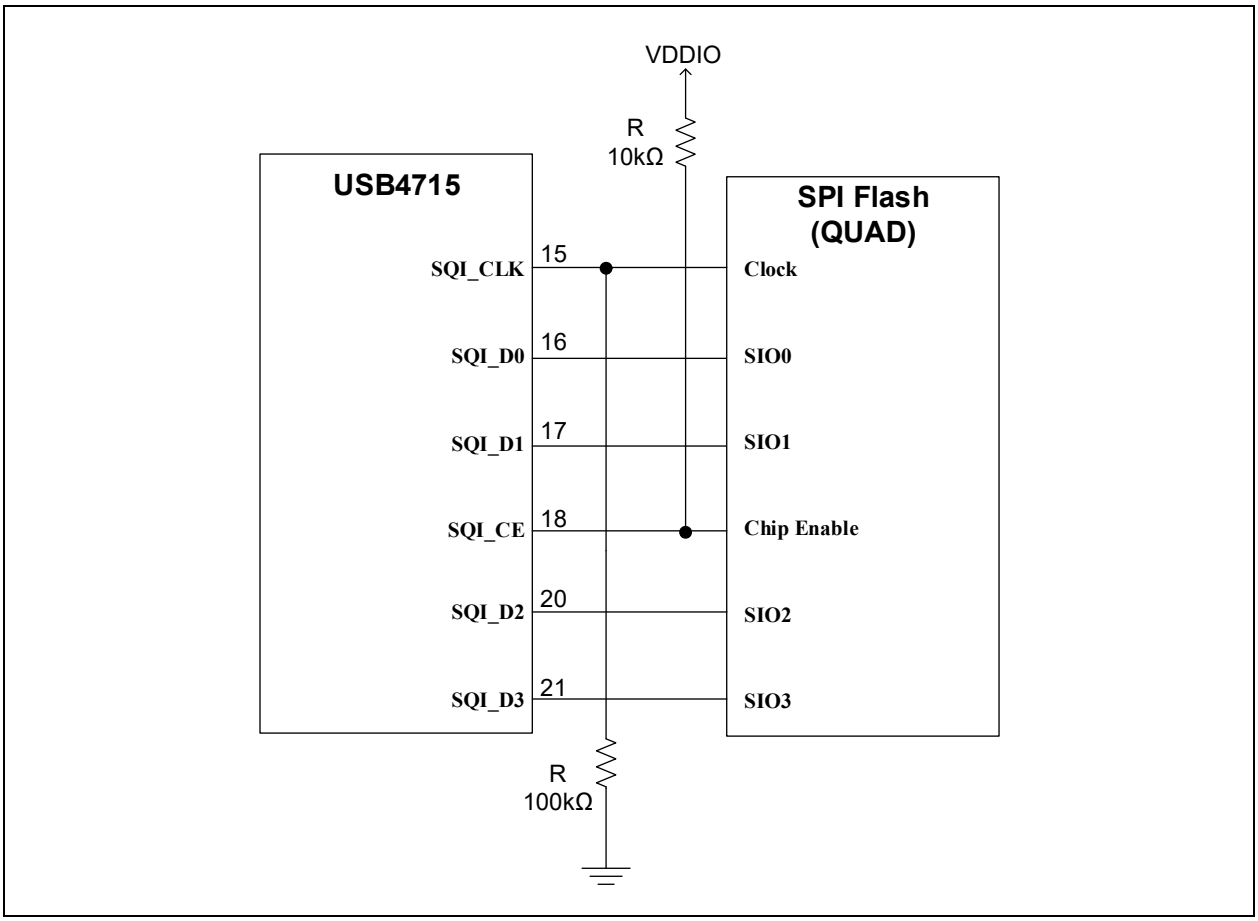
If a Dual SPI Flash device is used, the recommended schematic connections are shown in Figure 8-1.

FIGURE 8-1: DUAL SPI FLASH CONNECTIONS



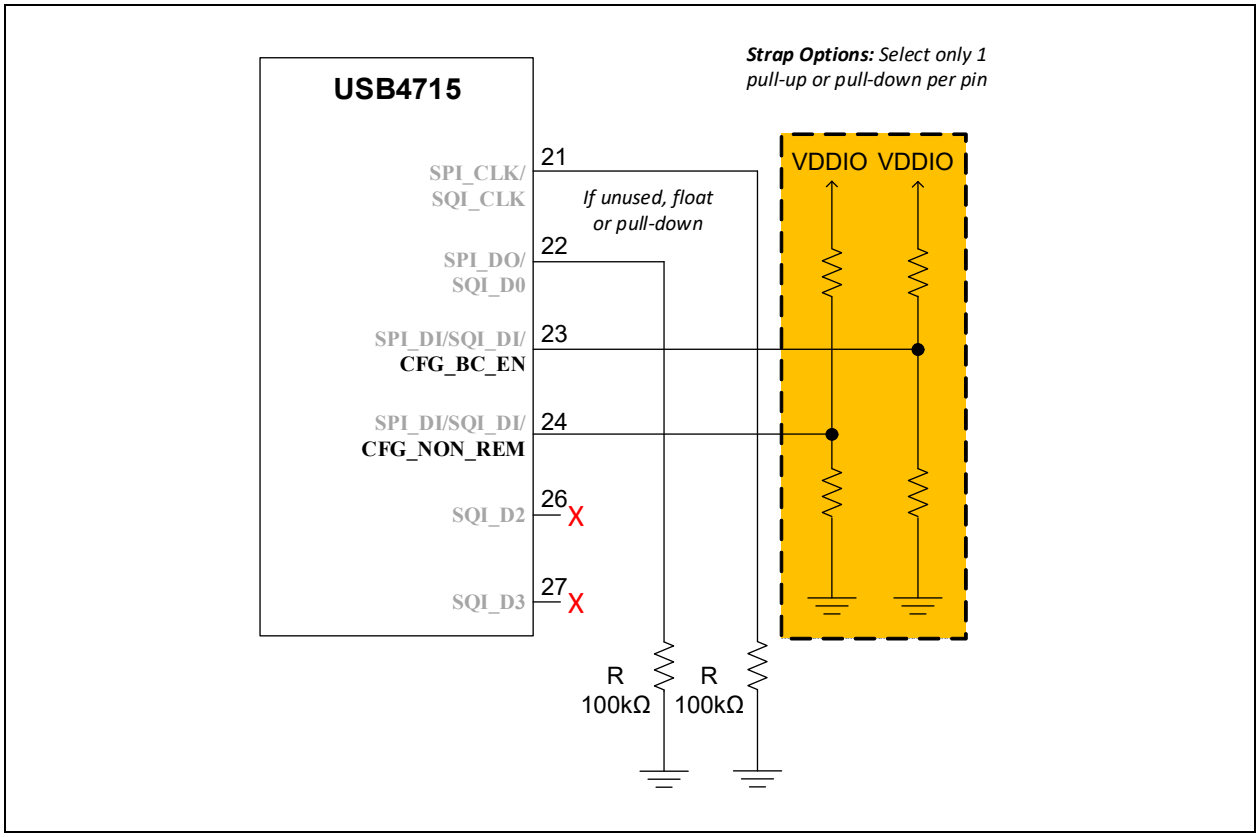
If a Quad SPI Flash device is used, the recommended schematic connections are shown in Figure 8-2.

FIGURE 8-2: QUAD SPI FLASH CONNECTIONS



If an SPI Flash device is not used, the recommended schematic connections are shown in Figure 8-3. Some of the SPI pins become configuration straps when an SPI Flash device is not connected. A configuration strap option must be selected, and these pins cannot be floated.

FIGURE 8-3: RECOMMENDED CONNECTIONS IF SPI FLASH IS NOT USED



9.0 MISCELLANEOUS

9.1 GPIOs

The four GPIO pins included on the USB4715 may be controlled from the USB host or from an embedded SOC/MCU. These GPIOs are available to be used without any additional configuration. By default, all of the GPIOs are configured as inputs. If a default output power-on state is required, the default pin output state can be configured in the hub's OTP memory or through the I^{2}C/SMBus slave interface during the configuration stage (SOC_CFG). These pins are described in Table 9-1.

TABLE 9-1: AVAILABLE GPIOS

Pin	Pin Name	GPIO Number	Required Configuration
30	PROG_FUNC_4	GPIO6	Configuration mode 2, 4, or 5; or manual override configuration via OTP or SMBus during runtime
29	PROG_FUNC_5	GPIO8	Configuration mode 2, 3, or 4; or manual override configuration via OTP or SMBus during runtime
28	PROG_FUNC_6	GPIO1	Configuration mode 2, 3, or 4; or manual override configuration via OTP or SMBus during runtime
11	PROG_FUNC_7	GPIO11	Configuration mode 2, 4, 5, or 6; or manual override configuration via OTP or SMBus during runtime

Instructions for operating these pins, including register definitions, are described in full in *AN2437 - USB to GPIO Bridging with Microchip USB471x and USB49xx Hubs*.

Ensure that the voltages applied to these pins are within the electrical specifications for the pins, and that any external loading is within the drive strength capabilities as described in the *USB4715 Data Sheet*.

9.2 I^{2}C/SMBus Connections

Two I^{2}C/SMBus interfaces are available on USB4715. These are described in Table 9-2.

TABLE 9-2: I^{2}C/SMBUS PINS

Pin	Pin Name	Pin Role	Required Configuration
37	PROG_FUNC1	SMB1_DAT USB to I^{2}C Master Data	Any Configuration Mode
38	PROG_FUNC8	SMB1_CLK USB to I^{2}C Master Clock	Any Configuration Mode
29	PROG_FUNC5	SMB2_DAT USB to I^{2}C Slave Data	Configuration Mode 5 or 6
28	PROG_FUNC6	SMB2_CLK USB to I^{2}C Slave Clock	Configuration Mode 5 or 6

9.2.1 SLAVE INTERFACE

The USB4715 may be configured by an embedded SOC/MCU during both the start-up and runtime stages. Pull-up resistors must be detected by the hub at start-up in order for the I^{2}C/SMBus interface to become active. The interface command specification and configuration register set is described in full in *AN2651 - Configuration of Microchip USB47xx/USB49xx.*

Typically, a pull-up resistor of 1-10 kΩ is sufficient, depending on the interface speed and total capacitance on I^{2}C tree.

A pull-up voltage of 1.8V-3.3V is supported.

Note: If I^{2}C/SMBus pull-up resistors are detected by the USB4715 at start-up, the hub will wait indefinitely to be configured by the attached I^{2}C/SMBus master. For early prototyping, it may be necessary to physically remove the pull-up resistors until the I^{2}C/SMBus master is fully operational and able to properly configure the hub at start-up.

9.2.2 MASTER INTERFACE

The USB4715 has an I²C/SMBus master interface that can bridge USB commands to I²C/SMBus. Instructions for operating the I²C/SMBus master interface are contained in *AN2438 - USB-to-I2C Bridging with USB47xx/USB49xx*.

Typically, a pull-up resistor of 1-10 kΩ is sufficient, depending on the configured interface speed and total capacitance on the I²C tree.

A pull-up voltage of 1.8V to 3.3V is supported.

Ensure that all I²C/SMBus slave devices connected to the bus have unique addresses assigned.

Ensure that the USB4715 and all I²C/SMBus slave devices connected to the bus can support the target bus speed.

9.3 I²S Connections

One USB to I²S interface is available on USB4715. The interface is enabled when Configuration 1 is selected through the **CFG_STRAP** pin.

A compatible I²S codec is required. By default, the hub is configured to operate with an ADAU1961.

Use the compatibility guide listed in Table 9-4 to ensure that the selected codec is compatible with the options available on USB4715.

TABLE 9-3: I²S CODEC COMPATIBILITY GUIDE

Parameter	Supported Values
Sampling Frequency (fs)	8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, and 48 kHz
MCLK Frequency	1*fs to 1024*fs Since LRCLK is derived from MCLK source, MCLK signal should be an even integer multiple of fs.
Audio Sample Size	16 bit, 24 bit, 32 bit
I²S Audio Format	I²S mode, Left Justified mode, Right Justified mode
I²C Master Control Interface Frequency	100 kHz or 400 kHz
Audio Channels	Mono or Stereo
Interface Enable/Disable Options	Three options: • Audio OUT and Audio IN mode • Audio OUT Only mode (Speaker Interface) • Audio IN Only mode (Mic Interface)
Audio Jack Insertion Detection	Two options: • Audio Jack Insertion Detection Enabled (through HID interface) • Audio Jack Insertion Detection Disabled

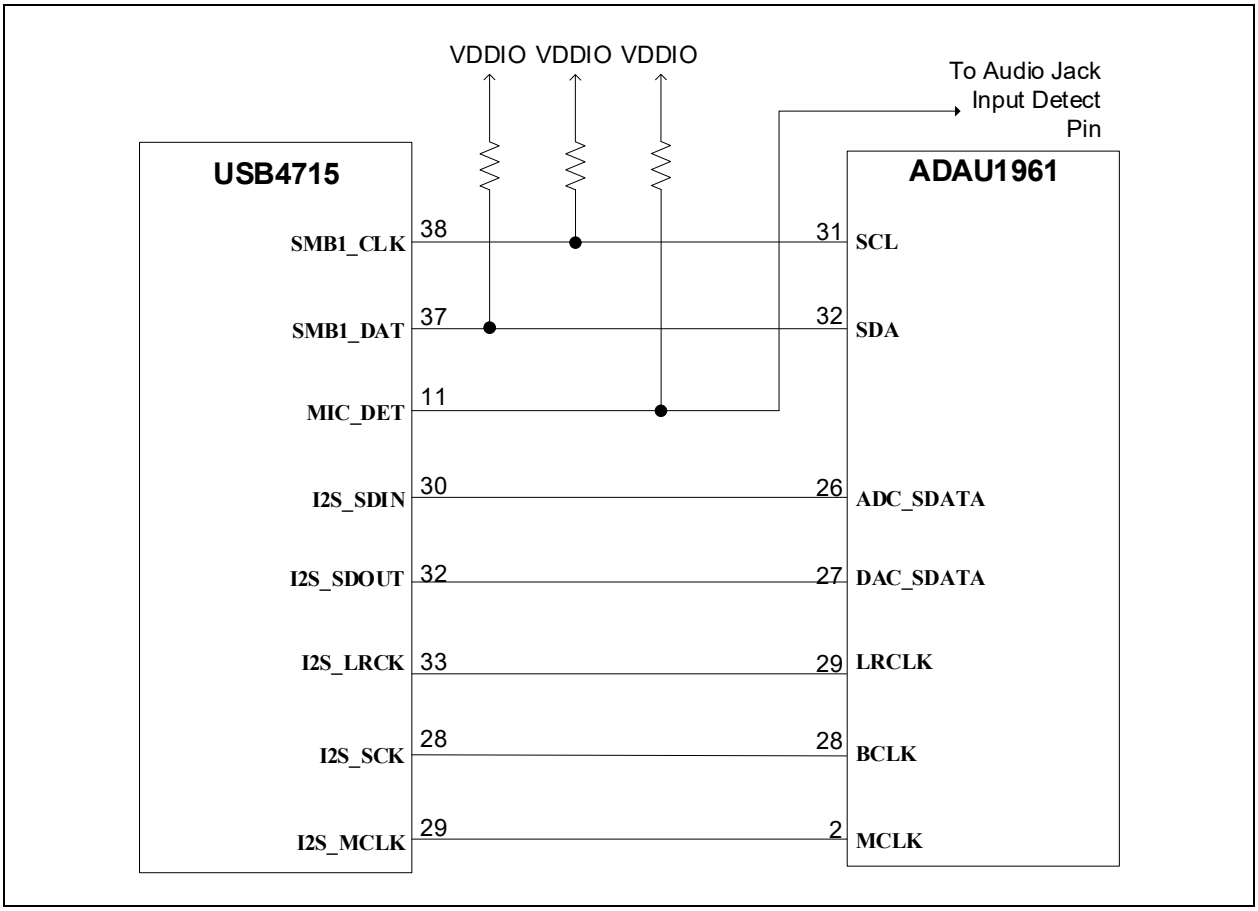
The I2S pins are described in Table 9-4.

TABLE 9-4: I2S PINS

Pin	PF Pin	Name	Role	Configuration Requirements
33	PROG_FUNC2	I2S_LRCK	I2S Left Right Clock	Configuration 1 or 6
32	PROG_FUNC3	I2S_SDOUT	I2S Serial Data Out	Configuration 1 or 6
30	PROG_FUNC4	I2S_SDIN	I2S Serial Data In	Configuration 1 or 6
29	PROG_FUNC5	I2S_MCLK	I2S Master Clock	Configuration 1 or 6
28	PROG_FUNC6	I2S_SCK	I2S Continuous Serial Clock	Configuration 1 or 6
11	PROG_FUNC7	MIC_DET	Optional - Microphone Detection Pin	Configuration 1 Only

If connecting to an ADAU1961, the I2S signals should be connected as shown in Figure 9-1. If using a different codec, consult the design guidelines provided by the manufacturer of the selected codec for implementation guidelines. These pins cannot be floated.

FIGURE 9-1: ADAU1961 I2S CODEC CONNECTIONS



9.4 UART Connections

One USB-to-UART interface is available on USB4715.

The interface is enabled when Configuration 2 is selected through the **CFG_STRAP** pin. The pins described in Table 9-5.

These signals may be attached directly to an embedded UART device, or connect to an RS232 connector. If routing the UART signals to an RS232 connector, a UART transceiver is recommended.

TABLE 9-5: UART PINS

Pin	PF Pin	Name	Role	Configuration Requirements
32	PROG_FUNC3	UART_RX	UART Receiver	Configuration 2, 4, or 5
33	PROG_FUNC2	UART_TX	UART Transmitter	Configuration 2, 4, or 5

9.5 FlexConnect

The FlexConnect feature allows the USB host role to be reassigned to any downstream port of the hub. For any Flex-Connect application, the key design options to consider are:

- How the FlexConnect will be controlled (initiated and terminated)
- How the **VBUS_DET** pin will be handled
- How their respective Type-C port roles will stay in sync with the state of FlexConnect if USB Type-C ports are present in the system

FlexConnect can be initiated via one of three methods:

- GPIO, which is selected and configured via OTP configuration
- A USB command to the Hub Feature Controller (HFC)
- Direct register manipulation via the I^2C/SMBus slave interface

This feature is highly implementation-specific and usually has numerous hardware design ramifications. If the FlexConnect feature is required in any specific application, it is recommended to reach out to a Microchip support representative early on in the design cycle to discuss the options available.

The FlexConnect feature and design guidelines are further explained in *AN4027 - USB58xx and USB59xx FlexConnect Operation.*

9.6 Non-Removable Port Settings

In a typical USB4715 application, downstream ports are routed to a user-accessible USB connector, and hence the downstream port should be configured as a removable port.

The USB4715 has a configuration strap option, **CFG_NON_REM**, which can be used to set the default configuration for port 1. This is located on pin 18. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. These are described in Table 9-6.

TABLE 9-6: CFG_NON_REM

Setting	Effect
200 kΩ pull-down to GND	All ports are removable.
200 kΩ pull-up to 3.3V	Port 1 is non-removable.
10 kΩ pull-down to GND	Ports 1 and 2 are non-removable.
10 kΩ pull-up to 3.3V	Ports 1, 2, and 3 are non-removable.
10Ω pull-down to GND	Ports 1, 2, 3, and 4 are non-removable.

The following guidelines can be used to determine which setting to use:

- If the port is routed to a user-accessible USB connector, it is *removable*.
- If the port is routed to a permanently-attached and embedded USB device on the same PCB, or non-user-accessible wiring or cable harness, it is *non-removable*.

Note: The removable/non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors that the USB host may use to understand if a port is a user-accessible port, or if the device is a permanently-attached device. Under standard operating conditions, the USB host may or may not modify its operation based upon this information. Certain USB compliance tests are impacted by this setting, so designs that must undergo USB compliance testing and certification must ensure the configuration settings are correct.

9.7 Self-Powered/Bus-Powered Settings

In a typical USB4715 application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the upstream USB connector's **VBUS** pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is *bus-powered*.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is *self-powered*.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely *self-powered* (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

Note: The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors that the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device that connects to a self-powered hub that declares it needs more than 100 mA will be prevented from operating by the USB host.

9.8 Battery Charging Settings

The USB4715 hub includes built-in Dedicated Charging Port (DCP), Charging Downstream Port (CDP), and vendor-specific (SE1) battery charging support.

The USB4715 has a configuration strap option, **CFG_BC_EN**, which can be used to set the default configuration for port 1. This is located on pin 17. The strap setting is sampled one time at start-up. A configuration strap option must be selected unless the hub firmware is being executed from an external SPI Flash device. The configuration strap options are described in Table 9-7.

TABLE 9-7: CFG_BC_EN

Setting	Effect	Additional Notes
200 kΩ pull-down to GND	All Ports - BC disabled	Battery Charging is not enabled. Select this option if configuration will be done in hub OTP, via I^2C/SMBus, or by external FW in SPI Flash. If SE1 charging is required, this strap option should be selected and SE1 must be enabled in hub OTP, via I^2C/SMBus, or by external FW in SPI Flash.
200 kΩ pull-up to 3.3V	Port 1 BC enabled	Battery Charging is on port 1. When no USB host is present (VBUS_DET = 0), downstream port 1 operates in Dedicated Charging Port (DCP) mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream port 1 operates in Charging Downstream Port (CDP) mode.

TABLE 9-7: CFG_BC_EN (CONTINUED)

Setting	Effect	Additional Notes
10 kΩ pull-down to GND	Ports 1 and 2 BC enabled	Battery Charging is on ports 1 and 2. When no USB host is present (VBUS_DET = 0), downstream ports 1 and 2 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1 and 2 operate in CDP mode.
10 kΩ pull-up to 3.3V	Ports 1, 2, and 3 BC enabled	Battery Charging is on ports 1, 2, and 3. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, and 3 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, and 3 operate in CDP mode.
10Ω pull-down to GND	Ports 1, 2, 3, and 4 BC enabled	Battery Charging is on ports 1, 2, 3 and 4. When no USB host is present (VBUS_DET = 0), downstream ports 1, 2, 3, and 4 operate in DCP mode. When a USB host is present (VBUS_DET = 1) and the USB host has commanded the hub to enable port power, downstream ports 1, 2, 3, and 4 operate in CDP mode.

Note: The vendor-specific SE1 charging mode uses the USB data lines to communicate charging capability. Hence, SE1 can only be active when no USB host is present. Additional vendor-specific charging modes exist for charging at elevated current levels when an active data connection is also present. This is handled by vendor-specific USB protocol between the USB host and the device. The USB4715 supports these vendor-specific protocol exchanges. These vendor-specific command specifications must be obtained from the respective device vendors.

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.2, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.3, "Ground"	Verify that the grounds are tied together.		
	Section 2.4, "USB-IF Compliant USB Connectors"	Verify that USB-IF compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure **VDDIO33** is in the range 3.0V to 3.6V and a 0.1 µF capacitor is on each pin. • Ensure **VDDPLLREF33** has a 0.1 µF capacitor to GND. It is also recommended to isolate this pin from the 3.3V supply rail behind a ferrite bead. • Ensure **VDD12CR** has a 0.1 µF capacitor and 1.0 µF capacitor in parallel to GND.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D- data lines.		
	Section 4.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Verify that the Upstream Port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.2, "Downstream Port VBUS and PRT_CTLx"	If the downstream ports are standard Type-A ports, verify that **PRT_CTLx** is properly connected to both the 'enable' pin of the downstream port power controller and the fault indicator output of the port power controller.		
	Section 5.3, "Downstream Port Type-C Support"	If the downstream ports are standard Type-C ports, verify that **PRT_CTLx** is properly connected to both the 'enable' pin of the Type-C port controller and the fault indicator output of the port power controller.		
	Section 5.4, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the GND pins and the SHIELD pins. It is recommended that an RC filter be placed in between the SHIELD pins and PCB ground.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "USB Connectors"	Section 6.1, "Crystal and External Clock Connection"	Confirm the crystal or clock is 25.000 MHz (±50 ppm). If a single-ended clock is used, ensure it is connected to **XTALI** while leaving **XTALO** floating. If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	Confirm that a 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V-3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the RESET_N line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the RESET_N signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC,MCU, or Reset supervisor device.		
Section 8.0, "External SPI Memory"	Section 8.1, "SPI Operation Summary"	Determine if a custom SPI FW image is required, and which mode of operation the selected SPI Flash device must support.		
	Section 8.2, "Compatible SPI Flash Devices"	Ensure the selected SPI Flash device is compatible with the hub.		
	Section 8.3, "SPI Connection Diagrams"	Verify that the SPI Flash device is connected according to the diagrams in Figure 8-1 or Figure 8-2. Follow Figure 8-3 if no SPI Flash device is connected in the design.		
Section 9.0, "Miscellaneous"	Section 9.1, "GPIOs"	Verify that any GPIO pins that will be used as GPIOs within the application are connected properly, and never exceed the voltage maximums/minimums, or overload the current source/sink maximums as defined by the hub data sheet.		
	Section 9.2, "I2C/SMBus Connections"	If the USB to I^2C/SMBus slave interface is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the I^2C/SMBus master are correct. Note that pull-up resistors are detected on the I^2C/SMBus slave interface, the USB hub will not enumerate to a USB host until it receives the special “Attach” command from the I^2C/SMBus master.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
	Section 9.2, "I2C/SMBus Connections"	If the USB-to-I^{2}C/SMBus Bridge feature is implemented, ensure that appropriate pull-up resistors are connected and that the connections to the I^{2}C/SMBus slave devices are correct. Verify that all slave devices have a different I^{2}C/SMBus address. Verify that the hub and all slave devices can support the targeted bus speed.		
	Section 9.3, "I2S Connections"	If using the USB-to-I^{2}S Bridge feature, ensure that Configuration 2 is selected via the **CFG_STRAP** pin, and ensure that the pin connections to the I^{2}S codec are correct. If using any codec other that the ADAU1961, ensure that it is compatible by referencing the compatibility guide in Table 9-3.		
	Section 9.4, "UART Connections"	If using the USB-to-UART Bridge feature, ensure that Configuration 3 is selected via the **CFG_STRAP** pin, and ensure that the pin connections to the UART device or transceiver are correct.		
	Section 9.5, "FlexConnect"	If using the FlexConnect feature, ensure that **VBUS_DET** and **PRTCLT1** pins are implemented per the recommendations.		
	Section 9.6, "Non-Removable Port Settings"	Verify that the **CFG_NON_REM** configuration strap is set per application requirements.		
	Section 9.7, "Self-Powered/Bus-Powered Settings"	Verify the application requirements for Self-Powered or Bus-Powered operation. If Self-Powered operation is required, then no additional configuration or circuitry is required. If Bus-Powered operation is required, then the hub must be configured via OTP or I^{2}C/SMBus.		
	Section 9.8, "Battery Charging Settings"	Verify that the **CFG_BC_EN** configuration strap is set per application requirements.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004210A (09-30-21)	Initial release	

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