AN3762

LAN9253 and LAN9254 Connectivity Options

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INTRODUCTION

The LAN9253 and LAN9254 EtherCAT devices provide a variety of interfaces to operate in Microcontroller Expansion mode. Both devices communicate with the microcontroller through an SRAM-like client interface. The simple yet highly functional host bus interface provides a glueless connection to most common 8-bit or 16-bit microprocessors and microcontrollers as well as 32-bit microprocessors with an 8-bit or 16-bit external bus. Alternatively, the device can be accessed via SPI/SQI while also providing up to 16 inputs or outputs for general purpose usage. An SPI/SQI™ (Quad SPI) client controller provides a low pin count synchronous client interface that facilitates communication between the device and a host system.

This application note shows the different interfaces to connect the LAN9253 and LAN9254 devices with an external MCU.

SECTIONS

This application note covers the following sections:

REFERENCES

The following documents should be referenced when using this application note:

- *LAN9253 2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs Data Sheet*
- *LAN9254 2/3-Port EtherCAT® Slave Controller with Integrated Ethernet PHYs and Demultiplexed HBI/32 DIGIOs Data Sheet*
- *LAN9253 Schematic Design Checklist*
- *LAN9254 Schematic Design Checklist*

LAN9253/LAN9254 CONNECTION INTERFACES

Below are the different connections for the LAN9253 and LAN9254 devices:

1. SPI Interface
2. SQI Interface
3. HBI Interface
   a) HBI Multiplexer Interface
   b) HBI Index mode
   c) HBI Demultiplexer Interface (LAN9254 only)
4. GPIO Interface
   a) 16-bit GPIO
   b) 32-bit GPIO (LAN9254 only)

REGISTER DEFINITIONS

PDI Interface Register Definition

This section details the registers required to configure the Process Data Interface (PDI) for the LAN9253 and LAN9254 devices. The bit definitions of this register depend on the selected PDI mode (Process Data Interface [PDI_SELECT]) field in the PDI Configuration register.

Offset = 0150h

Size = 8 bits

Table 1 shows the PDI Configuration register for the Digital I/O mode.

TABLE 1: PDI CONFIGURATION REGISTER: DIGITAL I/O MODE

Bits	Default	Description
7:6	00b	**Output Data Sample Selection** 00 = End of Frame 01 = RESERVED 10 = DC SYNC0 event 11 = DC SYNC1 event See **Note 1**.
5:4	00b	**Input Data Sample Selection** 00 = Start of frame 01 = Rising edge of LATCH_IN 10 = DC SYNC0 event 11 = DC SYNC1 event
3	0b	**Watchdog Behavior** 0 = Outputs are reset immediately after watchdog expires. 1 = Outputs are reset with next output event that follows watchdog expiration.
2	0b	**Unidirectional/Bidirectional Mode** 0 = Unidirectional mode: Input/output direction of pins are configured individually. 1 = Bidirectional mode: All I/O pins are bidirectional. See **Note 2**.

Note 1: If OUTVALID Mode = 1, output DATA is updated at Process Data Watchdog trigger event. (Output Data Sample Selection bit is ignored.)

2: Direction control must be set to input.

3: This overrides the Output Data Sample Selection bit.

TABLE 1: PDI CONFIGURATION REGISTER: DIGITAL I/O MODE (CONTINUED)

Bits	Default	Description
1	0b	**OUTVALID Mode** 0 = Output event signaling 1 = Process Data Watchdog trigger (WD_TRIG) signaling on OUTVALID. Output data is updated if watchdog is triggered. See **Note 3**.
0	0b	**OUTVALID Polarity** 0 = Active-high 1 = Active-low

Note 1: If OUTVALID Mode = 1, output DATA is updated at Process Data Watchdog trigger event. (Output Data Sample Selection bit is ignored.)

2: Direction control must be set to input.

3: This overrides the Output Data Sample Selection bit.

Table 2 shows the PDI Configuration register for the SPI mode.

TABLE 2: PDI CONFIGURATION REGISTER: SPI MODE

Bits	Default	Description
7:3	00000b	**RESERVED** See **Note 1**.
2	0b	**SPI AL Event Request and INT_STS Enable** 0 = SPI AL Event Request and INT_STS disabled. 1 = SPI AL Event Request and INT_STS enabled.
1	0b	**SPI WAIT_ACK Polarity** 0 = Active-low 1 = Active-high
0	0b	**SPI WAIT_ACK Buffer Type** 0 = Push-pull 1 = Open drain

Note 1: Set EEPROM value to 0.

Table 3 shows the PDI Configuration register for the Beckhoff SPI mode.

TABLE 3: PDI CONFIGURATION REGISTER: BECKHOFF SPI MODE

Bits	Default	Description
7:6	00b	**RESERVED** See **Note 1**.
5	0b	**Data Out Sample Mode** 0 = Normal sample (SPI_DO and SPI_DI are sampled at the same SPI_CLK edge.) 1 = Late sample (SPI_DO and SPI_DI are sampled at different SPI_CLK edges.)
4	0b	**SCS# Polarity** 0 = Active-low 1 = Active-high
3:2	00b	**RESERVED** See **Note 2**.
1:0	00b	**SPI Mode** 00 = SPI mode 0 01 = SPI mode 1 10 = SPI mode 2 11 = SPI mode 3

Note 1: Set EEPROM value to 0.
2: Set EEPROM value to 0.

Table 4 shows the PDI Configuration register for the HBI mode.

TABLE 4: PDI CONFIGURATION REGISTER: HBI MODE

Bits	Default	Description
7	0b	**HBI ALE Qualification** This configures the HBI interface to qualify the ALEHI and ALELO signals with the CS signal. 0 = Address input is latched with ALEHI and ALELO 1 = Address input is latched with ALEHI and ALELO only when CS is active.
6	0b	**HBI Read/Write Mode** This configures the HBI interface for separate read and write signals. or direction and enable signals. 0 = Read and write 1 = Direction and enable
5	0b	**HBI Chip Select Polarity** This configures the polarity of the HBI interface chip select signal. 0 = Active-low 1 = Active-high

TABLE 4: PDI CONFIGURATION REGISTER: HBI MODE (CONTINUED)

Bits	Default	Description
4	0b	**HBI Read, Read/Write Polarity** This configures the polarity of the HBI interface read signal. 0 = Active-low read 1 = Active-high read This configures the polarity of the HBI interface read/write signal. 0 = Read when 1, write when 0 (R/nW) 1 = Write when 1, read when 0 (W/nR)
3	0b	**HBI Write, Enable Polarity** This configures the polarity of the HBI interface write signal. 0 = Active-low write 1 = Active-high write This configures the polarity of the HBI interface read/write signal. 0 = Active-low enable 1 = Active-high enable
2	0b	**HBI ALE Polarity** This configures the polarity of the HBI interface ALEHI and ALELO signals. 0 = Active-low strobe (Address saved on rising edge) 1 = Active-high strobe (Address saved on falling edge)
1	0b	**HBI WAIT_ACK Polarity** 0 = Active low 1 = Active high
0	0b	**HBI WAIT_ACK Buffer Type** 0 = Push-pull 1 = Open drain

Extended PDI Interface Register Definition

This section details the registers required to configure the extended PDI interface for the LAN9253 and LAN9254 devices. The extended PDI Configuration registers provide additional information, such as I/O type and I/O's direction, to the EtherCAT host. The bit definitions of this register are dependent on the selected PDI mode (Process Data Interface [PDI_SELECT]) field in the PDI Control register.

Offset = 0152h-0153h

Size = 16 bits

Table 5 and Table 6 show the extended PDI Configuration register for the Digital I/O mode for LAN9253 and LAN9254, respectively.

TABLE 5: EXTENDED PDI CONFIGURATION REGISTER: DIGITAL I/O MODE (LAN9253 ONLY)

Bits	Default	Description
7	0b	**I/O[15:14] Direction** 0 = Input 1 = Output See **Note 1**.
6	0b	**I/O[13:12] Direction** 0 = Input 1 = Output See **Note 1**.
5	0b	**I/O[11:10] Direction** 0 = Input 1 = Output See **Note 1**.
4	0b	**I/O[9:8] Direction** 0 = Input 1 = Output See **Note 1**.
3	0b	**I/O[7:6] Direction** 0 = Input 1 = Output See **Note 1**.
2	0b	**I/O[5:4]** Direction 0 = Input 1 = Output See **Note 1**.
1	0b	**I/O[3:2] Direction** 0 = Input 1 = Output See **Note 1**.
0	0b	**I/O[1:0] Direction** 0 = Input 1 = Output See **Note 1**.

Note 1: This must be cleared to 0 during Bidirectional mode.

TABLE 6: EXTENDED PDI CONFIGURATION REGISTER: DIGITAL I/O MODE (LAN9254 ONLY)

Bits	Default	Description
15	0b	**I/O[31:30] Direction** 0 = Input 1 = Output See **Note 1**.
14	0b	**I/O[29:28] Direction** 0 = Input 1 = Output See **Note 1**.
13	0b	**I/O[27:26] Direction** 0 = Input 1 = Output See **Note 1**.
12	0b	**I/O[25:24] Direction** 0 = Input 1 = Output See **Note 1**.
11	0b	**I/O[23:22] Direction** 0 = Input 1 = Output See **Note 1**.
10	0b	**I/O[21:20] Direction** 0 = Input 1 = Output See **Note 1**.
9	0b	**I/O[19:18] Direction** 0 = Input 1 = Output See **Note 1**.
8	0b	**I/O[17:16] Direction** 0 = Input 1 = Output See **Note 1**.
7	0b	**I/O[15:14] Direction** 0 = Input 1 = Output See **Note 1**.
6	0b	**I/O[13:12] Direction 0:** Input 0 = Input 1 = Output See **Note 1**.

Note 1: This must be cleared to 0 during Bidirectional mode.

TABLE 6: EXTENDED PDI CONFIGURATION REGISTER: DIGITAL I/O MODE (LAN9254 ONLY)

Bits	Default	Description
5	0b	**I/O[11:10] Direction** 0 = Input 1 = Output See **Note 1**.
4	0b	**I/O[9:8] Direction** 0 = Input 1 = Output See **Note 1**.
3	0b	**I/O[7:6] Direction** 0 = Input 1 = Output See **Note 1**.
2	0b	**I/O[5:4] Direction** 0 = Input 1 = Output See **Note 1**.
1	0b	**I/O[3:2] Direction** 0 = Input 1 = Output See **Note 1**.
0	0b	**I/O[1:0] Direction** 0 = Input 1 = Output See **Note 1**.

Note 1: This must be cleared to 0 during Bidirectional mode.

Table 7 shows the extended PDI Configuration register for the SPI mode.

TABLE 7: EXTENDED PDI CONFIGURATION REGISTER: SPI MODE

Bits	Default	Description
15	0b	**I/O[15:14] Buffer Type** 0 = Push-pull 1 = Open drain
14	0b	**I/O[13:12] Buffer Type** 0 = Push-pull 1 = Open drain
13	0b	**I/O[11:10] Buffer Type** 0 = Push-pull 1 = Open drain
12	0b	**I/O[9:8] Buffer Type** 0 = Push-pull 1 = Open drain
11	0b	**I/O[7:6] Buffer Type** 0 = Push-pull 1 = Open drain
10	0b	**I/O[5:4] Buffer Type** 0 = Push-pull 1 = Open drain
9	0b	**I/O[3:2] Buffer Type** 0 = Push-pull 1 = Open drain
8	0b	**I/O[1:0] Buffer Type** 0 = Push-pull 1 = Open drain
7	0b	**I/O[15:14] Direction** 0 = Input 1 = Output
6	0b	**I/O[13:12] Direction** 0 = Input 1 = Output
5	0b	**I/O[11:10] Direction** 0 = Input 1 = Output
4	0b	**I/O[9:8] Direction** 0 = Input 1 = Output

Note 1: This must be cleared to 0 during Bidirectional mode.

TABLE 7: EXTENDED PDI CONFIGURATION REGISTER: SPI MODE (CONTINUED)

Bits	Default	Description
3	0b	**I/O[7:6] Direction** 0 = Input 1 = Output
2	0b	**I/O[5:4] Direction** 0 = Input 1 = Output
1	0b	**I/O[3:2] Direction** 0 = Input 1 = Output
0	0b	**I/O[1:0] Direction** 0 = Input 1 = Output See **Note 1**.

Note 1: This must be cleared to 0 during Bidirectional mode.

Table 8 shows the extended PDI Configuration register for the HBI mode.

TABLE 8: EXTENDED PDI CONFIGURATION REGISTER: HBI MODE

Bits	Default	Description
15:13	000h	**RESERVED** 0 = Push-pull 1 = Open drain
2	0b	**HBI BE1/BE0 Polarity** 0 = BE1/BE0 pins active-low 1 = BE1/BE0 pins active-high See **Note 1**.
1	0b	**Perform Internal Write** 0 = Following host write cycle (posted) 1 = Following host read cycle (non-posted)
0	0b	**Read WAIT_ACK Removal Delay** 0 = Normal read WAIT_ACK output 1 = Delayed read WAOT_ACK output

Note 1: Multiplexed mode only

LAN9253/LAN9254 PHYSICAL CONNECTIONS

This section shows the physical connections for SPI, SQI, and different HBI interfaces. Refer to Figure 1 to Figure 8.

FIGURE 1: SPI INTERFACE

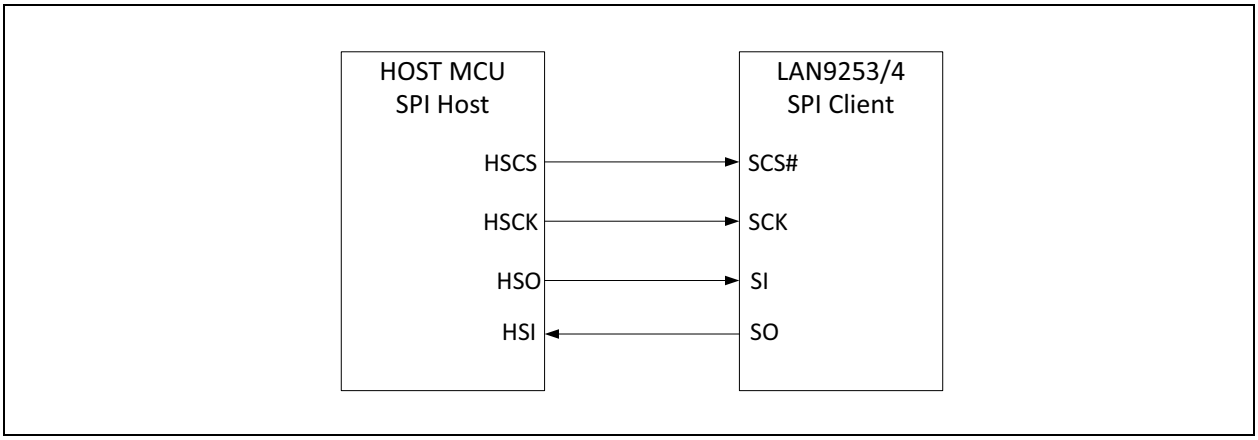


FIGURE 2: SQI™ INTERFACE

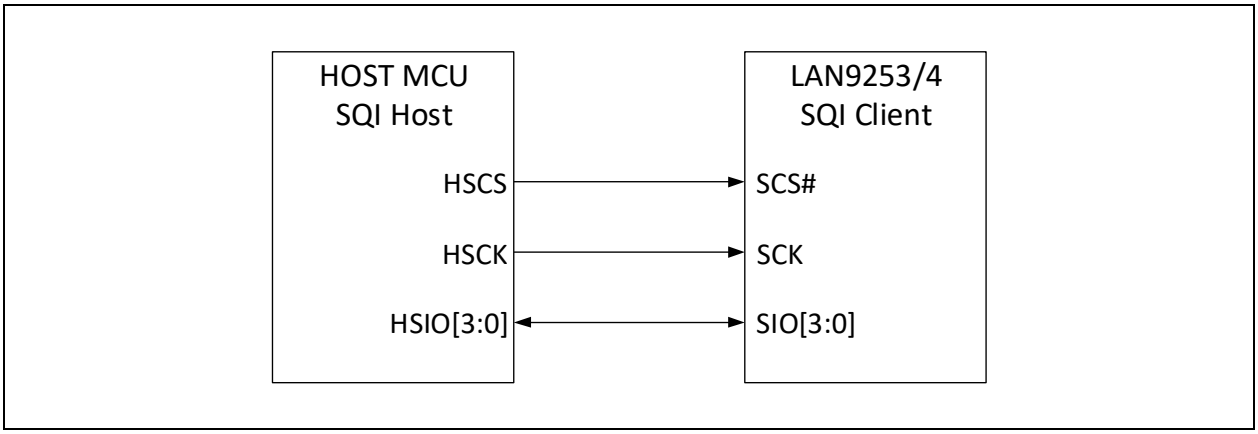


FIGURE 3: INDEXED ADDRESS READ/WRITE FOR 8-BIT AND 16-BIT HOST BUS

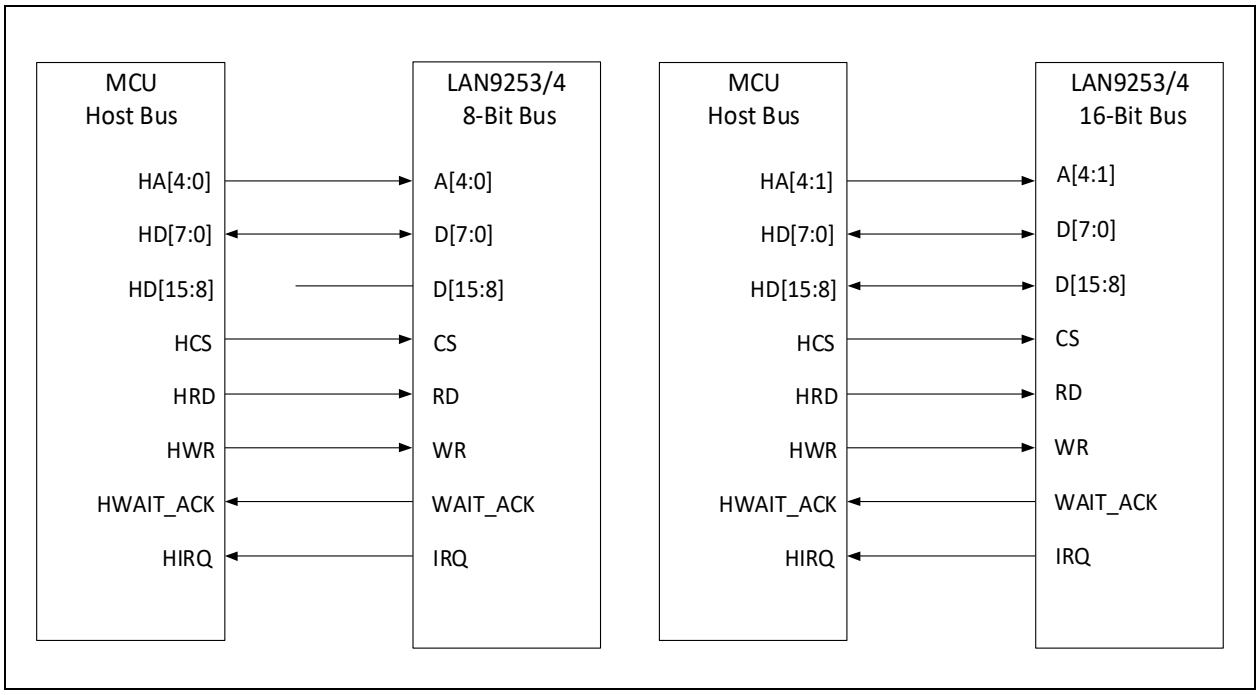


FIGURE 4: MULTIPLEXED ADDRESS WITH SINGLE-PHASE LATCHING FOR 8-BIT AND 16-BIT HOST BUS

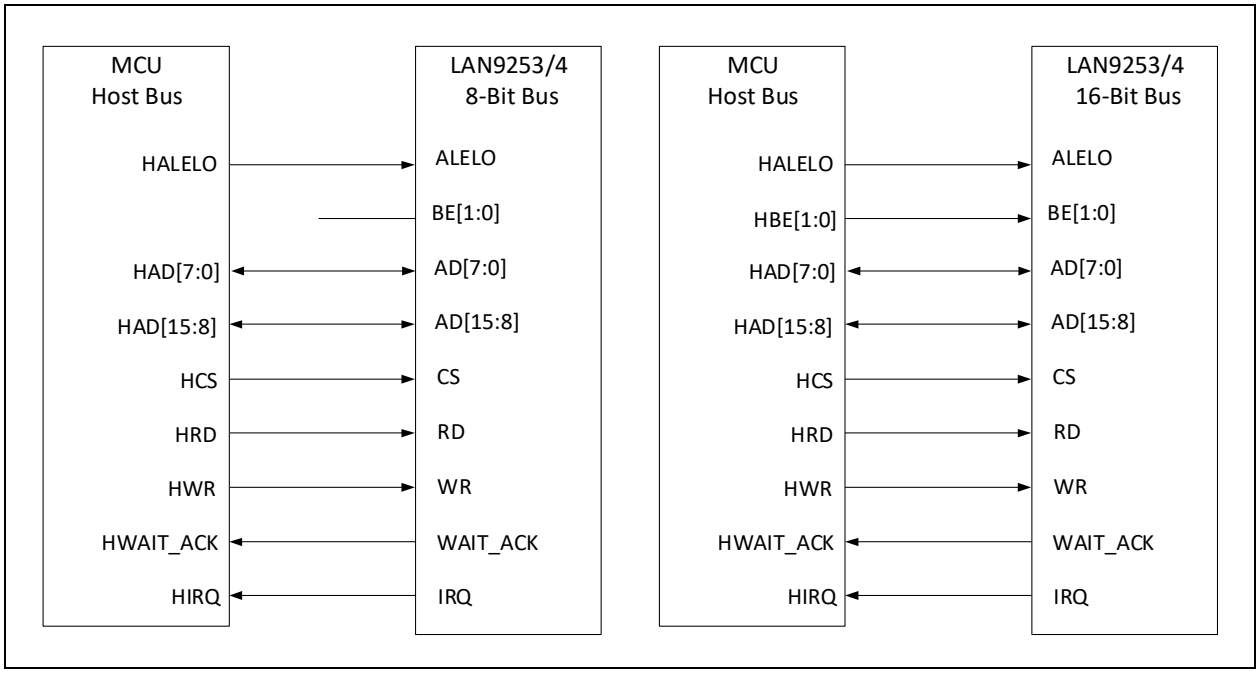


FIGURE 5: MULTIPLEXED ADDRESS WITH DUAL-PHASE LATCHING FOR 8-BIT AND 16-BIT HOST BUS

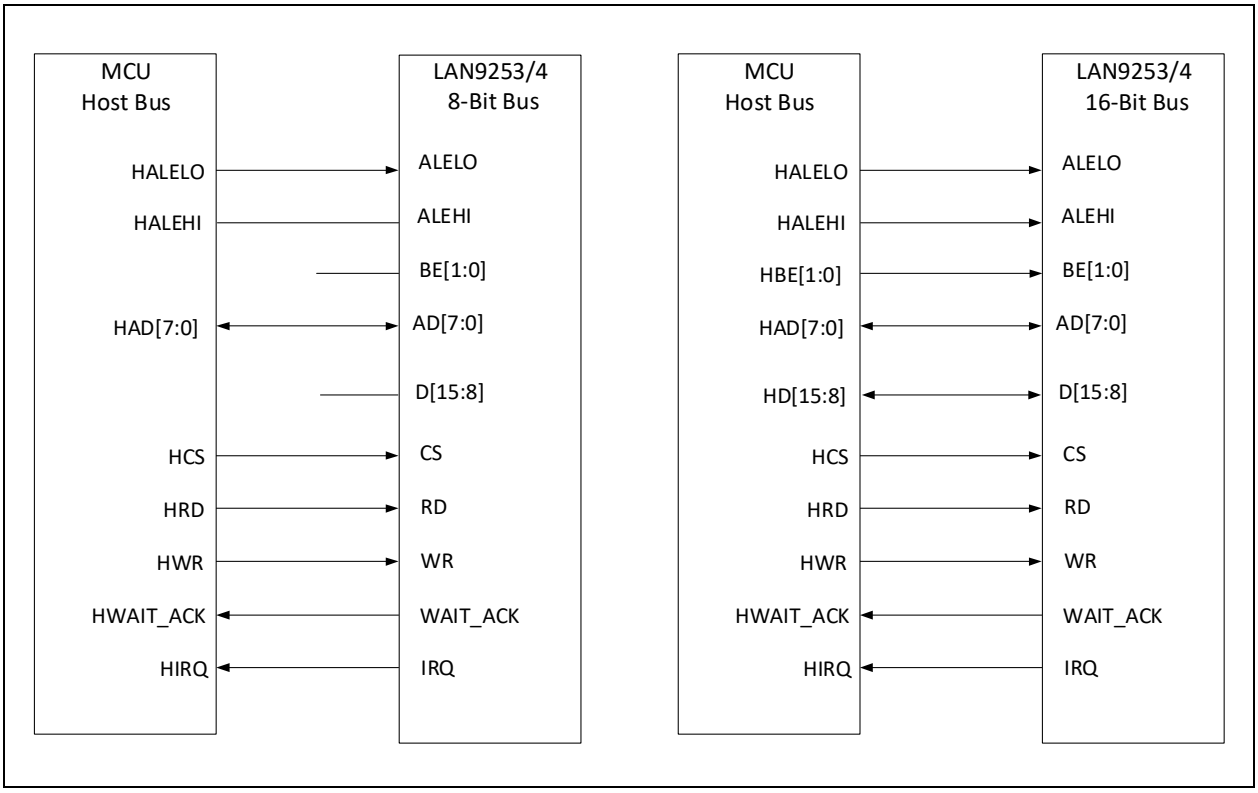


FIGURE 6: MULTIPLEXED ADDRESS RD_WR/ENB CONTROL MODE FOR 8-BIT AND 16-BIT HOST BUS

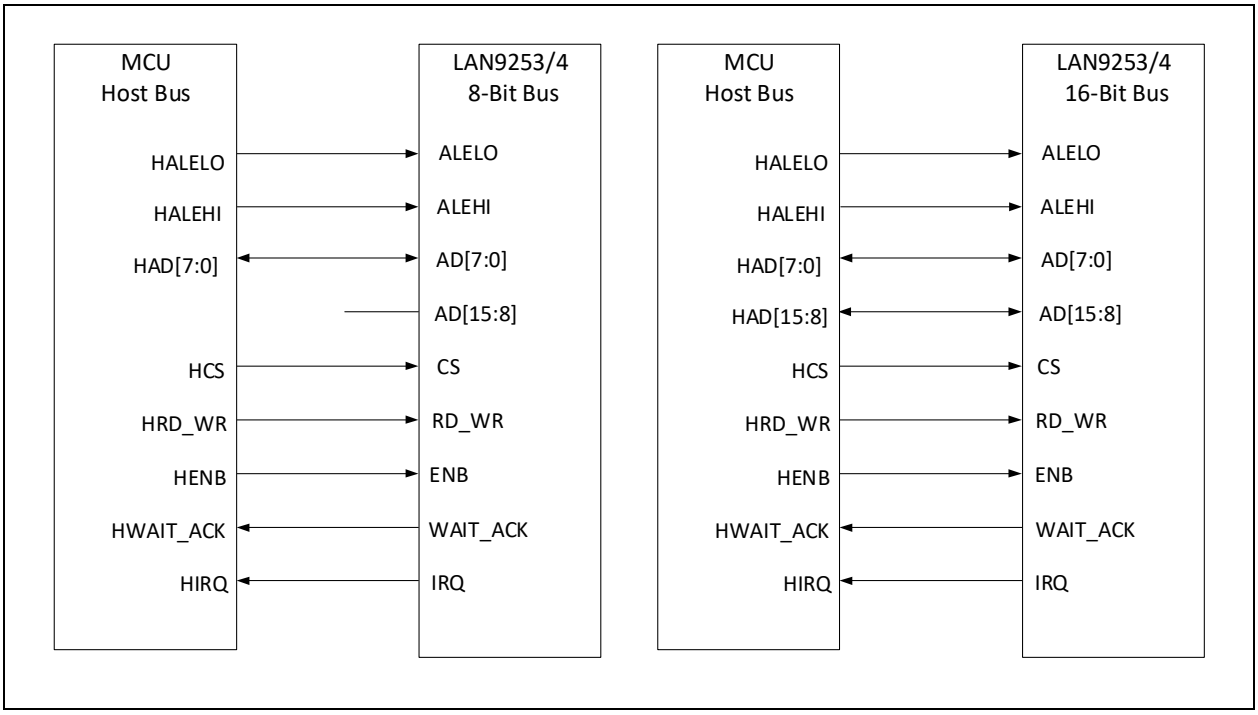


FIGURE 7: DEMULTIPLEXED ADDRESSING 8-BIT AND 16-BIT HOST BUS INTERFACE

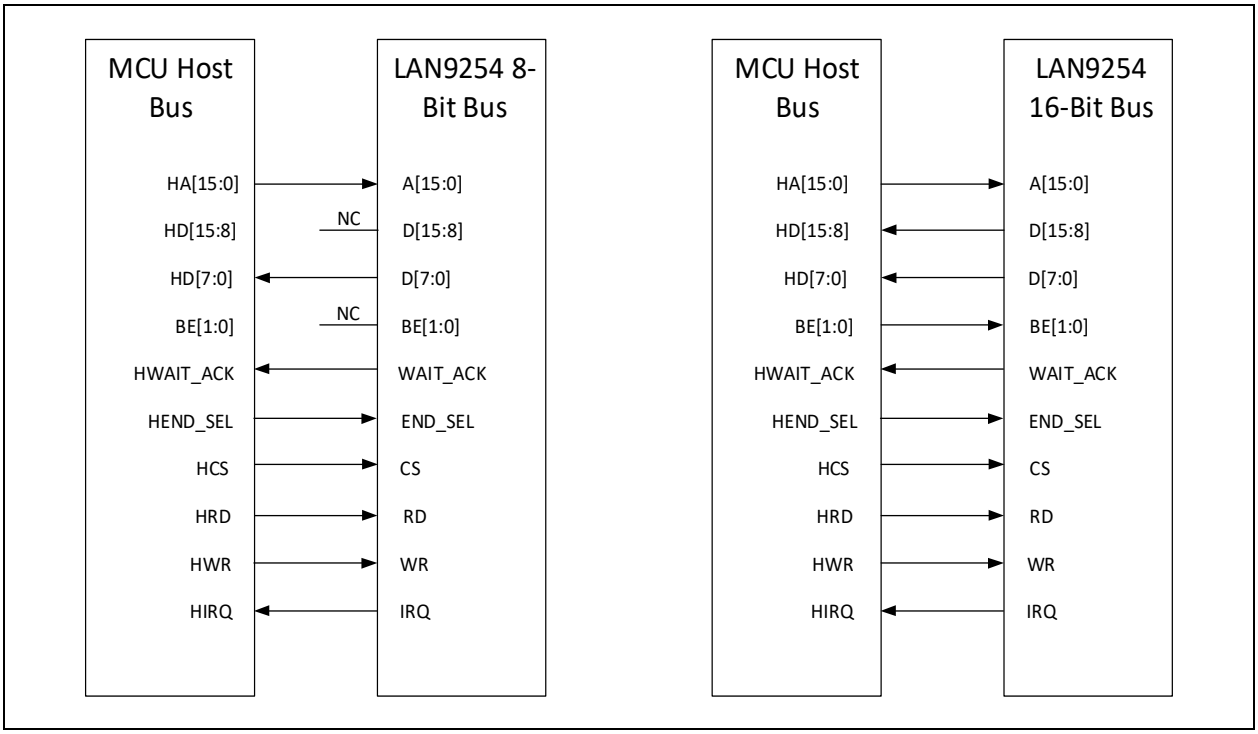
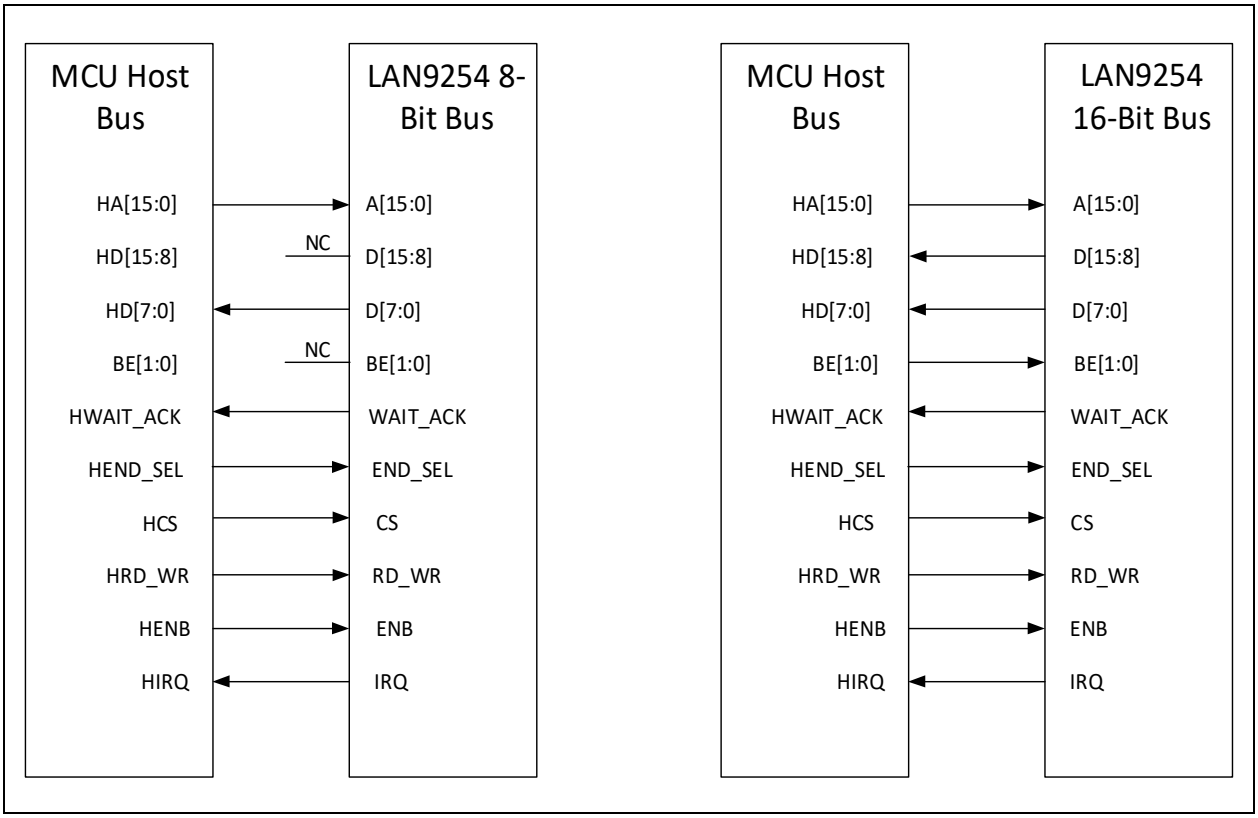


FIGURE 8: DEMULTIPLEXED ADDRESS RD_WR/ENB CONTROL MODE FOR 8-BIT AND 16-BIT HOST BUS INTERFACE



SUMMARY

In conclusion, the different PDI interfaces for LAN9253 and LAN9254 devices have been described in this application note. The SPI, SQI, and HBI interfaces on the LAN9253 and LAN9254 devices are extremely easy to configure and use with any external MCUs. This application note has also covered the connection arrangements for different interfaces and the configuration register values. Lastly, this document has featured the Digital I/O mode where the LAN9253 or LAN9254 devices may not require a connection to an external MCU.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003762A (12-15-20)	Initial release	

Note: The EtherCAT standard uses the terminology "slave." The equivalent Microchip terminology used in this document is "client."

NOTES:

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