LAN9513

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN9513. These checklist items should be followed when utilizing the LAN9513 in a new design. A summary of these items is provided in Section 8.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet Signals"
- Section 5.0, "USB Signals"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The LAN9513 implementer should have the following document(s) on hand:

- *LAN9513 Data Sheet*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The LAN9513 has one exposed pad (**VSS**) on bottom of package, which must be connected directly to a solid, contiguous digital ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connectors

- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER

3.1 3.3V Supply

- **VDD33IO** (pins 19, 27, 33, 39, and 46) require a connection to +3.3V. Each pin should have one 0.1 µF (or smaller) decoupling capacitor. The capacitor size should be SMD_0603 or smaller.
- **VDD33A** (pins 5, 10, 49, 51, 54, 57, and 64) require a connection to +3.3V through a ferrite bead. Each pin should have one 0.1 µF (or smaller) decoupling capacitor. The capacitor size should be SMD_0603 or smaller.

3.2 VDD18CORE

- **VDD18CORE** (pins 15 and 38) are used to provide bypass for the internal +1.8V core regulator. Each pin requires a 0.1 µF bypass capacitor located as close as possible to the pin without using vias. In addition, a 4.7 µF ceramic capacitor with <2.0 Ohm ESR is required on pin 38. Other values, tolerances, and characteristics are not recommended.

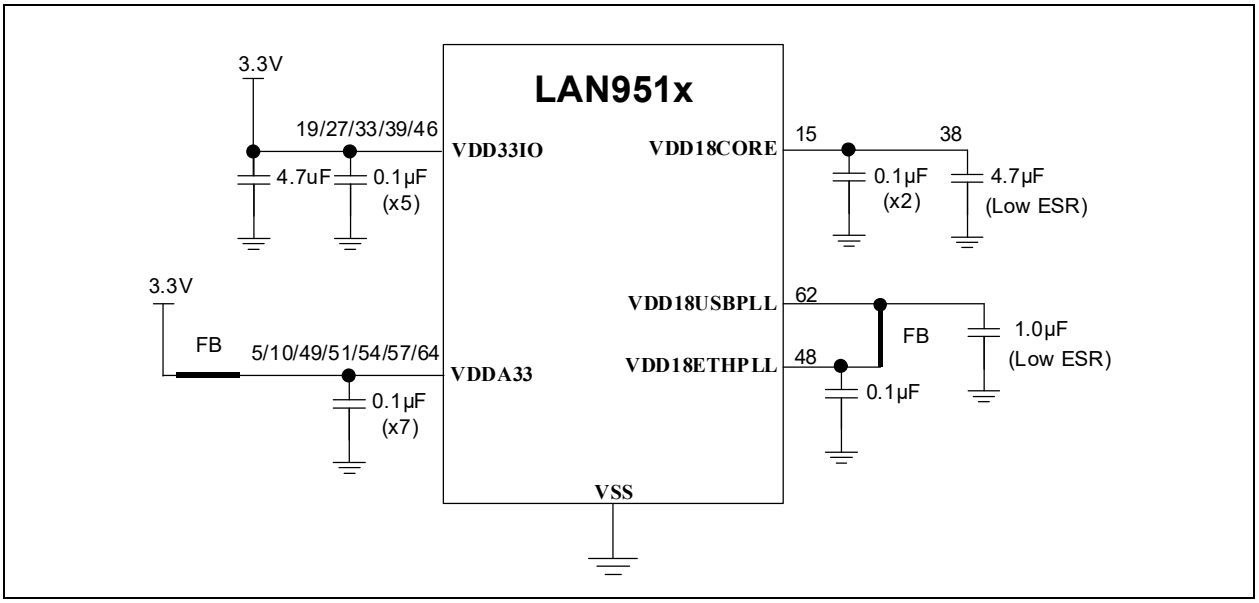
Note: Do not connect **VDD18CORE** to either **VDD18USBPLL** or **VDD18ETHPLL**.

3.3 VDD18USBPLL and VDD18ETHPLL

- **VDD18ETHPLL** (pin 48) supplies power to the core PLL. This pin must be connected to **VDD18USBPLL** through a ferrite bead.
- The **VDD18USBPLL** (pin 62) and **VDD18ETHPLL** (pin 48) should also have a 1.0 µF bypass capacitor in size of SMD_0603 or smaller. The capacitor must have an ESR of no more than 2.0.

Refer to Figure 3-1 for power and ground connections.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



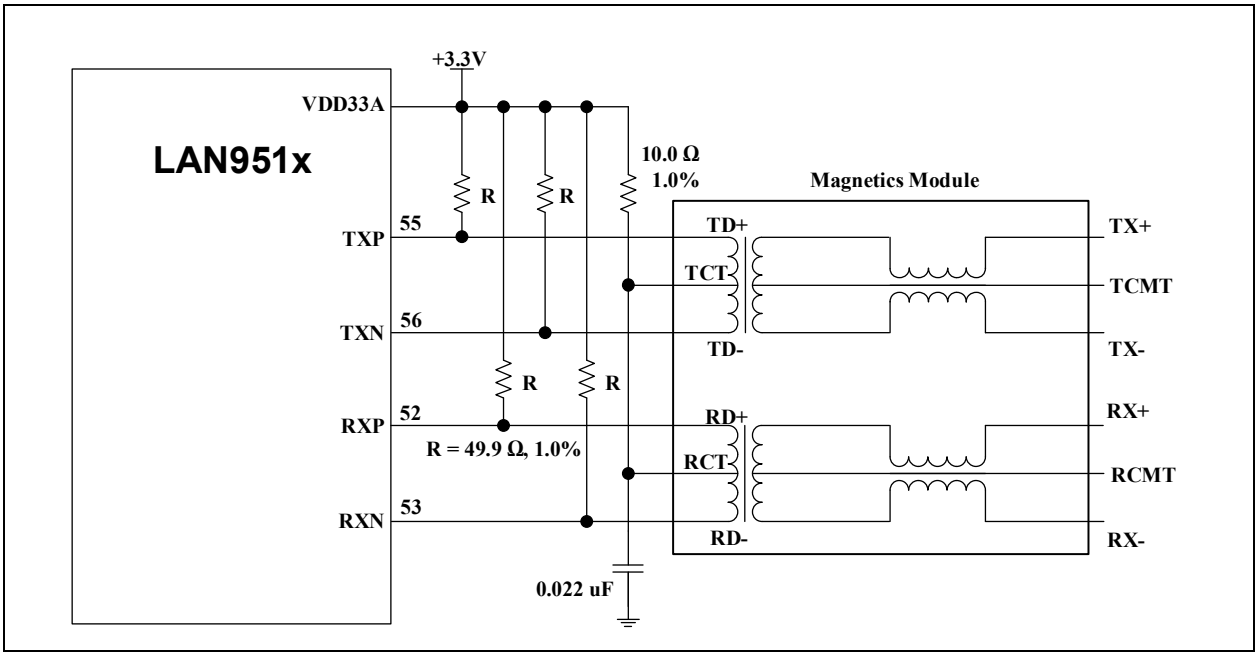
4.0 ETHERNET SIGNALS

4.1 Ethernet PHY Interface

- **TXP** (pin 55) is the transmit twisted pair output positive connection from the internal PHY. It requires a 49.9 ohm, 1.0% pull-up resistor to **VDD33A**. This pin also connects to the transmit channel of the magnetics.
- **TXN** (pin 56) is the transmit twisted pair output negative connection from the internal PHY. It requires a 49.9 ohm, 1.0% pull-up resistor to **VDD33A**. This pin also connects to the transmit channel of the magnetics.
- **RXP** (pin 52) is the receive twisted pair input positive connection from the internal PHY. It requires a 49.9 ohm, 1.0% pull-up resistor to **VDD33A**. This pin also connects to the receive channel of the magnetics.
- **RXN** (pin 53) is the receive twisted pair input negative connection from the internal PHY. It requires a 49.9 ohm, 1.0% pull-up resistor to **VDD33A**. This pin also connects to the receive channel of the magnetics.

For transmit and receive channel connection details, refer to Figure 4-1.

FIGURE 4-1: ETHERNET CHANNEL CONNECTIONS AND TERMINATIONS



4.2 Magnetics Connection

- The center tap connection on the LAN9513 side for the transmit channel must be connected to **VDD33A** through a 10.0 ohm series resistor with a tolerance of 1.0%. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics. In addition, a 0.022 µF capacitor is required from the receive channel center tap of the magnetics to ground.
- The center tap connection on the cable side (RJ45 side) for the transmit and receive channels should be terminated with a 75 ohm resistor through a shared 1000 pF, 2 kV capacitor to chassis ground.
- When in the PHP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the Microchip application note AN8.13 “Suggested Magnetics” for proper magnetics.

4.3 RJ45 Connector

- Unused pairs 4-5 and 7-8 of the RJ45 connector are tied together and connected to the same 2 kV capacitor through a 75Ω resistor. This provides direct termination for potential common mode noise on the unused pairs.

5.0 USB SIGNALS

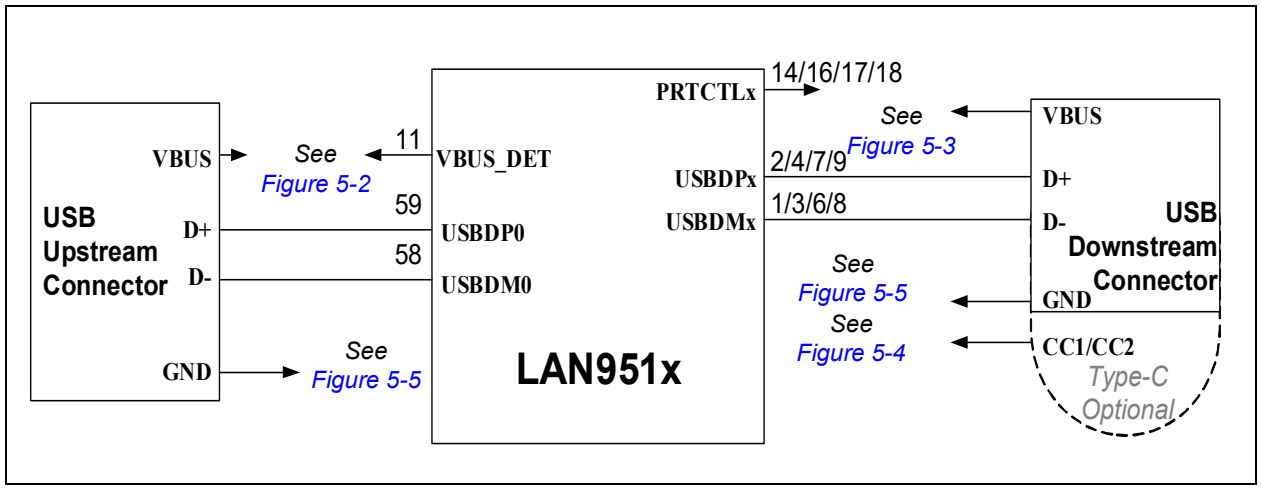
5.1 USB PHY Interface

- **USBDP0** (pin 59) is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D+/DP pin of a USB connector.
- **USBDM0** (pin 58) is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. This pin can connect directly to the D–/DM pin of a USB connector.
- **USBDP2/USBDP3/USBDP4** (pins 2/4/7): These pins are the positive (+) signal of the downstream ports USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. These pins can connect directly to the D+/DP pins of USB connectors.
- **USBDM2/USBDM3/USBDM4** (pins 1/3/6): These pins are the negative (–) signal of the downstream ports USB2.0 differential pair. All necessary USB terminations and resistors are included internal the IC. These pins can connect directly to the D–/DM pin of USB connectors.

Note:	The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I^2C configuration registers.

For transmit and receive channel connections details, refer to Figure 5-1.

FIGURE 5-1: USB DATA SIGNAL CONNECTIONS



5.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

- If any downstream of the LAN9513 is unused, it should be disabled through hub configuration (I^2C), or through a port disable strap option.

5.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These are generally grouped into three categories:

1. TVS protection diodes
   - ESD protection for IEC-61000-4-2 system level tests
2. Application-targeted protection ICs or galvanic isolation devices
   - DC overvoltage protection for short to battery protection
3. Common-mode chokes
   - For EMI reduction

The LAN9513 can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have as well as to select components accordingly and follow the implementation guidelines from the manufacturer of these devices. You may also use the following general guidelines for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Based on the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- These devices should be placed as close to the USB connector as possible.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low impedance path to a large ground plane.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note:	Microchip PHYBoost configuration options are available for compensating the negative effects of these devices. This feature may help to overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests, on physical hardware.

5.3 USB Connectors

5.3.1 UPSTREAM PORT VBUS AND VBUS_DET

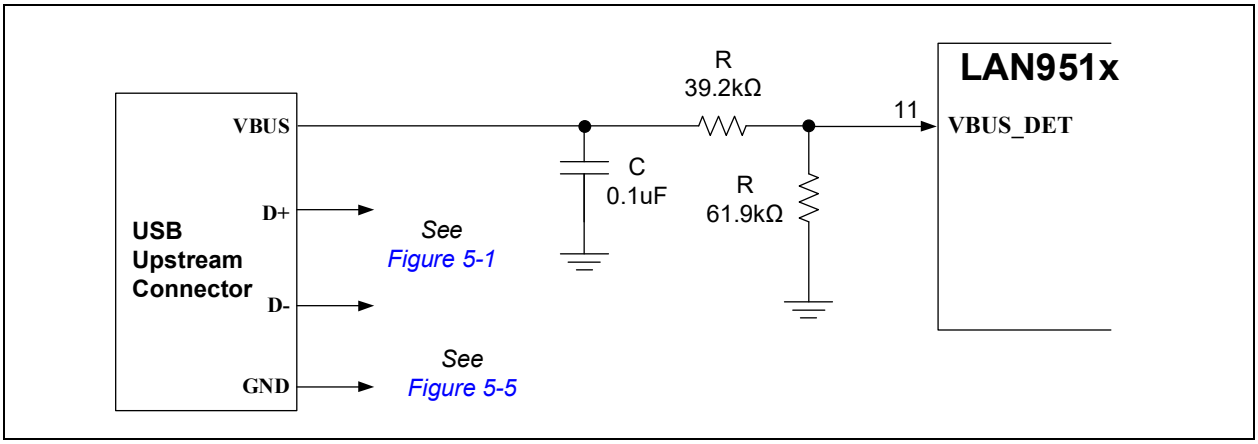
The upstream port VBUS line must have no more than 10 µF of the total capacitance connected.

The **VBUS_DET** pin is used to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft Reset and reconnection of the LAN9513. It is permissible to tie **VBUS_DET** directly to 3.3V. However, this is not recommended as the ability to force a Reset of the hub from the USB host VBUS toggling is lost.

The recommended implementation is shown in Figure 5-2. Note that the precise resistor values are not critical, and alternate values may be selected as long as:

- The impedance from the **VBUS** pin of the USB connector to the **VBUS_DET** pin is sufficiently high-impedance to minimize pin leakage when **VBUS** is present before the Hub IC is powered on.
- A sufficient voltage level is present on the **VBUS_DET** for the full range of VBUS (4.5V to 5.5V).

FIGURE 5-2: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS

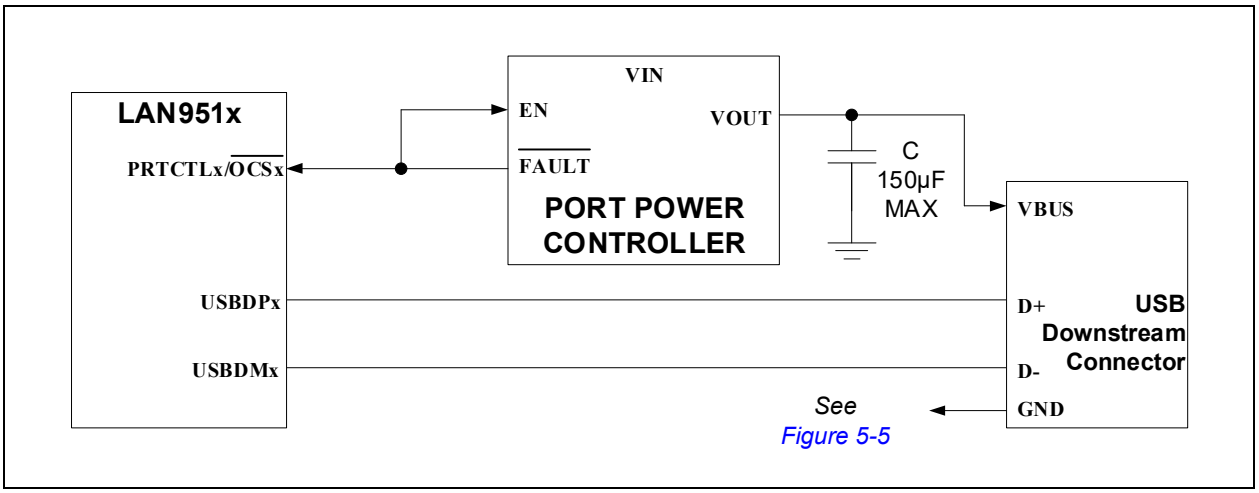


5.3.2 DOWNSTREAM PORT POWER CONTROL AND OVERCURRENT SENSING

The LAN9513 has a single port power control and overcurrent sense signal for each downstream port. When disabling port power, the driver will actively drive a ‘0’. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled and the pull-up resistor is enabled, creating an open-drain output. If there is an overcurrent situation, the USB Power Controller will assert the open-drain OCS signal. The Schmitt trigger input will recognize this situation as a low. The open-drain output does not interfere.

A typical VBUS port power control implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM VBUS AND PRTCTL/OCS CONNECTIONS



Note: The implementation, as shown in Figure 5-3, assumes that the port power controller has an active-high enable input, and an active-low, open-drain style FAULT indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3.3 DOWNSTREAM PORT TYPE-C SUPPORT

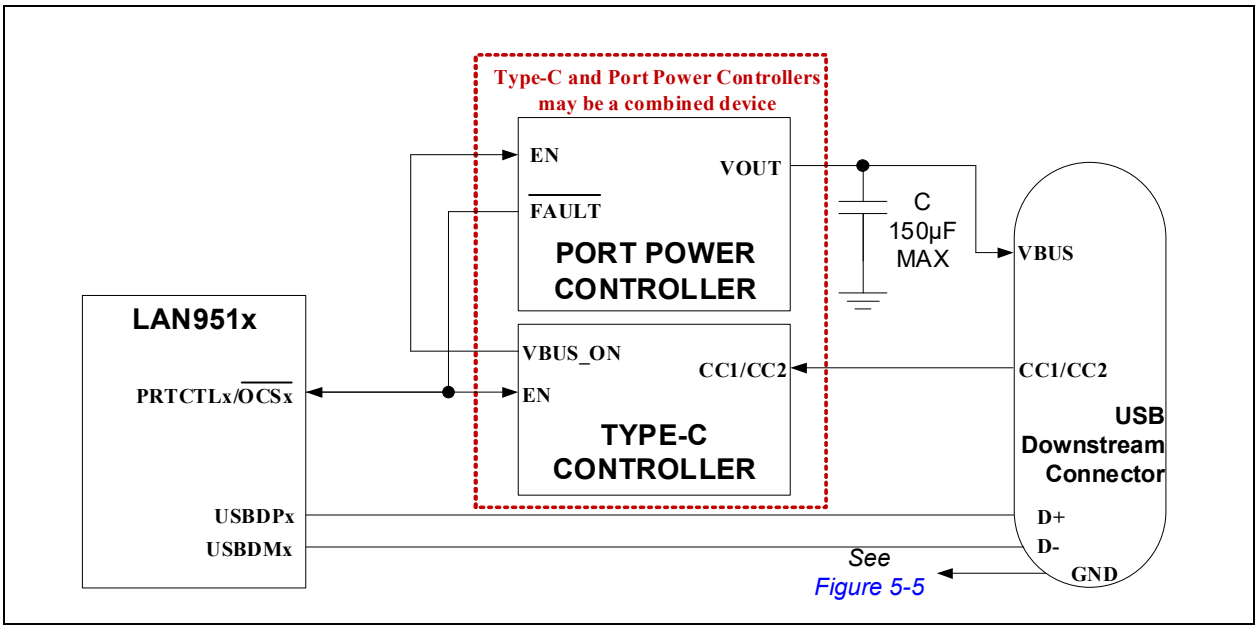
The LAN9513 may be used with Type-C as the downstream port. This requires a Type-C port controller or combined port power controller and Type-C port controller. The LAN9513 simply controls the Type-C port controller in the same way it would control a standard Type-A port power controller. This does not require any kind of Type-C port status information from the Type-C port controller. The **PRTCTLx/OCSx** signal should be connected to an enable pin on the Type-C controller and the FAULT indicator output of the port power controller.

If the Type-C controller and the port power controller are separate devices, the Type-C controller must control the enable pin of the port power controller. The **PRTCTLx** should not directly control the enable signal of the port power controller.

A Type-C controller may be configured to signal a 500 mA, 1.5A, or 3.0A port power capability. The selected port power controller should be sized accordingly.

A typical implementation is shown in Figure 5-4.

FIGURE 5-4: DOWNSTREAM VBUS AND PRTCTLX CONNECTIONS WITH A TYPE-C PORT



Note:	The implementation, as shown in Figure 5-4, assumes that the Type-C controller has an active-high enable input, and the port power controller has an active-low, open-drain style FAULT indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller and/or port power controller has different I/O characteristics.

5.3.4 GND AND SHIELD RECOMMENDATIONS

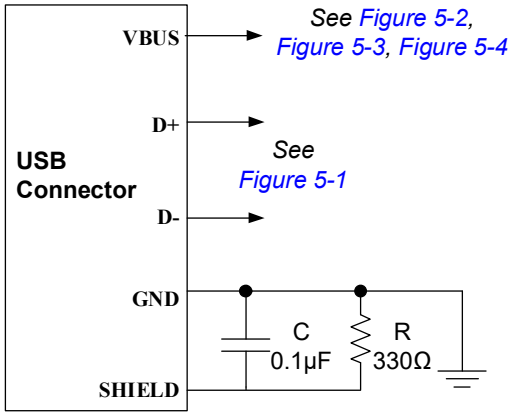
The **GND** pins of the USB connector must be connected to a large ground plane of PCB with a low-impedance path directly.

The SHIELD pins of the USB connector may be connected in one of two ways:

- (Recommended) Connect to **GND** through a resistor and capacitor in parallel. An RC filter can help decouple and minimize EMI between a PCB and a USB cable.
- Directly to the **GND** plane.

The recommended implementation is shown in Figure 5-5.

FIGURE 5-5: RECOMMENDED USB CONNECTOR GND AND SHIELD CONNECTIONS



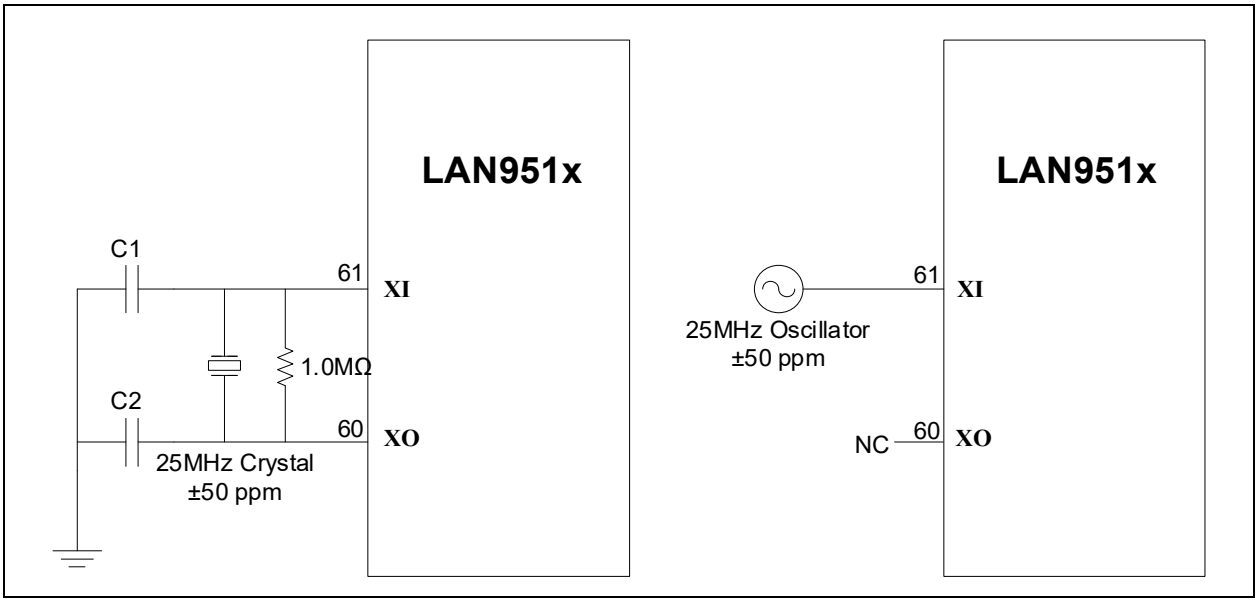
6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

The LAN9513 can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (±50 ppm) input. If the single-ended clock oscillator method is implemented, **XO** should be left unconnected and **XI** should be driven with a nominal 0V to 3.3V clock signal. See Figure 6-1.

- **XI** (pin 61) is the clock circuit input for the LAN9513. This pin requires a 15 pF to 33 pF capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 60) is the clock circuit output for the LAN9513. This pin requires a matching 15 pF to 33 pF capacitor to ground and the other side of the crystal.
- The crystal loading capacitor values are system dependent, based on the total C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:
  - $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$
  - Where: C_L is the spec from the crystal datasheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$.
  - Note that C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, within the 1 pF to 2 pF range, and then verified by physical experiments in the laboratory if PCB simulation tools are not available.
- For proper operation, an additional 1.0 MΩ resistor is required to the crystal circuit. This resistor is placed in parallel with the crystal.
- Alternately, a 25 MHz clock oscillator may be used to provide the clock source for the LAN9513. When using a single-ended clock source, **XO** (pin 60) should be left floating as a No Connect (NC).

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



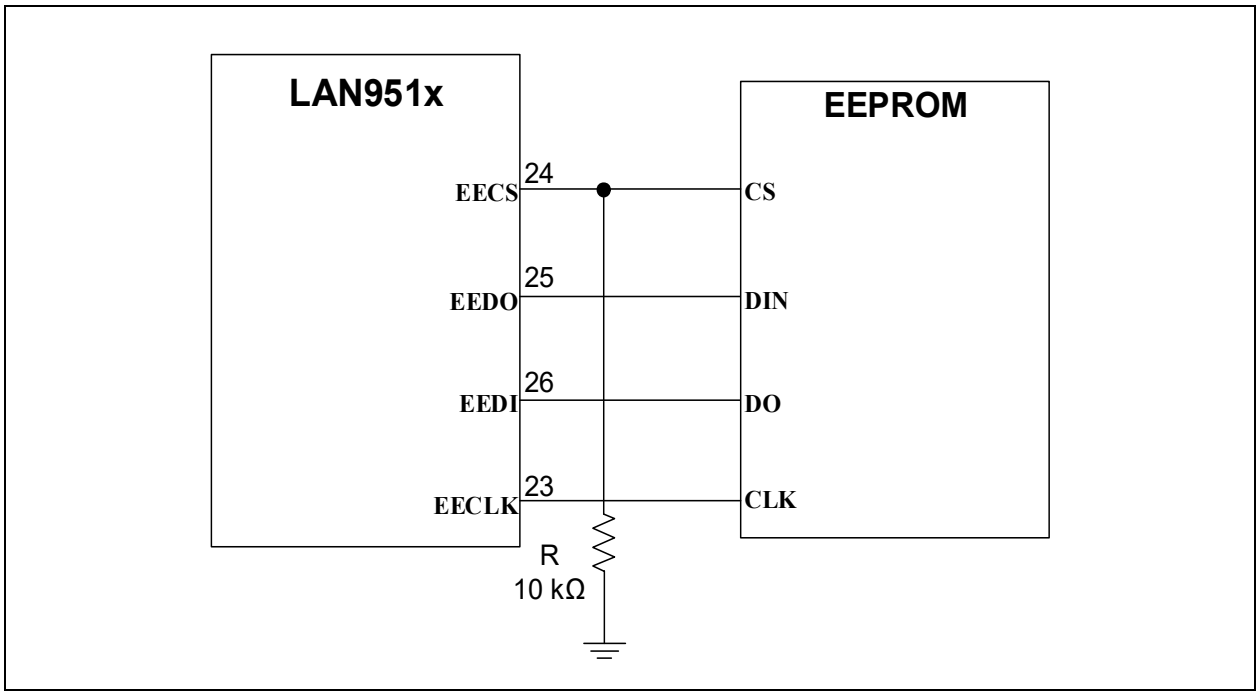
7.0 MISCELLANEOUS

7.1 EEPROM Interface

The LAN9513 may use an external EEPROM to store the default values for the USB descriptors and the MAC address. (See Figure 7-1.) The EEPROM controller supports most “93C46” type EEPROMs. A total of nine address bits are used to support 256/512 byte EEPROMs.

- Select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation.

FIGURE 7-1: EEPROM CONNECTION DIAGRAM



7.2 EXRES Resistor

- **EXRES** (pin 50) should connect to ground through a 12.4 kΩ resistor with a tolerance of 1.0%. This pin is used to set up critical bias currents for the embedded 10/100 Ethernet physical device.

7.3 USBRBIAS Resistor

- **USBRBIAS** (pin 63) should connect to ground through a 12.0 kΩ resistor with a tolerance of 1.0%. This pin is used to set up critical bias currents for the embedded USB physical device.

7.4 Required External Pull-ups/Pull-downs

- GPIO[7:0] require pull-up resistors if configured as open-drain output.

7.5 Configuration Straps

- All configuration strap values are latched in on Power-On Reset and System Reset. For more detailed information on each bit and functionality, consult the latest version of the *LAN9513 Data Sheet*.
- **AUTOMDIX_EN** (pin 41), this pin determines the default Auto MDIX setting. The settings are as follows:
  - 0 = Auto MDIX is disabled.
  - 1 = Auto MDIX is enabled.

See the latest version of the *LAN9513 Data Sheet* for complete details. This pin has a weak internal pull-up and can be driven low with an external 10.0 kΩ resistor to ground.

7.6 nRESET

- **nRESET** (pin 12) is an active-low Reset input. This signal resets all logic and registers within the LAN9513. This signal is pulled high by a weak internal pull-up resistor. If **nRESET** is left unconnected, the LAN9513 will rely on its internal power-on Reset circuitry.

7.7 CLK24_EN and CLK24_OUT

- **CLK24_EN** (pin 44) enables the generation of a 24.0 MHz clock on the **CLK24_OUT** pin, which can be used as a reference clock for other devices. The input signal has no internal termination and should rely on an external resistor. The settings are as follows:
  - 0 = **CLK24_OUT** is disabled.
  - 1 = **CLK24_OUT** is enabled.

7.8 TESTx Pins

- **TEST1** (pin 13), this pin must remain as a no-connection in order to ensure proper operation.
- **TEST2** (pin 34), this pin must be tied directly to digital ground in order to ensure proper operation.
- **TEST3** (pin 40), this pin must be tied directly to +3.3V in order to ensure proper operation.
- **TEST4** (pin 47), this pin must remain as a no-connection in order to ensure proper operation.

NOTES:

8.0 HARDWARE CHECKLIST SUMMARY

TABLE 8-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	Pull up the necessary document(s).		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify that a single ground reference as a system ground is used for all ground pins. Check if there is a chassis ground for the line-side ground.		
	Section 2.4, "USB-IF Compliant USB Connectors"	Verify that USB-IF compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.1, "3.3V Supply"	Ensure **VDD33IO** and **VDD33A** are within the range of 3.0V to 3.6V, and 0.1 µF capacitors are connected to each pin.		
	Section 3.2, "VDD18CORE"	**VDD18CORE** require 0.1 µF bypass each pin and a low-ESR 4.7 µF ceramic capacitor. Do not connect **VDD18CORE** with **VDD18USBPLL** or **VDD18ETHPLL**.		
	Section 3.3, "VDD18USBPLL and VDD18ETHPLL"	**VDD18USBPLL** and **VDD18ETHPLL** require a 1.0 µF bypass capacitor for each pin. The **VDD18ETHPLL** should be connected to **VDD18USBPLL** through a ferrite bead. Do not connect **VDD18CORE** with **VDD18USBPLL** or **VDD18ETHPLL**.		
Section 4.0, "Ethernet Signals"	Section 4.1, "Ethernet PHY Interface"	**TRx** pins require 49.9Ω termination resistors.		
	Section 4.2, "Magnetics Connection"	Verify if the center taps are connected to the **GND** using separate 0.1 µF capacitors on the device side and are terminated with 75 resistors through a 1000 pF, 2 kV capacitor to the chassis ground on the RJ45 line side.		
	Section 4.3, "RJ45 Connector"	Verify if pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to the chassis ground through a 1000 pF, 2 kV capacitor.		

TABLE 8-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "USB Signals"	Section 5.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 5.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance, the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
	Section 5.3.1, "Upstream Port VBUS and VBUS_DET"	Verify that the upstream port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.3.2, "Downstream Port Power Control and OverCurrent Sensing"	Verify that the USB data pins are correctly routed to any embedded USB devices or secondary hub tiers.		
	Section 5.3.3, "Downstream Port Type-C Support"	Verify that the USB data pins are correctly routed to the USB Type-C connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines. Also, ensure that an external Type-C controller capable of DFP operation is present.		
	Section 5.3.4, "GND and Shield Recommendations"	Connect to GND plane through a resistor and capacitor in parallel, or directly to the GND plane.		
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	Verify usage of 25 MHz ±50 ppm crystal or a 25 MHz oscillator. If using crystal, for proper operation, an additional 1.0 MΩ resistor is required for the crystal circuit. This resistor is placed in parallel with the crystal.		
Section 7.0, "Miscellaneous"	Section 7.1, "EEPROM Interface"	Ensure that the selected EEPROM device is compatible with the device.		
	Section 7.2, "EXRES Resistor" and Section 7.3, "USBRBIAS Resistor"	Verify that EXRES and USBRBIAS connect to ground through proper resistors.		
	Section 7.4, "Required External Pull-ups/Pull-downs"	GPIOs require pull-up resistors if configured as an open-drain output.		
	Section 7.5, "Configuration Straps"	Check for default Auto MDIX setting.		
	Section 7.6, "nRESET"	Ensure that **nRESET** signal has an external pull-up resistor or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		
	Section 7.7, "CLK24_EN and CLK24_OUT"	Check for default **CLK24** output setting.		
	Section 7.8, "TESTx Pins"	Verify that **TESTx** pins are configured properly.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004677A (07-22-22)	Initial release	

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