ENT-AN1243

Application Note

VSC8254, VSC8257, and VSC8258 1588 Timestamp Out-of-Sync (OOS) Summary

August 2017

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Contents

1 Revision History 1.0

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in August 2017. It was the first publication of this document.

2 1588 Timestamp Out-of-Sync (OSS)

This document describes the susceptibility of the VSC8254, VSC8257, and VSC8258 devices (revision A die) to incorrectly process timestamps within the IEEE 1588 block. When IEEE 1588 functionality is enabled, the devices should process precision time protocol (PTP) frames by inserting or modifying timestamps within these packets. Certain link conditions, signal impairments, and protocol events can lead to a loss of timestamp coherency, commonly termed out-of-sync (OOS). The methods and impact of entering OOS as well as the software mitigation and recovery routine are covered.

The device family contains the VSC8254, VSC8257, and VSC8258 base part numbers. A device's full part number is visibly marked on the top of each package. The die revision can be determined by reading the last letter of the device's datecode, also printed on the top of the package. Revision D devices, available in the second half of 2017, do not exhibit this susceptibility and so will not require any software routine workaround.

2.1 Loss of Timestamp Coherency

The VSC8254, VSC8257, and VSC8258 devices support the IEEE 1588 functionality by timestamping classified frames with a timestamp based on a calibrated local time counter (LTC) located within the device. The classification of the frame can be based on various types of supported PTP encapsulations, such as PTPoE, PTP-over-IP, and so on.

Timestamp coherency is impacted by several factors. Link conditions such as fiber cuts, fiber pulls, or impairments may truncate packets. Signal impairments, especially to the reference clock for the 1588 engine, will impact the engine's behavior and accuracy. Fault propagation and fault handling may impact traffic and processing.

2.2 Impact of Packet Size

The 1588 processor expects valid packets from the PCS/MAC in both directions, ingress and egress. These packets must be at least 64 bytes long for normal traffic. Short frames are typically a result of a link-down failure, traffic interruption due to fault signaling, or certain manual interventions such as enabling/disabling a loopback during live traffic.

The 1588 processor initiates an internal start of frame (SOF) signal during the reception of the third 64-bit
word (counting from word 1), which contains the preamble and start of frame delimiter (SFD). This signal writes the timestamp (TSP) relating to that frame into a timestamp-storing FIFO (TSP_FIFO). The internal end of frame (EOF) signal is triggered by several possible events and causes the TSP to be removed from the TSP_FIFO.

The 1588 processor handles short frames (shorter than 64 bytes) in different ways, as described in the following sections. The examples given show possible data values presented to the 1588 processor. The dd code is used to represent valid data, CC to represent control characters (excluding faults), and FFFFFFFF to represent faults (local or remote). The ?? code represents “don't care” values.

2.3 Frames 25 Bytes or More (Including Preamble)

Frames with 25 or more bytes (including preamble) are handled properly. The 1588 processor recognizes control and fault characters within words 4 or greater to signal end of frame (EOF), which causes the captured timestamp to be flushed.

Table 1 • Frames 25 Bytes or More

Word/Byte	Value	SOF	EOF	Comment
1/1–8	FB555555555555D5			Preamble and SFD

Word/Byte	Value	SOF	EOF	Comment
2/9–16	dddddddddddddddd			
3/17–24	dddddddddddddddd	Y		SOF asserted, TSP captured

Table 2 • Frames 25 Bytes or More

Word/Byte	Value	SOF	EOF	Comment
N				Preamble and SFD
N+1	ddddddddddddddCC			
N+2	????????????????		Y	SOF asserted, TSP captured

2.4 Frames with 7 or Fewer Bytes of Preamble (No SFD)

Frames with 7 or fewer bytes of preamble are handled properly. Because the short frame does not meet the SOF criteria by containing a SFD, the block does not initiate a timestamp.

Table 3 • Frames with 7 Bytes or Fewer of Preamble_No SFD

Word/Byte	Value	SOF	EOF	Comment
1/1–7	FB555555555555??			Preamble, no SFD
2	????????????????			
3	????????????????	N		No SOF signal, criteria not met

2.5 Frames with 8 to 24 Bytes (Inclusive)

Frames that are within 8 to 24 bytes (inclusive) may cause a loss of timestamp coherency. Because a valid SOF is created, a timestamp is entered into the TSP_FIFO. Thus, loss of timestamp coherency depends on the proper identification and handling of EOF, which is influenced by control characters, faults, and their location.

The EOF logic is summarized in the following pseudo code, using dd to represent valid data, CC to represent control characters (excluding faults), and FFFFFFFF to represent faults.

Figure 1 • Psuedo Code

```
If (Word# == 2 OR Word# == 3)
      If (word contains dd followed by CC [excluding faults])
            EOF = true
      If (word contains all CC [excluding faults])
            EOF = true
If (Word# > 3 AND SOF asserted)
      If (word contains first fault)
            EOF = true
      If (word contains CC [excluding faults])
            EOF = true
```

Table 4 • Case 1: Proper Operation

Word/Byte	Value	SOF	EOF	Comment
1/1–8	FB555555555555D5			Preamble and SFD
2/9–16	dddddddddddddddd	Y		
3/17–24	ddddddddddddddCC		Y	SOF asserted, TSP captured
4	????????????????			EOF asserted due to control character in word 2 or 3

In this case, control characters other than faults in words 2 or 3 result in proper EOF.

Table 5 • Case 2: Proper Operation

Word/Byte	Value	SOF	EOF	Comment
1/1–8	FB555555555555D5			Preamble and SFD
2/9–16	dddddddddddddddd			
3/17–24	dddddddddddddddd	y		SOF asserted, TSP captured
4	ddddddddFFFFFFFF			
5	FFFFFFFFFFFFFFFF		y	EOF asserted as first fault in word >3

In this case, faults begin in words 4 or later.

Table 6 • Case 3: Proper Operation

Word/Byte	Value	SOF	EOF	Comment
1/1–8	FB555555555555D5			Preamble and SFD
2/9–16	dddddddddddddddd			

Word/Byte	Value	SOF	EOF	Comment
3/17–24	ddddddddFFFFFFFF	Y		SOF asserted, TSP captured. First fault within word 2 or 3
4	FFFFFFFFFFFFFFFF		N	EOF does not assert due to design limit, first fault began prior to SOF assertion
N	FFFFFFFFFFFFFFFF			
N+1	CCCCCCCCCCCCCCCC			CC includes Terminate or Idle ordered sets
N+2	????????????????		Y	EOF asserted due to control characters

In this case, faults begin in words 2 or 3 and extend until a control character.

Note: A start-of-packet/preamble/start-of-frame delimiter is not interpreted as a CC.

Table 7 • Case 4: Improper Operation (Faults Begin in Words 2 or 3 and Extend Until a New Frame)

Word/Byte	Value	SOF	EOF	Comment
1/1–8	FB555555555555D5			Preamble and SFD
2/9–16	dddddddddddddddd			
3/17–24	ddddddddFFFFFFFF	Y		SOF asserted, TSP captured. First fault within word 2 or 3
4	FFFFFFFFFFFFFFFF		N	EOF does not assert due to design limit, first fault began prior to SOF assertion
. .	FFFFFFFFFFFFFFFF			
N	FFFFFFFFFFFFFFFF			
N+1	FB555555555555D5			CC includes Terminate or Idle ordered sets
N+2	dddddddddddddddd		Y	EOF asserted due to control characters
N+3	dddddddddddddddd	Y		SOF asserted, TSP captured
N+4	????????????????			

Because the first fault appears within word 2 and/or word 3, an EOF is not asserted and the fault detection logic does not flag the fault from words 4 through N, so the timestamp from word 1 remains in the TSP_FIFO. The arrival of word N+1 with a new SFD followed by a normal frame or any acceptable short frame will result in another SOF and timestamp entry into the TSP_FIFO.

Table 8 • Case 5: Improper Operation (Faults without Control Characters in Words 2 or 3 Result in a Missing EOF)

Word/Byte	Value	SOF	EOF	Comment
1/1–8	FB555555555555D5			Preamble and SFD

Word/Byte	Value	SOF	EOF	Comment
2/9–16	dddddddddddddddd			
3/17–24	ddddddddFFFFFFFF	Y		SOF asserted, TSP captured. First fault within word 2 or 3
4	FB555555555555D5		N	EOF does not assert due to design limit, first fault began prior to SOF assertion
5				
6	FFFFFFFFFFFFFFFF			
N+1	FB555555555555D5			CC includes Terminate or Idle ordered sets
N+2	dddddddddddddddd		Y	EOF asserted due to control characters
N+3	dddddddddddddddd	Y		SOF asserted, TSP captured
N+4	????????????????			

Because the fault codes only appear within word 2 and/or word, 3 an EOF is not asserted, so the timestamp from word 1 remains in the TSP_FIFO. The arrival of Word 4 with a new SFD followed by a normal frame or any acceptable short frame will result in another SOF and timestamp entry into the TSP_FIFO.

For additional details regarding the loss of timestamp coherency/an OOS situation, see Appendix A: TSP_FIFO Operation.

2.6 Impact of Link Status

As previously discussed, the positioning and handling of faults are a significant contributor to the initiation of OOS. During a link transition from up to down or down to up, external factors (such as optical module stabilization, SerDes lock and stabilization, or PCS synchronization to the proper 66-bit code) all result in some amount of block lock chatter that may impact the MAC as well as assertion of link up or down. During this chatter, additional faults may result from the MAC. No convincing data exists to indicate that the chatter differs between a link up and a link down condition.

2.7 Impact of the MAC

The primary difference between the passing case 3 and problematic case 4 is the presence of Idles (control characters) following a fault situation. Some analysis of test hardware and an open-source design shows that the MAC design and/or configuration influence the presence of Idles following a fault, thus impacting the likelihood of an OOS condition.

2.8 Impact of Local Time Counter Clock

The local time clock is the primary clock to the 1588 processor logic. Signals are transferred from the PCS block into the 1588 processor, which operates in different clock domains. Synchronization logic is used to ensure proper signal transfer between domains. The SOF signal from the PCS domain is stretched to three words (18.6 ns) as it crosses to the 1588 processor domain. Assuming the lowest allowed 1588 processor clock frequency of 125 MHz (or an 8 ns period), if one edge is missed due to a glitch or intended clock transition, the second edge will still arrive within the 18.6 ns SOF pulse width, thus allowing the signal to correctly cross domains. If no edges occur during the 18.6 ns SOF pulse, the 1588 processor domain will lose synchronization with the data path, resulting in a command FIFO error known as TSP_CMD_FIFO OOS. If this situation occurs, the software synchronization routine must be called (Software Recovery).

Note: Because the local time counter (LTC) is based off the 1588 processor clock, any missing edges will result in a LTC error. This error will continue until the counter is reloaded or updated.

2.9 1G Mode

When the VSC8254, VSC8257, and VSC8258 devices are configured for 1G operation, internal MACs are enabled to handle flow control. These MACs reside between the PCS block and the 1588 engine. The MACs discard short frames, potentially protecting against OOS causing short frames. Furthermore, local and remote faults are not used in 1G mode, again avoiding the OOS causing criteria.

2.10 MACsec Mode

When the VSC8254, VSC8257, and VSC8258 devices are configured for either 1G or 10G MACsec operation, the internal MACs are enabled to handle flow control and other features. The inclusion of the MACs in the data path has system implications for link fault signaling, link management, and latency. These MACs reside between the PCS block and the 1588 engine and will discard short frames, thus avoiding potential OOS causing conditions.

If the user intends to enable or disable MACsec while 1588 is enabled and processing live traffic, it is imperative that the specific sequence of API calls be used. If the incorrect procedure is used, it is possible that 1588 correction factors used to compensate for delays in the MACsec block will be corrupted, resulting in an OOS-like condition.

3 Software Recovery

he VSC8254, VSC8257, and VSC8258 devices contain no mechanism to detect that the TSP_FIFO has entered an OOS state. Without a direct detection mechanism, a mitigation and recovery strategy is necessary. The recovery sequence described here should be called following any potential OOSinducing event.

The following events may be used to initiate the recovery function call.

- A link down state (either 10G PCS or XAUI PCS)
- External MAC detection of local or remote faults

3.1 Recovery Procedure

The various recovery procedures are described in the following sections.

3.1.1 Recovery Procedure for Revision A in 10G Mode

The following sequence of transactions is used to ensure that the TSP_FIFO is reset.

1. Identify the appropriate interrupt and clear it
2. Enable 1588 bypass
3. Reset 1588 ingress block
4. Reset 1588 egress block
5. Reload local delays (both ingress and egress)
6. Disable 1588 bypass. If `MALIBU_A_BYPASS_API` is set, the API will immediately disable the 1588 bypass. If set to False, it is the user's responsibility to call the disable bypass function following a stable linkup within their application code.

The VTSS_ARCH_MALIBU_C compilation flag must be set to True for proper code operation with revision A devices. The `MALIBU_A_BYPASS_API` flag must be set appropriately to select when the egress bypass feature is disabled. True will release it when the link is down while False requires the application code to call the disable bypass function.

If the recovery procedure is called upon a link-down condition, it is possible that the link-up chatter may induce a new OOS condition. To avoid such a condition, it is recommended that the 1588 blocks be bypassed until a stable link-up condition is found. For this reason, it is recommended that `MALIBU_A_BYPASS_API` be set to False and that the bypass be disabled upon a stable link-up state. When the bypass is enabled, no PTP frames will be timestamped. The implications of no timestamping should be further considered by the customer.

3.1.2 Recovery Procedure for Revision A in 1G Mode

The following sequence of transactions is used to ensure that the TSP_FIFO is reset.

1. Identify the appropriate interrupt and clear it
2. Enable 1588 bypass
3. Wait 100 ms
4. Reset 1588 ingress block
5. Reset 1588 egress block
6. Wait 5 ms
7. Reload local delays (both ingress and egress)
8. Disable 1588 bypass. If `MALIBU_A_BYPASS_API` is set, the API will immediately disable the 1588 bypass. If set to False, it is the user's responsibility to call the disable bypass function following a stable linkup within their application code.

The `VTSS_ARCH_MALIBU_B` compilation flag must be set True for proper code operation with revision A devices.

If the recovery procedure is called upon a link-down condition, it is possible that the link-up chatter may induce a new OOS condition. To avoid such a condition, it is recommended that the 1588 blocks be bypassed until a stable link-up condition is found. When the bypass is enabled, no PTP frames will be timestamped. The implications of no timestamping should be further considered by the customer.

3.1.3 API Call

The following call should be included within the customer application code to mitigate the occurrence of TSP_FIFO OOS following detection of a link down or other previously mentioned OOS-inducing event.

```
vtss_rc vtss_phy_ts_10g_fifo_sync(const vtss_inst_t inst,

const vtss_port_no_t port_no,

const vtss_debug_printf_t pr)
```

This function will in turn call other functions depending upon the device identification and intended response.

3.1.4 Design Considerations

The software workaround for revision A can be called during a link-up state. While the 1588 block is in bypass as part of the recovery routine, any PTP frames traversing the device will not be timestamped, and so there may be an impact to related timestamp calculations. Because the timestamp coherency issue may occur in either the ingress or egress direction, path delay values in both directions should be examined.

4 Appendix A: TSP_FIFO Operation

Under normal operating conditions, the device will generate a timestamp upon reception of any packet, either at the host or line interface. Although every packet creates a timestamp, only PTP-classified packets will require its timestamp for further processing. Timestamps of non-classified packets will traverse the processor, but not be used. PTP-related timestamps may be directly inserted into PTP frames at a specific field location, used for calculation of parameters like residence time, and/or added to the correction field of the packet, based on the 1588 operating mode. The process for ingress PTP frames is the same as egress PTP frames. The scope of each timestamp is strictly local to the frame for which it is generated.

For each frame reception, regardless of the classification, the following operations are expected:

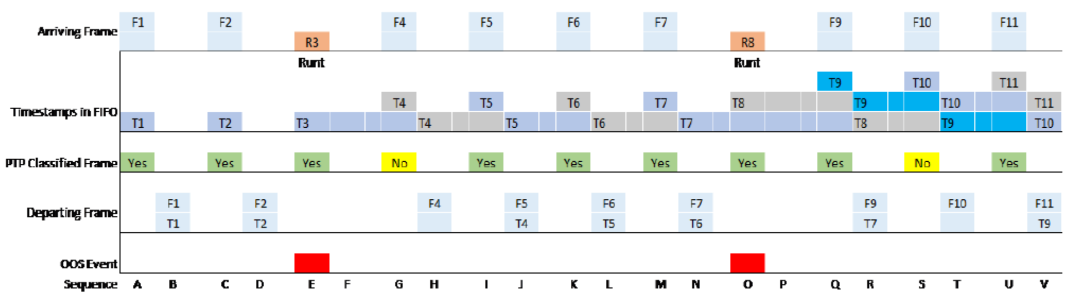
- Push timestamp entry into the TSP_FIFO corresponding to frame reception on the line or host interface (depending on the direction: ingress or egress).
- Optional write of the timestamp from the head of the TSP_FIFO into the frame upon its departure.
- Pop the timestamp entry from the TSP_FIFO when the frame completes.

Every time a start of frame is detected at the interface, a timestamp is generated and pushed into the TSP_FIFO, which will hold this entry until a pop operation is issued to pull the FIFO's next entry after the frame is written with this timestamp upon its departure from the 1588 processor. However, if for some reason every frame received does not have a corresponding pop operation, the FIFO will accumulate an extra timestamp, causing subsequent packets to be loaded with the incorrect timestamp.

It is possible that link events such as fiber breaks, fiber pulls, link flaps, or certain traffic interruptions may meet the defined criteria and cause the TSP_FIFO go out-of-sync. Frames following an OOS condition will be timestamped with the time from past frames. This continues for every classified frame thereafter, until the OOS condition is cleared.

The following illustration shows the sequence of events relating to timestamps. It demonstrates two OOS conditions as a result of short or runt frames meeting the inducing criteria and the events following it.

Figure 2 • Timestamp Sequence



A, B: Rx PTP frame F1, T1 into FIFO, T1 out of FIFO and into outgoing F1 (Normal)
C, D: Rx PTP frame F2, T2 into FIFO, T2 out of FIFO and into outgoing F2 (Normal)
E, F: Rx runt frame R3, T3 into FIFO, nothing outgoing so T3 remains in FIFO
G, H: Rx std. frame F4, T4 into FIFO, T3 out of FIFO but NOT placed in outgoing F4
I, J: Rx PTP frame F5, T5 into FIFO, T4 out of FIFO and into outgoing F5 (Wrong)
K, L: Rx PTP frame F6, T6 into FIFO, T5 out of FIFO and into outgoing F6 (Wrong)
M, N: Rx PTP frame F7, T7 into FIFO, T6 out of FIFO and into outgoing F7 (Wrong)
O, P: Rx runt frame R8, T8 into FIFO, nothing outgoing so T7 and T8 remain in FIFO
Q, R: Rx PTP frame F9, T9 into FIFO, T7 out of FIFO and into outgoing F9 (Wrong)
S, T: Rx std. frame F10, T10 into FIFO, T8 out of FIFO but NOT placed in outgoing F10
U, V: Rx PTP frame F11, T11 into FIFO, T9 out of FIFO and into outgoing F11 (Wrong)

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VPPD-04473