# 40 GHz Divide-by-1 to 127 Programmable Integer Divider
## UXN40M7K

**MICROCHIP**

## Product Overview

The UXN40M7K is a highly programmable integer divider covering all integer divide ratios between 1 and 127. The device features single-ended or differential inputs and outputs. Parallel control inputs are CMOS- and LVTTL-compatible for ease of system integration. The UXN40M7K is packaged in a 24-pin, 4 mm × 4 mm leadless ceramic surface mount package.

### Key Features

- Wide operating range: 0.5 GHz – 40 GHz
- Contiguous divide ratios: 1 to 127 Large Output Swings: > 600 mVpp/side
- Single-ended and/or differential inputs and outputs
- Parallel control lines
- Low SSB phase noise: –153 dBc at 10 kHz offset

### Applications

The UXN40M7K can be used as a general purpose, highly configurable divider in a variety of high-frequency synthesizer applications. Fast switching combined with a wide range of divide ratios make the UXN40M7K an excellent choice for fractional-N and integer-N PLLs. Fractional division may be achieved by applying a sequence to the divider control lines, such as a delta-sigma modulated sequence.

**Table 1.** Performance Overview

| Parameter | Typ. | Units |
|---|---|---|
| Input frequency | 0.5 – 50 | GHz |
| Output power | + 2 | dBm |

**Export classification**: EAR99

*Functional Block Diagram*
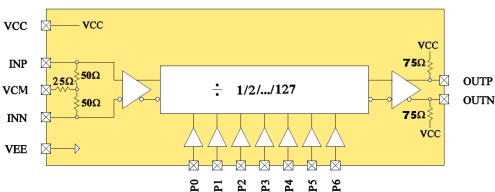


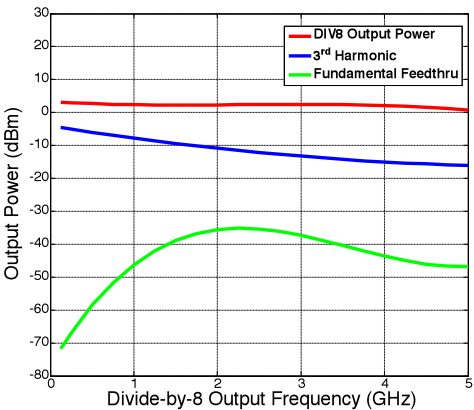*Divide-by-8 Output Power, 3rd Harmonic and Input Feedthru*

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# 1. Electrical Performance

This section shows the electrical performance of the UXN40M7K device.

## 1.1 Typical Electrical Performance

This section shows the typical electrical performance of the UXN40M7K device at +25 °C, + 3.3V/230 mA, and 50Ω terminations, unless otherwise specified.

**Table 1-1.** Typical Electrical Performance

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Input frequency | 0.5 | | 50 | GHz |
| Input power | −10 | 0 | +10 | dBm |
| Output power | | +2 | | dBm |
| DC power dissipation | | 0.75 | | W |

## 1.2 Typical Performance Curves

The following graphs show the typical performance curves of the UXN407K device at +25 °C and + 3.3V/230 mA, unless otherwise specified.

**Figure 1-1.** Input Sensitivity Window: Min/Max Single-Ended Input Power
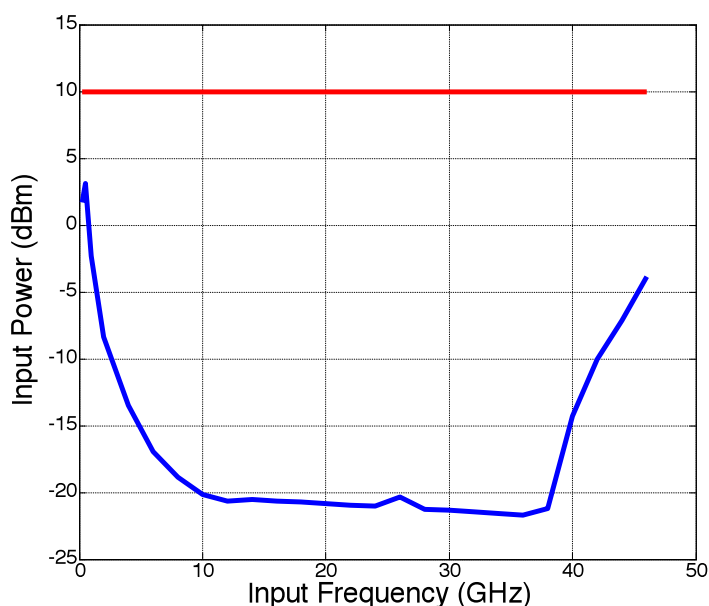


**Figure 1-2.** Divide-by-8 Output Power, 3rd Harmonic and Input Feedthru
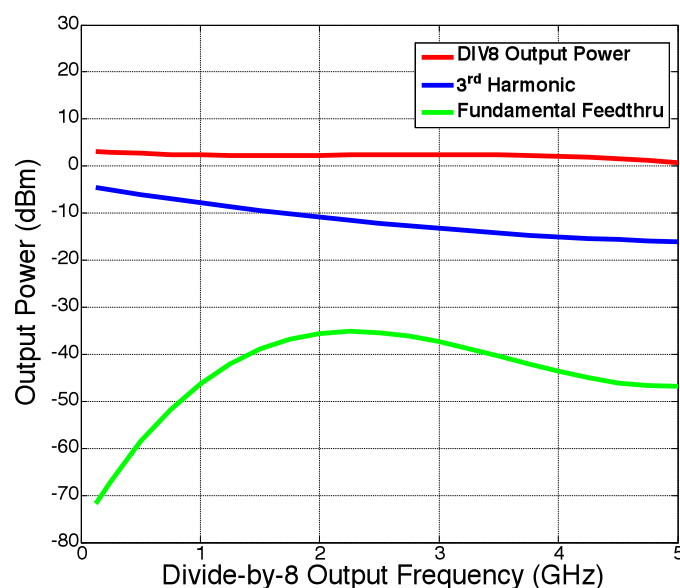
**Figure 1-3.** Static Divide-by-80 Configuration: Input Freq = 40 GHz at 25 °C
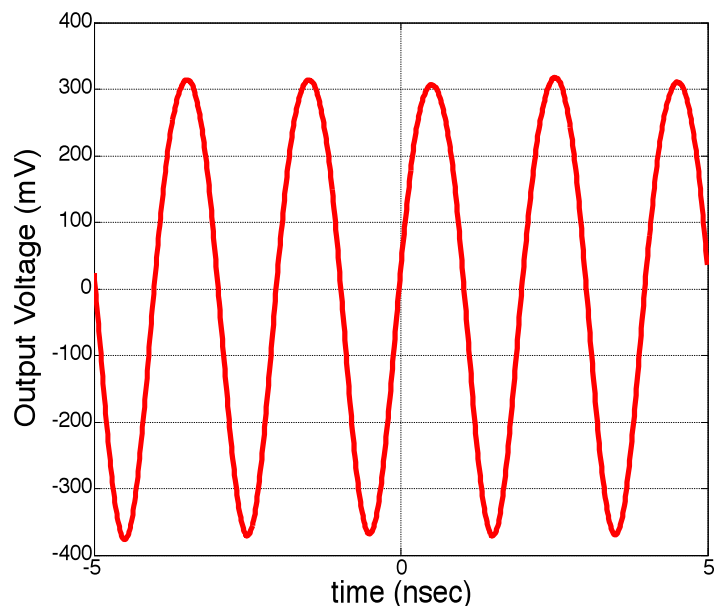


**Figure 1-4.** Static Divide-by-127 Configuration: Input Freq = 40 GHz at 25 °C
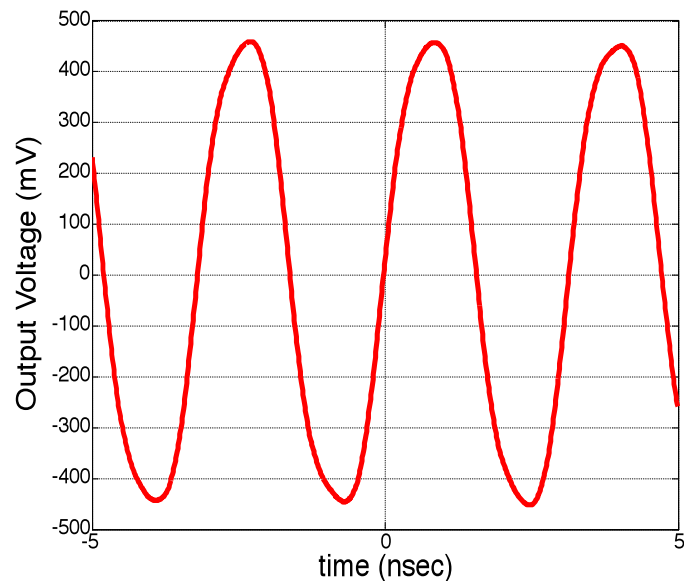


**Figure 1-5.** Output Amplitude vs. Frequency (N=2)
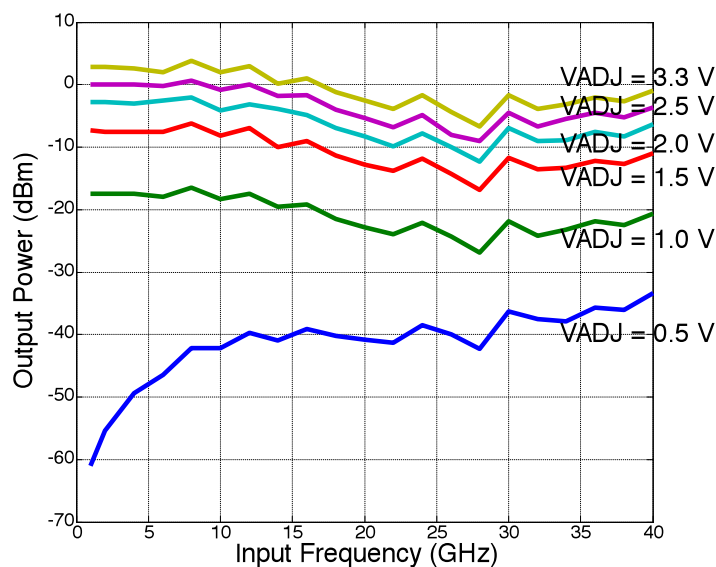


**Figure 1-6.** Fundamental Feedthru
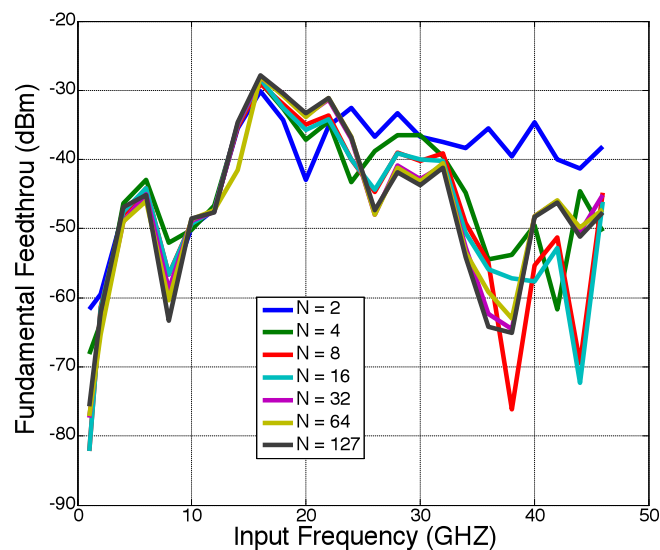
**Figure 1-7.** Sensitivity Window vs. Supply Voltage



**Sensitivity vs Supply Voltage**
**N = 42 (SW = 0101010)**
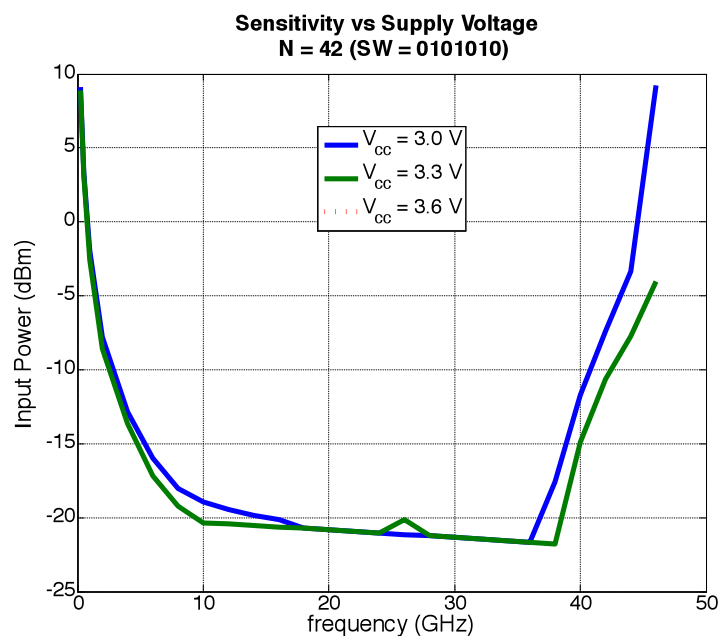
**Figure 1-8.** Sensitivity Window vs. Temperature



**Sensitivity vs Temperature**
**N = 85 (SW = 1010101)**
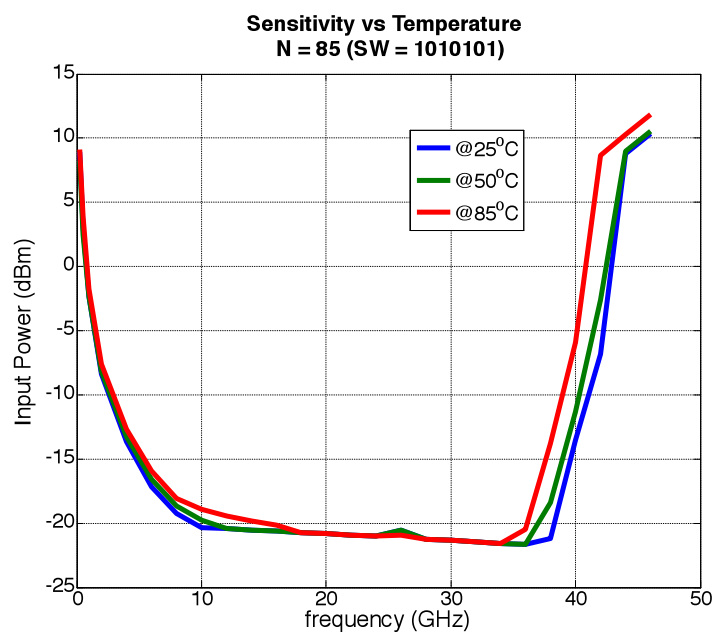
**Figure 1-9.** S11



**Figure 1-10.** S12

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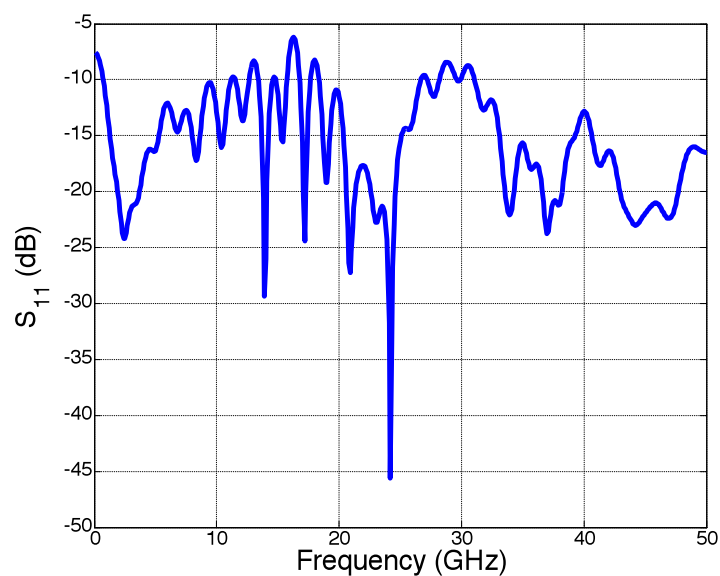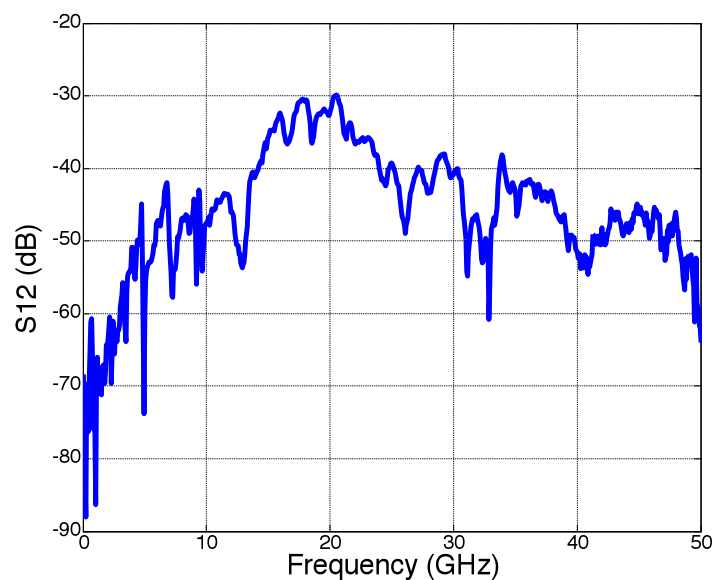
**Figure 1-11.** S21
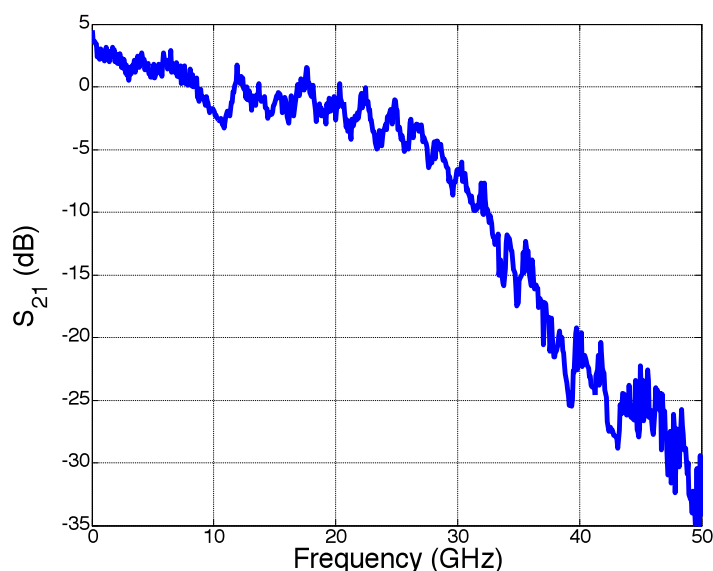


**Figure 1-12.** S22
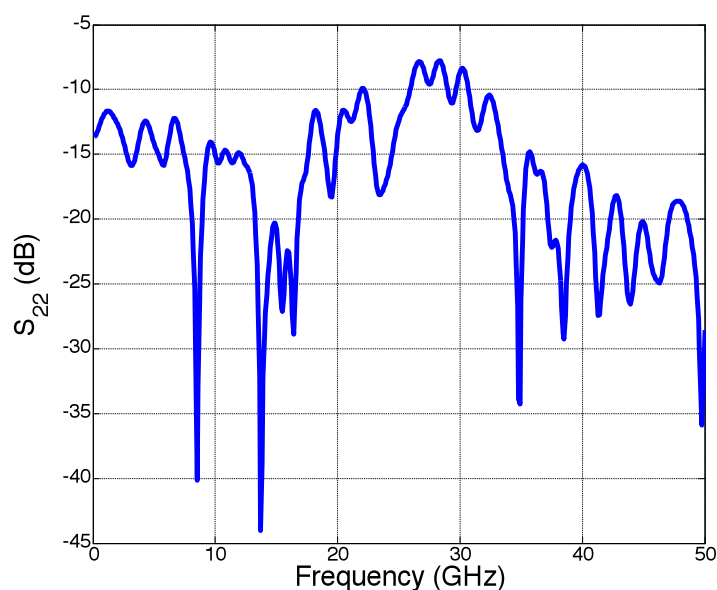


## 1.3    Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the UXN40M7K devices at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings could potentially cause damage or latent defects to the device.

**Table 1-2.** Absolute Maximum Ratings

| Parameter | Rating |
|-----------|--------|
| Supply voltage (VCC – VEE) | 3.6V |
| RF input power (INP, INN) | +10 dBm |
| Operating temperature | –40 °C to +85 °C |
| Junction temperature | +125 °C |
| Storage temperature | –85 °C to +125 °C |

ESD Sensitive Device

## 1.4    ESD Sensivity

Although SiGe ICs have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling. Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the low-frequency inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 100V. For performance reasons, the RF inputs are not protected with ESD diodes and the ESD sensitivity is higher

# 2. Package Specifications

For additional packaging information, contact your Microchip sales representative.

**Figure 2-1.** Package Outline Drawing
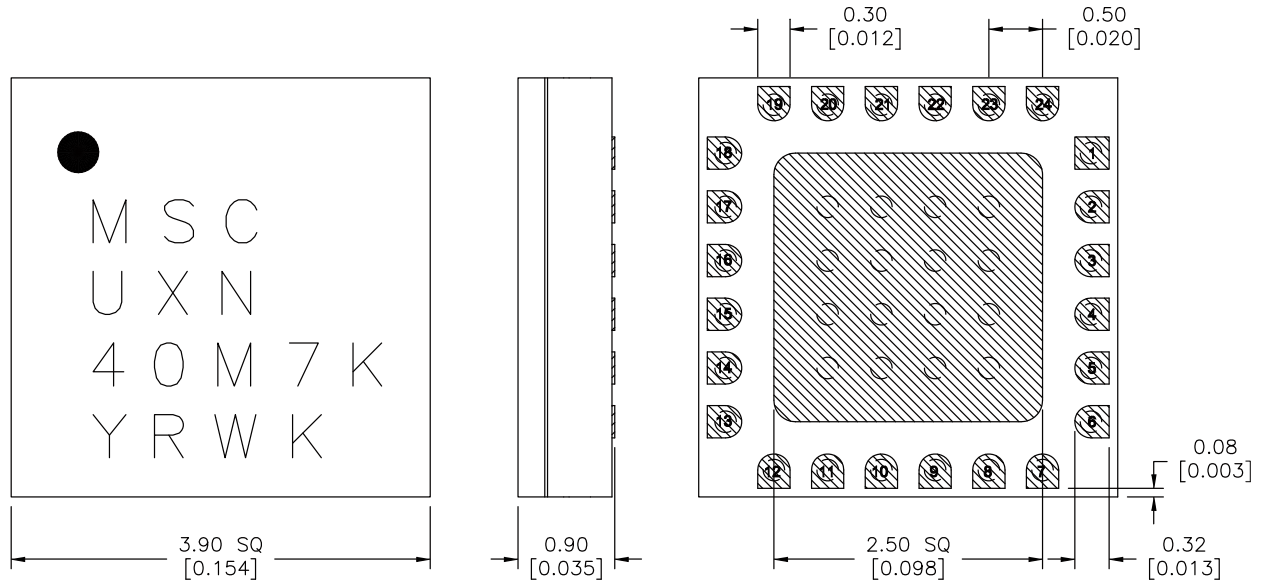


4 mm × 4 mm, 32L Air Cavity Ceramic QFN Package

**Table 2-1.** Package Information

| Parameter | Specification |
|---|---|
| Plating | Ni/Au |
| Package body material | Alumina |

**Table 2-2.** I/O Pad Description

| PIN Number | PIN Label | PIN Description | Notes |
|---|---|---|---|
| 4 / 5 | INP / INN | Divider differential REF inputs, positive/negative terminal | |
| 14/ 15 | OUTP / OUTN | Divider differential RF outputs, positive/negative terminal | |
| 20, 21, 22, 23, 24, 1, and 2 | R[6:0] | Divide modulus control | Defaults to logic 0, Connect ot VCC for logic 1. MSB =R6 |
| 18 | VADJ | Diff. output voltage analog control | Tie to VCC for max swing |
| 6 | VCM | Common mode input | Refer to Functional Diagram |
| 7, 10, 11, 13, 16, and 19 | VCC | Positive supply voltage | Nominally +3.3V/230 mA |
| 3, 8, 9, 12, and 17 | VEE | RF and DC ground | 0V |
| PKG backside | | DC/RF ground | Tie to heat sink |

# 3.    Operation

**Figure 3-1.** Functional Block Diagram
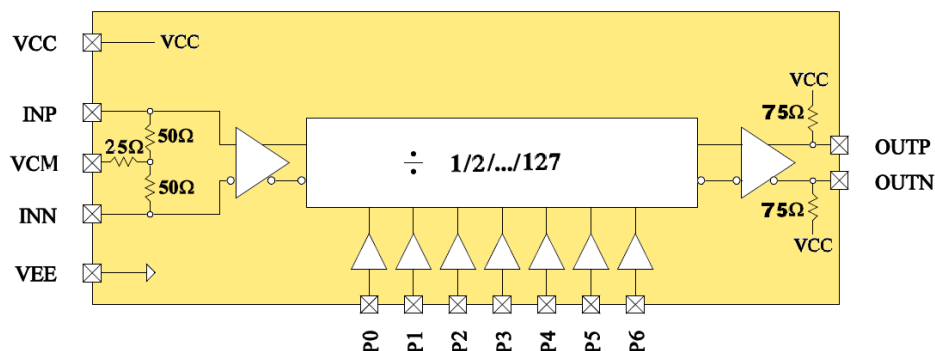


**Divider Modulus Equation**

$$N = P_0.2^0 + P_1.2^1 + P_2.2^2 + .... + P_6.2^6$$
$$\text{for } 1 \leq N \leq 127$$

Setting all bits to 0 results in N=1.

**Figure 3-2.** Simplified Control Logic Input
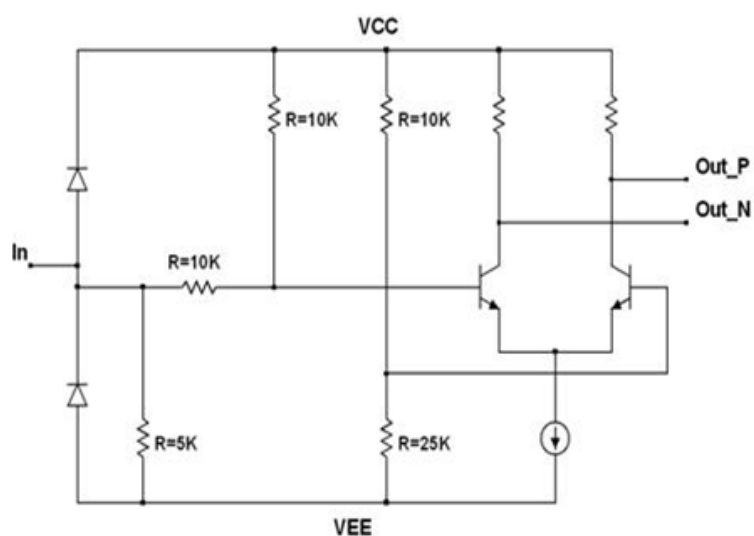


**Table 3-1.** CMOS Levels for Control Lines P0-P8

| Logic Level | Minimum | Typical | Maximum |
|---|---|---|---|
| 1 (high) | VCC – 1.3V | VCC | VCC |
| 0 (low) | VEE | VEE | VEE + 0.8V |

# 4. Application Note

### Low-Frequency Operation

Low-frequency operation is limited by external coupling capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the capacitors. Sine-wave inputs are limited to ~500 MHz.

The values of the coupling capacitors for the high-speed inputs and outputs (I/Os) are determined by the lowest frequency the IC will be operated at: $C >> \dfrac{1}{2\pi.50.f_{lowest}}$

For example, to use the device below 1 GHz, coupling capacitors should be larger than 3 pF.

### IC Assembly

The device is designed to operate with either single-ended or differential inputs. Figure 4-2 shows the IC assembly diagram for positive supply voltage. The supply should be capacitively bypassed to ground to provide a good AC ground over the frequency range of interest. RF I/Os should be AC-coupled through series capacitors. The backside of the chip should be connected to a good thermal heat sink.

### Differential vs. Single-Ended

The UXN40M7K is fully differential to maximize signal-to-noise ratios for high-speed operation. The high-speed outputs are terminated to VCC with on-chip 75Ω resistors. The maximum DC voltage on either of the output terminals must be limited to VCC ±1V to prevent damaging the termination resistors with excessive current.

The outputs require a DC return path capable of handling ~24 mA per side with VADJ set to VCC. With AC coupling on the output, a bias tee circuit such as is shown below is recommended for fastest operation with maximum swing. The value of the capacitor should be large enough to pass the lowest frequencies of interest. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

**Figure 4-1.** RF Output Bias



$$C = \frac{L}{R \cdot R}$$

$$L = \frac{R}{2 \cdot \pi \cdot f_{low}}$$

$$R = 50\ \Omega$$
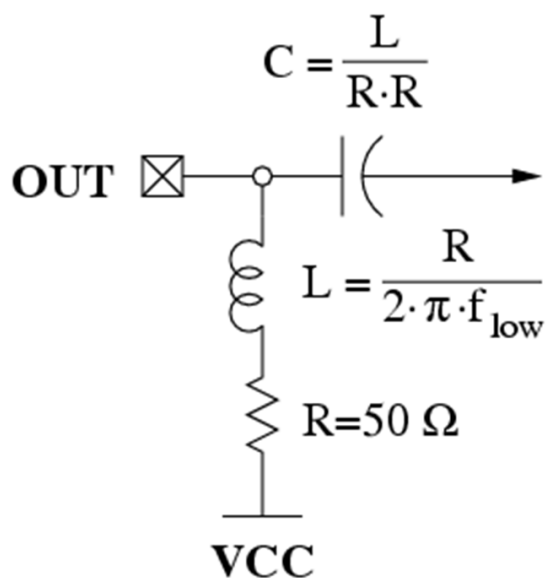
The high-speed inputs are terminated to an internal reference voltage (Vref) that is set by a resistive divider between VCC and VEE. (See Figure 4-2.) For VCC = 3.3V and VEE tied to ground, the nominal value of Vref is 1.9V, and equivalent impedance from Vref is ~800Ω. It is recommended that DC voltage on any of the input terminals be maintained between a minimum of VEE – 1V and a maximum of VCC + 1V.

Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Connecting a 10 kΩ resistor between either input and VEE should provide sufficient offset to prevent oscillation.

The UXN40M7K can also be used in single-ended applications. All unused ports should be terminated with the same loading as the ports being used.

**Figure 4-2.** Positive Supply AC Coupling
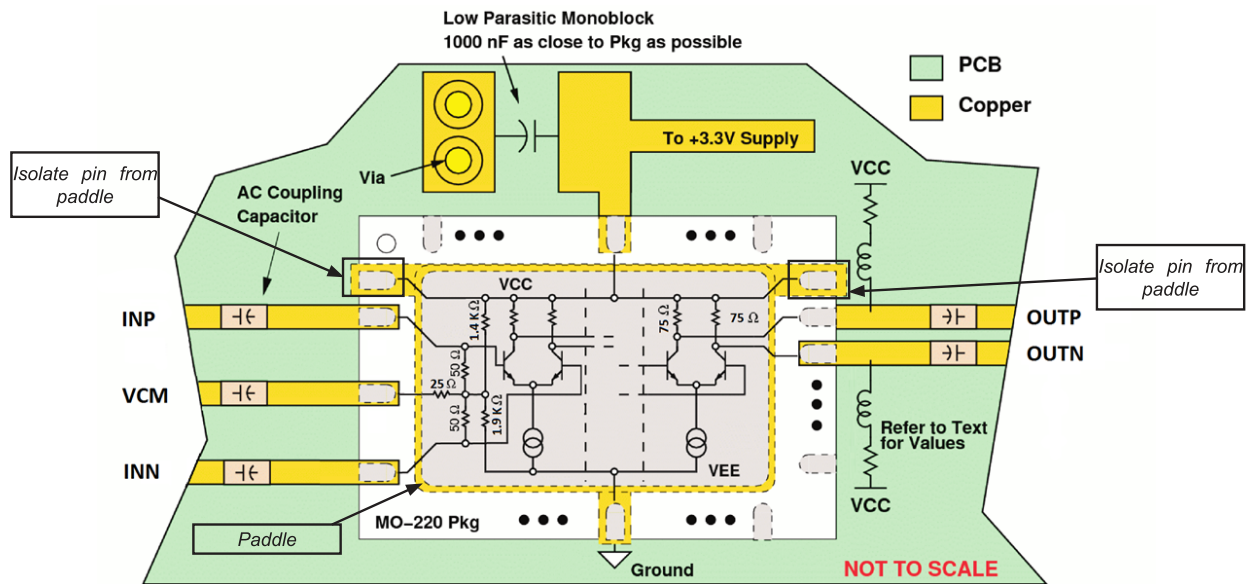


### Duty Cycle

The UXN40M7K output duty cycle varies between 33% and 66% as a function of the divide ratio, N. When N is a power of 2, the duty cycle is exactly 50%. As N deviates from a power of 2, so does the duty cycle deviate from 50%. For example, N=64 has 50% duty cycle, N=60 has 47% duty cycle, and N=56 has 43% duty cycle. Equation 4-1 and Equation 4-2 provide formulas for calculating pulse width and duty cycle as a function of N, for any integer N from 2 to 127. The table to the right shows the pulse width and duty cycle for N from 2 to 16, and duty cycle versus N is plotted below for N from 2 to 127.

**Equation 4-1.**

$$Pulse\,Width\Big(Input\,Cycles\Big) \;=\; N - 2^{floor[\log2(N/3)\,+\,1]}$$

**Equation 4-2.**

$$DutyCycle\Big(1\,\%\Big) \;=\; \frac{PulseWidth}{Divide\,Ratio}x100\,\%$$

**Table 4-1.** Duty Cycle Summary

| Divide Ratio | Pulse Width (Input Cycles) | Duty Cycle (%) |
|---|---|---|
| 2 | 1 | 50 |
| 3 | 1 | 33 |
| 4 | 2 | 50 |
| 5 | 3 | 60 |
| 6 | 2 | 33 |
| 7 | 3 | 43 |
| 8 | 4 | 50 |
| 9 | 5 | 55 |
| 10 | 6 | 60 |
| 11 | 7 | 63 |
| 12 | 4 | 33 |
| 13 | 5 | 38 |
| 14 | 6 | 43 |
| 15 | 7 | 47 |
| 16 | 8 | 50 |

**Figure 4-3.** Timing Diagram
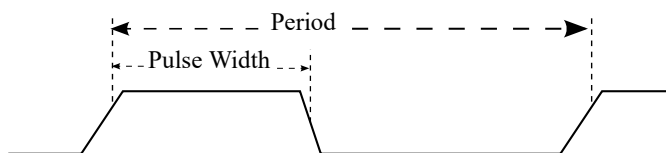


**Figure 4-4.** Duty Cycle Divide vs. Divide Ratio for N =1 to 127
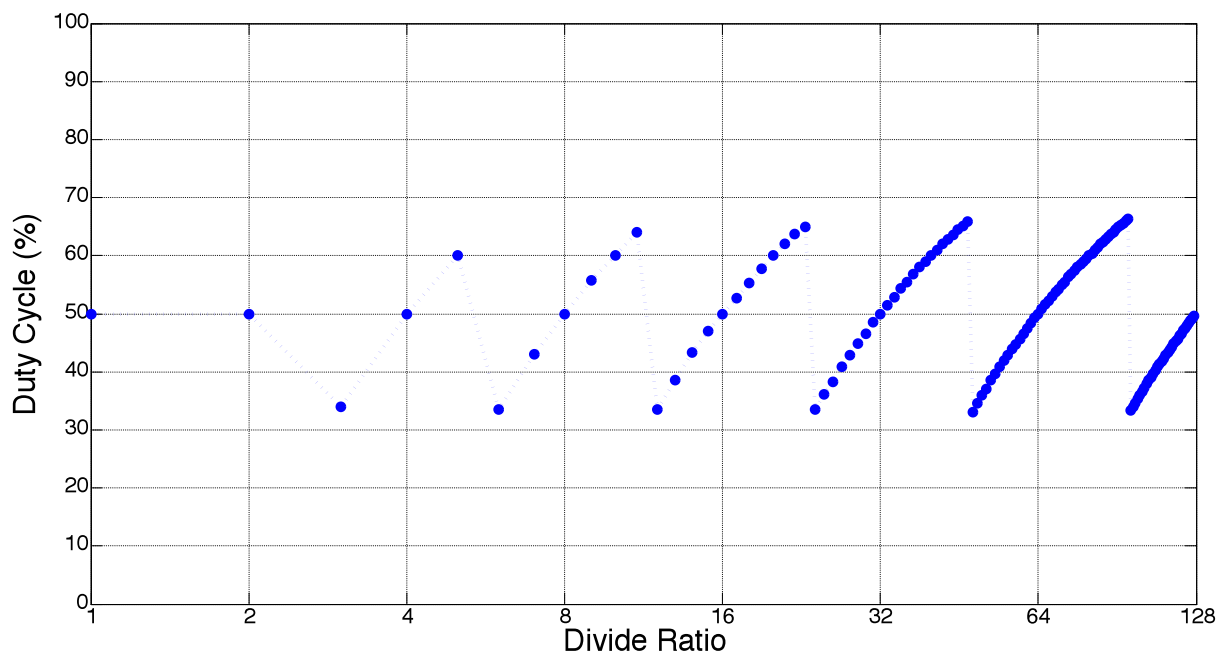
# 5.    Ordering, Shipping, and Handling

This section shows the ordering, shipping, and handling information for the UXN40M7K device.

## 5.1    Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the datasheet.

## 5.2    Ordering Information

For additional ordering information, contact your Microchip sales representative.

| Part Number | Package | Note |
|---|---|---|
| UXN40M7K | 4 mm × 4 mm, 24L Air Cavity Ceramic QFN | NiAu plating finish |
| UXN40M7K-Sn63 | 4 mm × 4 mm, 24L Air Cavity Ceramic QFN | Sn63Pb37 plating finish (gold embrittlement elimination) |
| UXN40M7KE | UXN40M7K Eval PCB | |

## 5.3    Packing Information

| Part Number | Description |
|---|---|
| UXN40M7K/TR | Tape and reel |

**Note:**   Contact your Microchip sales representative for the minimum quantity order

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# 6. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

**Table 6-1.** Revision History

| Revision | Date | Description |
|----------|---------|-------------------|
| A | 03/2024 | Document created. |

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