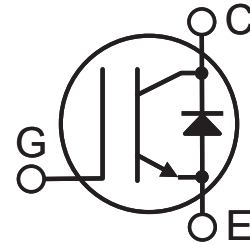
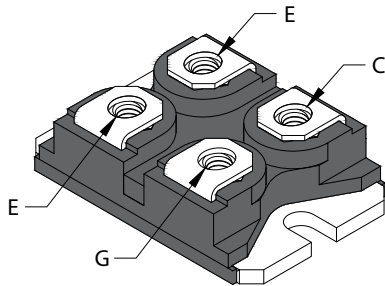


Product Overview

1200 V, 60 A at 20 kHz Power MOS 7 punch-through (PT) IGBT with co-packaged anti-parallel SiC diode, SOT-227




G—Gate
C—Collector, Diode Cathode
E—Emitter, Diode Anode

Table 1. Ordering Information

Catalog Part Number (CPN)	Package	Packing Media	Qualification
APT75GP120JSC30	SOT-227	Tube	Industrial

Features

- Low conduction loss and saturation voltage
- Low gate charge
- Ultrafast tail current shutoff
- No reverse recovery
- High operating frequency
- Reverse-bias safe operating area (RBSOA) rated
- RoHS compliant
- Isolated voltage to 2500 V, UL certified file E145592 
- Zero E_{on} switching loss from co-packaged, anti-parallel diode

1. Device Specifications: IGBT

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{CES}	Collector-emitter voltage	1200	V
V_{GE}	Gate-emitter voltage	± 20	
I_{C1}	Continuous collector current ($T_C = 25\text{ }^\circ\text{C}$)	128	A
I_{C2}	Continuous collector current ($T_C = 110\text{ }^\circ\text{C}$)	57	
I_{CM}	Pulsed collector current ¹ ($T_C = 150\text{ }^\circ\text{C}$)	300	
RBSOA	Reverse-bias safe operating area ($T_J = 150\text{ }^\circ\text{C}$, 960 V)	300	
P_D	Total power dissipation	543	W

Note:

1. Repetitive rating: Pulse width and case temperature limited by the maximum junction temperature.

1.2 Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance (IGBT)		0.16	0.23	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-case thermal resistance (diode)		0.60	0.87	
T_J, T_{STG}	Operating and storage junction temperature range	-55		150	$^\circ\text{C}$
$V_{ISOLATION}$	RMS voltage (50 Hz–60 Hz sinusoidal waveform from terminals to mounting base for 1 minute)	2500			V
τ_M	Mounting torque, M3 screw for heat sink attachment (requires 2, not included)		0.8		N·m
τ_T	Terminal screw torque, M4 screw (4 included)			1.1	
Wt	Package weight		29.2		g

ESD practices should comply with JESD-625.

1.3 Electrical Performance

The following table shows the static characteristics of this device. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}, I_G = 1200\text{ }\mu\text{A}$	1200			V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 2.5\text{ mA}$	3	4.5	6	
$V_{CE(on)}$	Collector-emitter on voltage	$V_{GE} = 15\text{ V}, I_C = 75\text{ A}$		3.3	3.9	
		$V_{GE} = 15\text{ V}, I_C = 75\text{ A}, T_J = 125\text{ }^\circ\text{C}$		3.0		

Table 1-3. Static Characteristics (continued)

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
I _{CEs}	Collector cut-off current ¹	V _{CE} = 1200 V, V _{GE} = 0 V			1200	μA
		V _{CE} = 1200 V, V _{GE} = 0 V, T _J = 125 °C			6000	
I _{GES}	Gate-emitter leakage current	V _{GE} = ±20 V			±100	nA

Note:

1. I_{CEs} includes both IGBT and diode leakages.

The following table shows the dynamic characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C _{ies}	Input capacitance	V _{GE} = 0 V, V _{CE} = 25 V, f = 1 MHz		7035		pF
C _{res}	Reverse transfer capacitance			80		
C _{oes}	Output capacitance			460		
V _{GEP}	Gate-to-emitter plateau voltage	V _{GE} = 15 V, V _{CE} = 600 V, I _C = 75 A		7.5		V
Q _G	Total gate charge ¹			320		
Q _{GE}	Gate-emitter charge			50		
Q _{GC}	Gate-collector ("Miller") charge			140		
RBSOA	Reverse-bias safe operating area	T _J = 150 °C, R _G = 5 Ω, V _{GE} = 15 V, V _{CE} = 960 V, L = 100 μH	300			A
t _{d(on)}	Turn-on delay time	V _{CC} = 600 V, V _{GE} = 15 V, I _C = 75 A, R _G = 5 Ω, T _J = 25 °C		20		ns
t _r	Current rise time			40		
t _{d(off)}	Turn-off delay time			165		
t _f	Current fall time			55		
E _{on}	Turn-on switching energy ²				2857	
E _{off}	Turn-off switching energy ³			2500		
t _{d(on)}	Turn-on delay time	V _{CC} = 600 V, V _{GE} = 15 V, I _C = 75 A, R _G = 5 Ω, T _J = 125 °C		20		ns
t _r	Current rise time			40		
t _{d(off)}	Turn-off delay time			245		
t _f	Current fall time			115		
E _{on}	Turn-on switching energy ²				2885	
E _{off}	Turn-off switching energy ³			4820		

Notes:

1. See MIL-STD-750 Method 3471.
2. E_{on} is the clamped inductive turn-on-energy of this device; there is no contribution to E_{on} from the SiC diode. (See Figures 1-22, 1-23.)
3. E_{off} is the clamped inductive turn-off energy measured in accordance with JEDEC standard JESD24-1. (See Figures 1-22, 1-24.)

1.4 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Output Characteristics

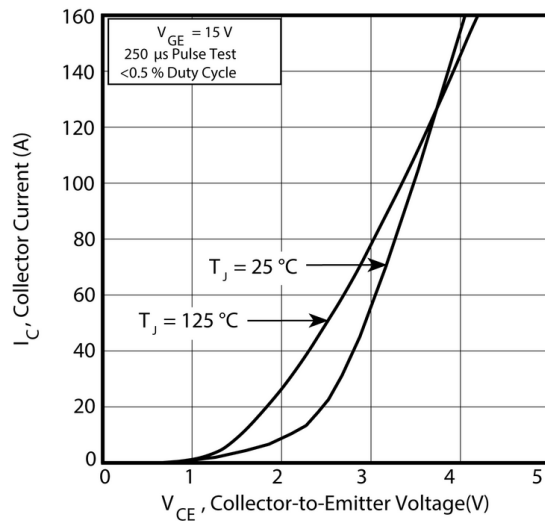


Figure 1-2. Output Characteristics

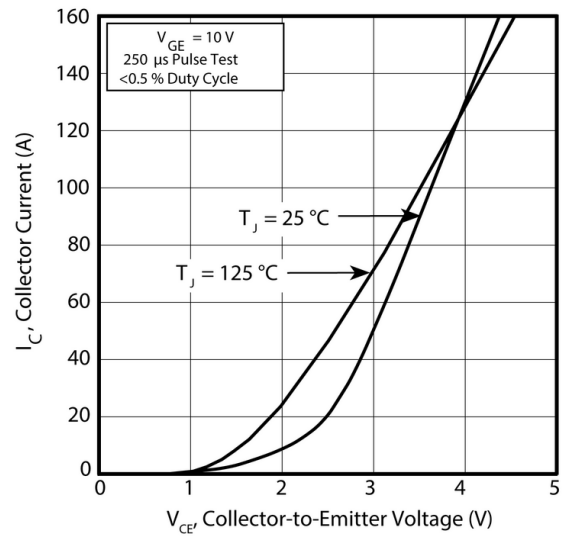


Figure 1-3. Transfer Characteristics



Figure 1-4. Gate Charge

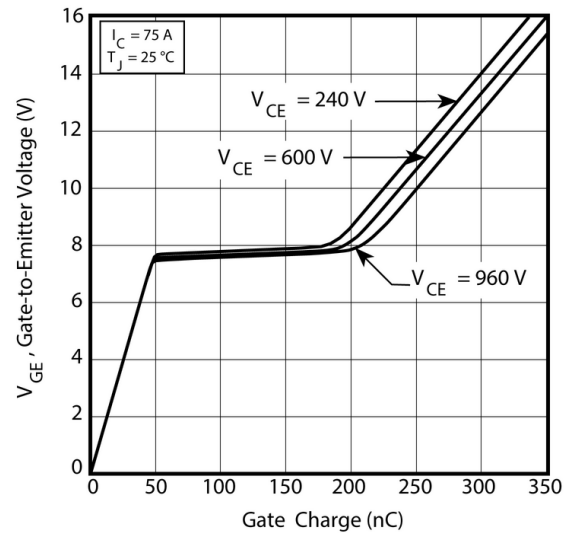


Figure 1-5. On-State Voltage vs. Gate-to-Emitter Voltage

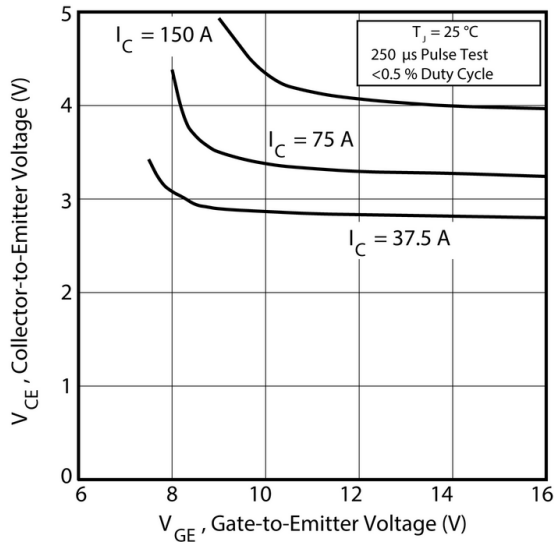


Figure 1-6. On-State Voltage vs. Junction Temperature

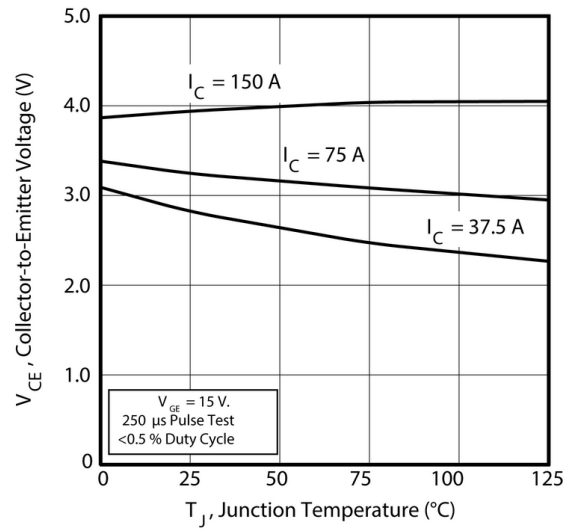


Figure 1-7. Breakdown Voltage vs. Junction Temperature

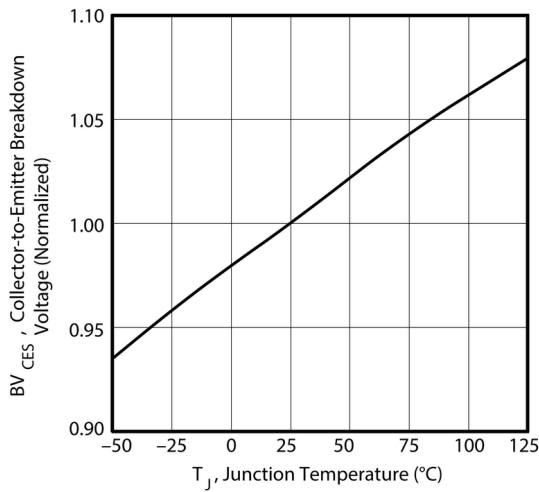


Figure 1-8. DC Collector Current vs. Case Temperature

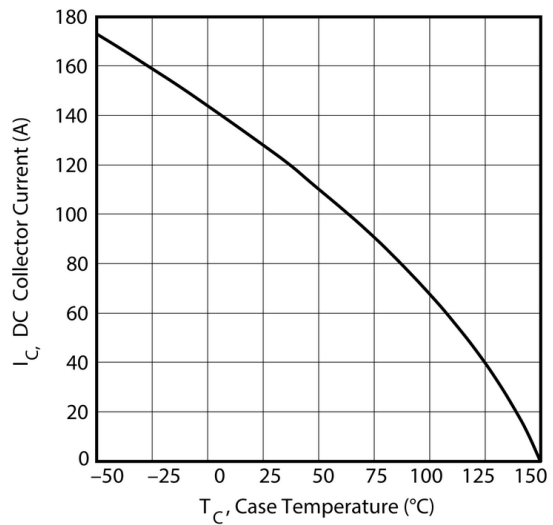


Figure 1-9. Turn-On Delay Time vs. Collector Current

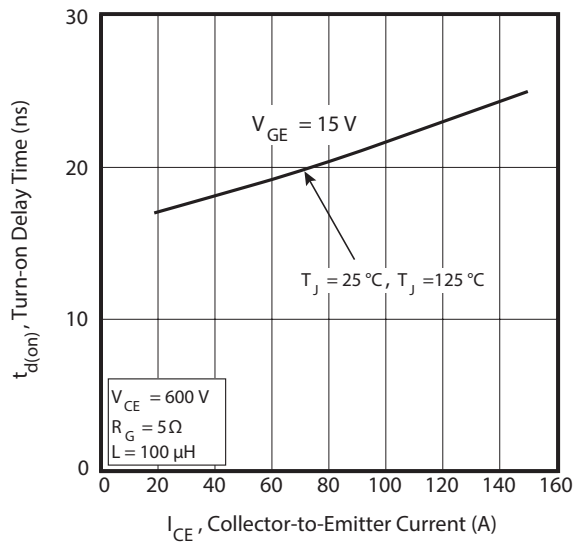


Figure 1-10. Turn-Off Delay Time vs. Collector Current

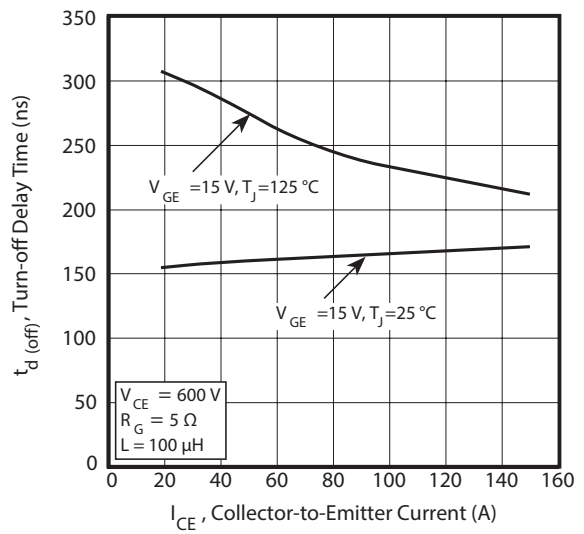


Figure 1-11. Current Rise Time vs. Collector Current

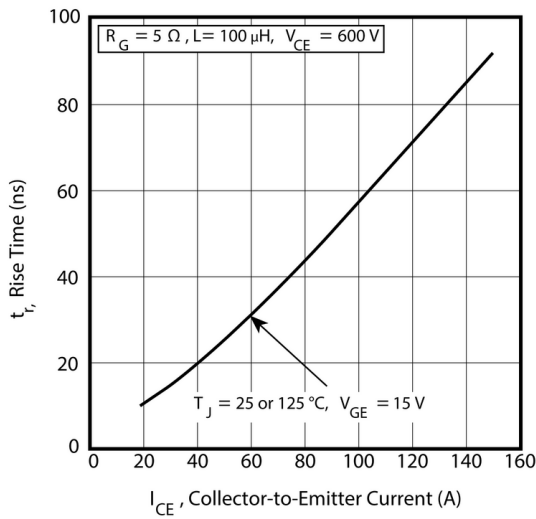


Figure 1-12. Current Fall Time vs. Collector Current

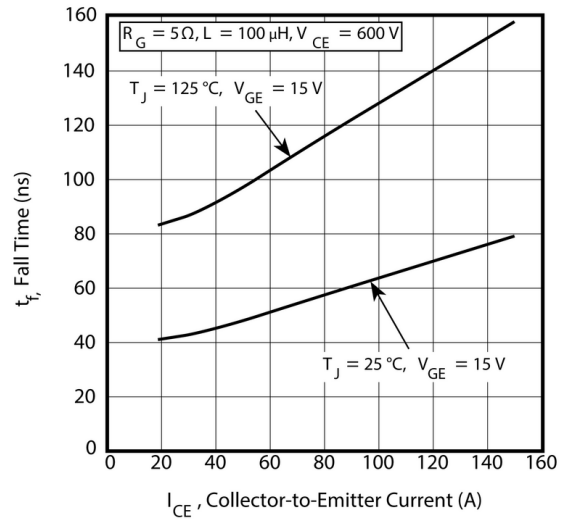


Figure 1-13. Turn-On Energy Loss vs. Collector Current

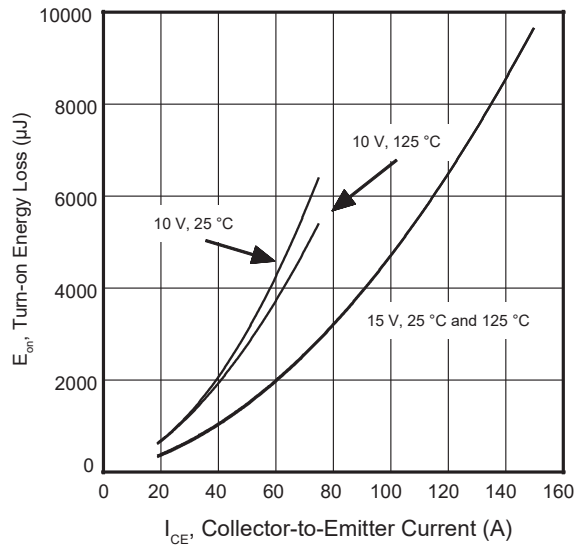


Figure 1-14. Turn-Off Energy Loss vs. Collector Current

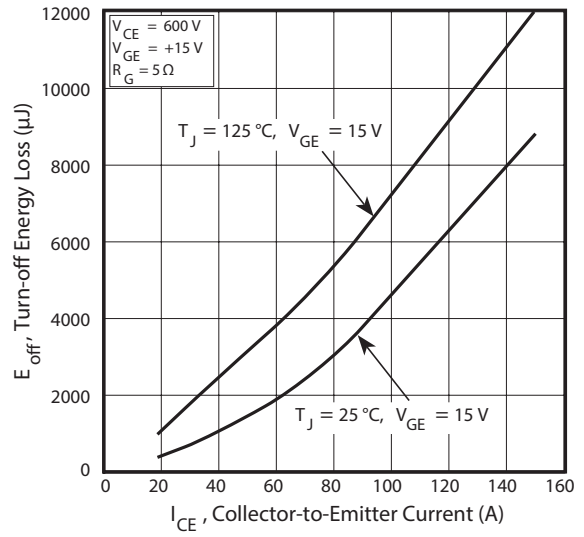


Figure 1-15. Switching Energy Losses vs. Gate Resistance

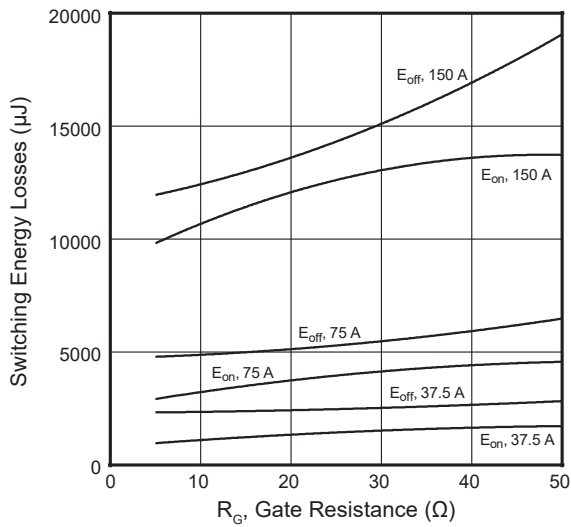


Figure 1-16. Switching Energy Losses vs. Junction Temperature

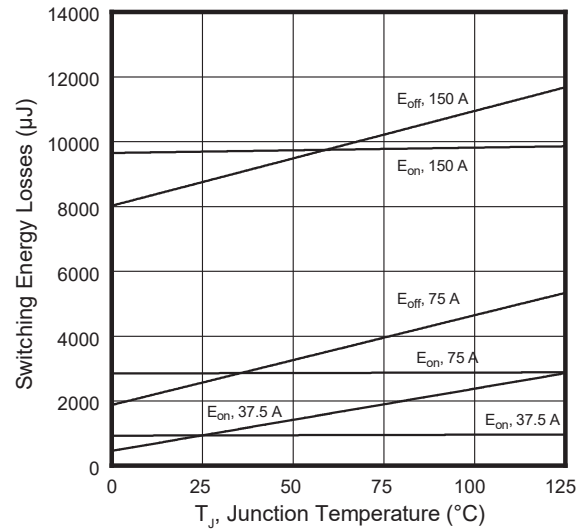


Figure 1-17. Capacitance vs. Collector-To-Emitter Voltage **Figure 1-18. Reverse-bias Safe Operating Area**

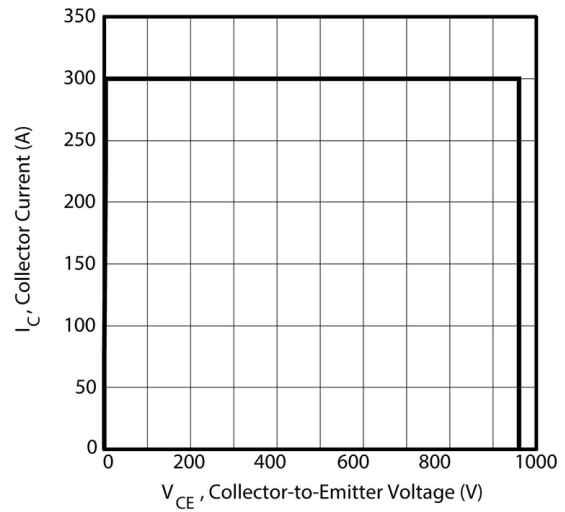
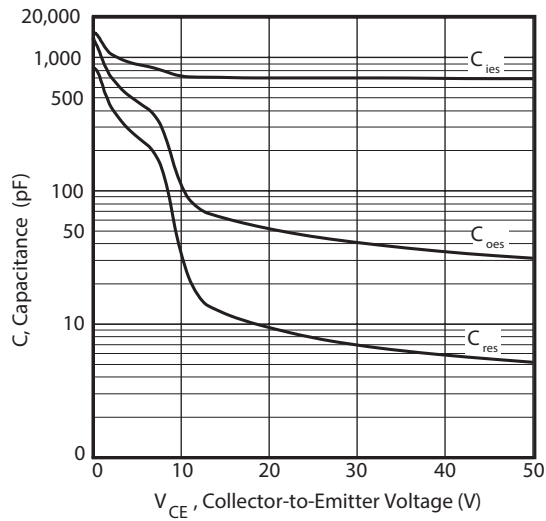


Figure 1-19. Maximum Transient Thermal Impedance

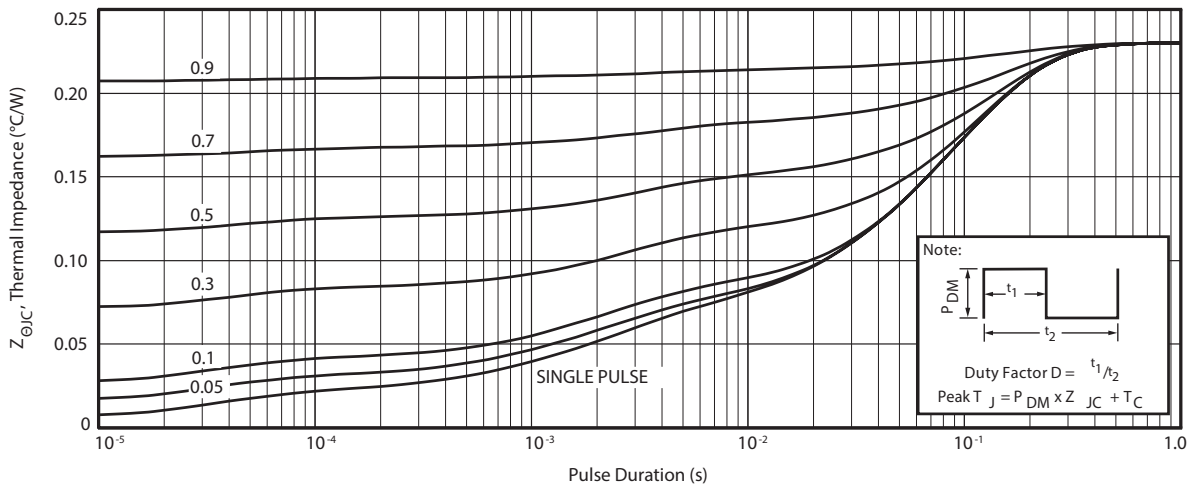


Figure 1-20. Transient Thermal Impedance Model

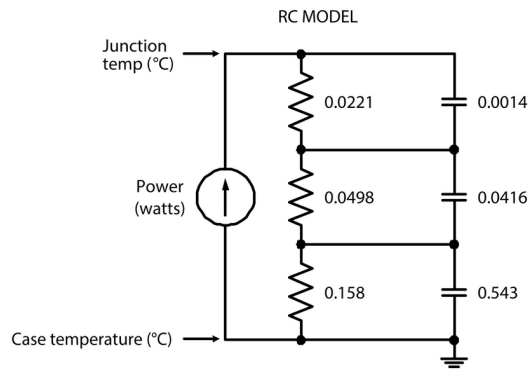


Figure 1-21. Operating Frequency vs. Collector Current

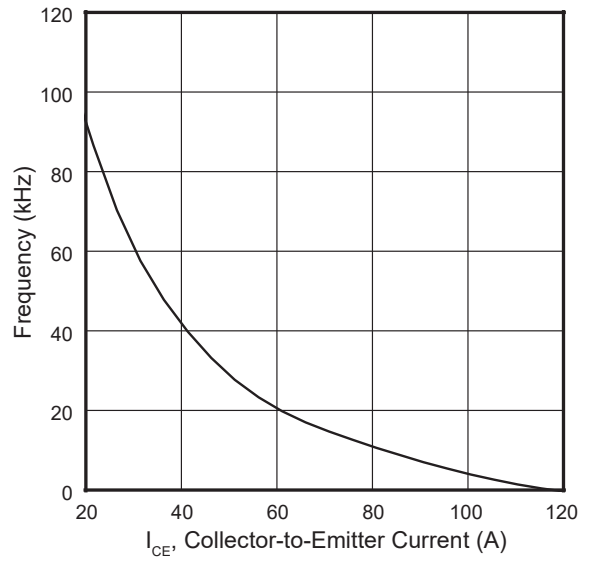


Figure 1-22. Inductive Switching Test Circuit

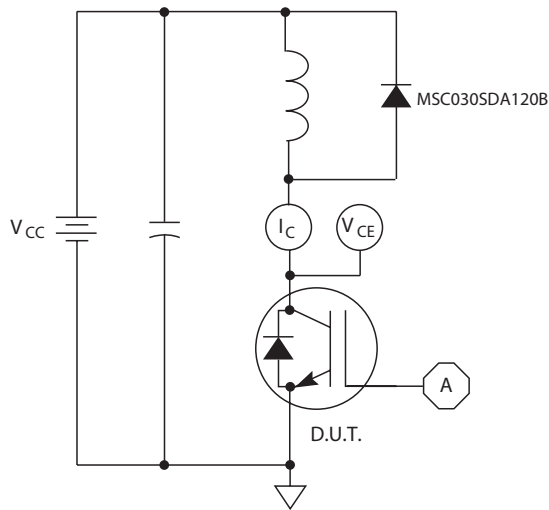


Figure 1-23. Turn-on Switching Waveforms and Definitions

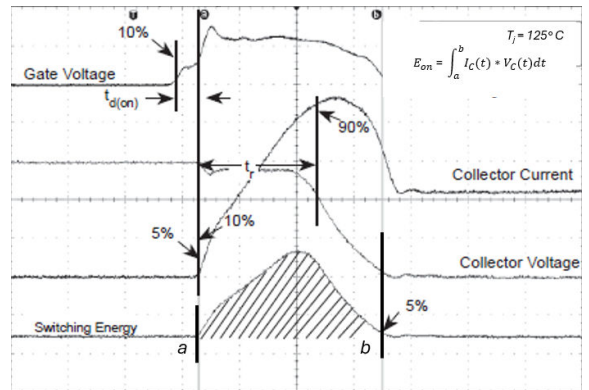
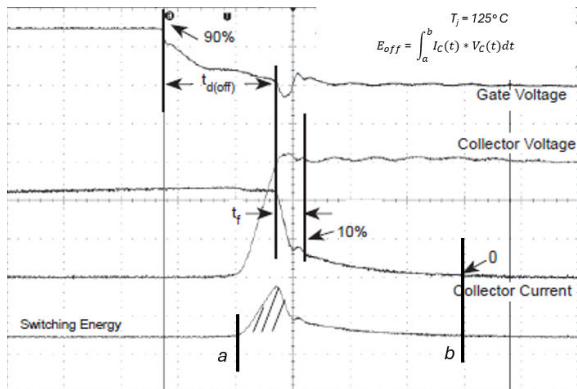


Figure 1-24. Turn-off Switching Waveforms and Definitions



2. Device Specifications: Zero-Recovery SiC Anti-Parallel Diode

This section shows the specifications of the co-packaged, anti-parallel diode.

2.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the anti-parallel diode. $T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_F	Maximum DC forward current ($T_C = 25\text{ }^\circ\text{C}$)	65	A
	Maximum DC forward current ($T_C = 110\text{ }^\circ\text{C}$)	30	
	Maximum DC forward current ($T_C = 135\text{ }^\circ\text{C}$)	22	
I_{FRM}	Repetitive peak forward surge current ($t_p = 8.3\text{ ms}$, half sine wave)	92	
I_{FSM}	Non-repetitive forward surge current ($t_p = 8.3\text{ ms}$, half sine wave)	165	
P_{TOT}	Total power dissipation ($T_C = 25\text{ }^\circ\text{C}$)	259	W
	Total power dissipation ($T_C = 110\text{ }^\circ\text{C}$)	112	

2.2 Electrical Performance

The following table shows the static characteristics of the anti-parallel diode.

Table 2-2. Static Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
V_F	Forward voltage	$I_F = 30\text{ A}$, $T_J = 25\text{ }^\circ\text{C}$		1.5	1.8	V
		$I_F = 30\text{ A}$, $T_J = 175\text{ }^\circ\text{C}$		2.1		

2.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 2-1. Maximum Transient Thermal Impedance

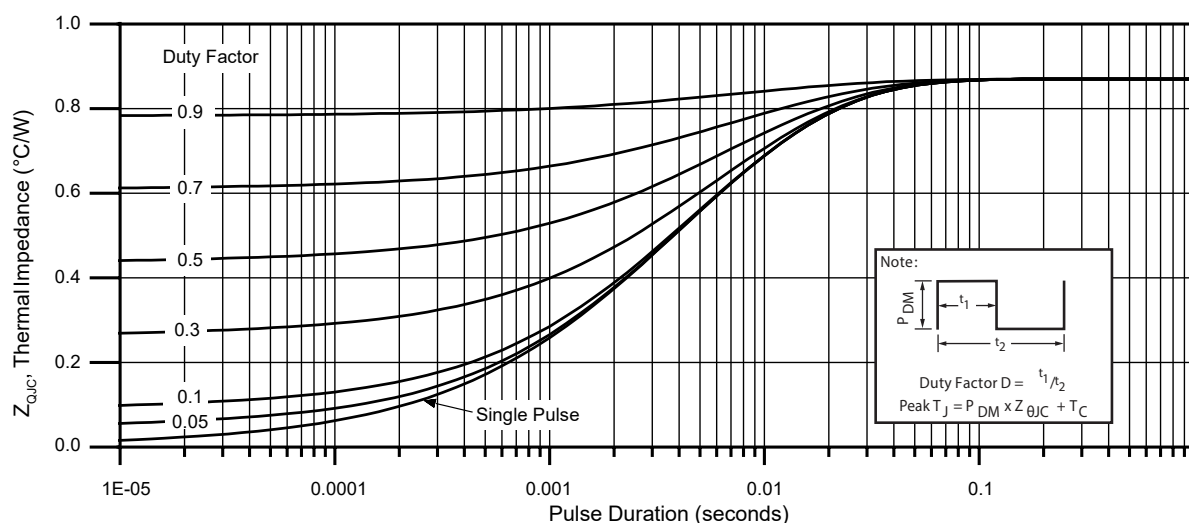


Figure 2-2. Forward Current vs. Forward Voltage

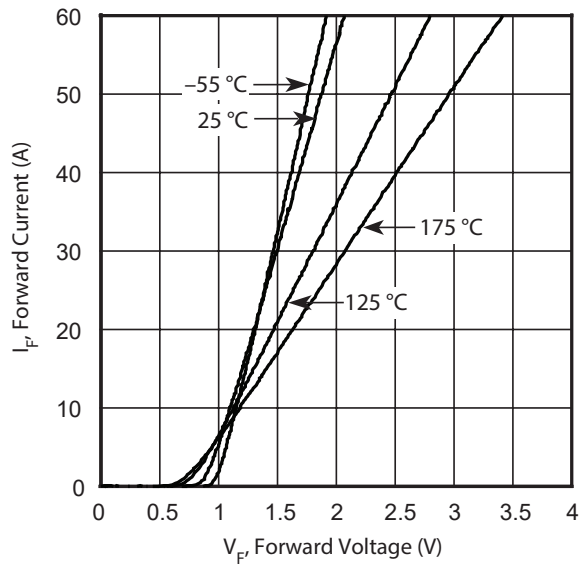


Figure 2-3. Max. Forward Current vs. Case Temp.

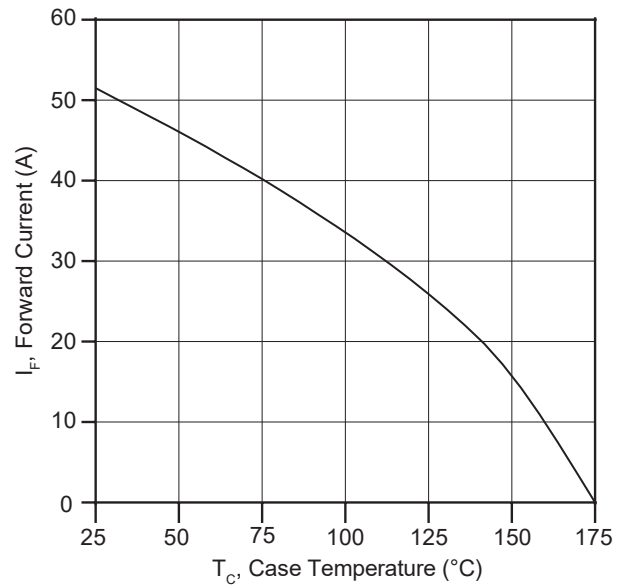


Figure 2-4. Max. Power Dissipation vs. Case Temp.

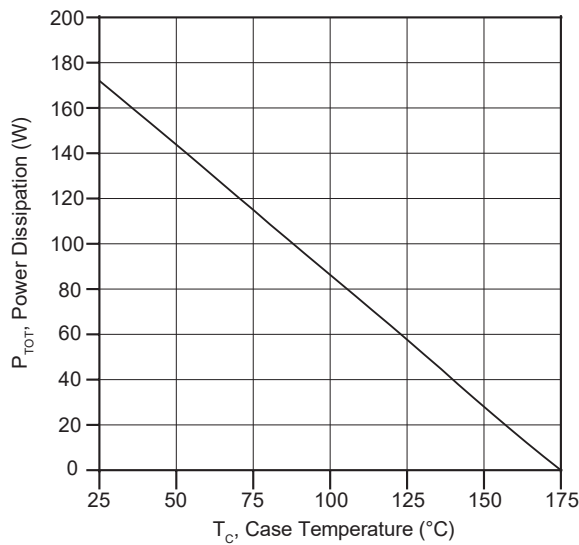


Figure 2-5. Total Capacitive Charge vs. Reverse Voltage

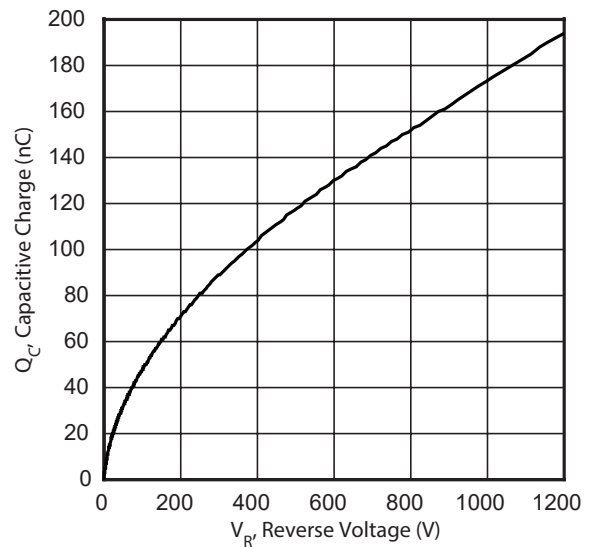
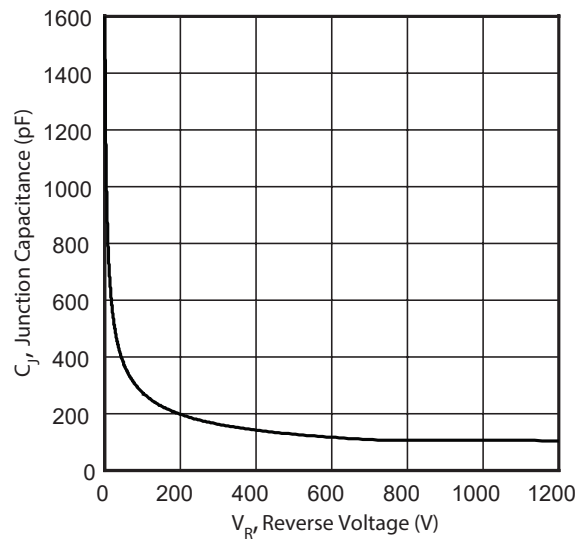


Figure 2-6. Junction Capacitance vs. Reverse Voltage

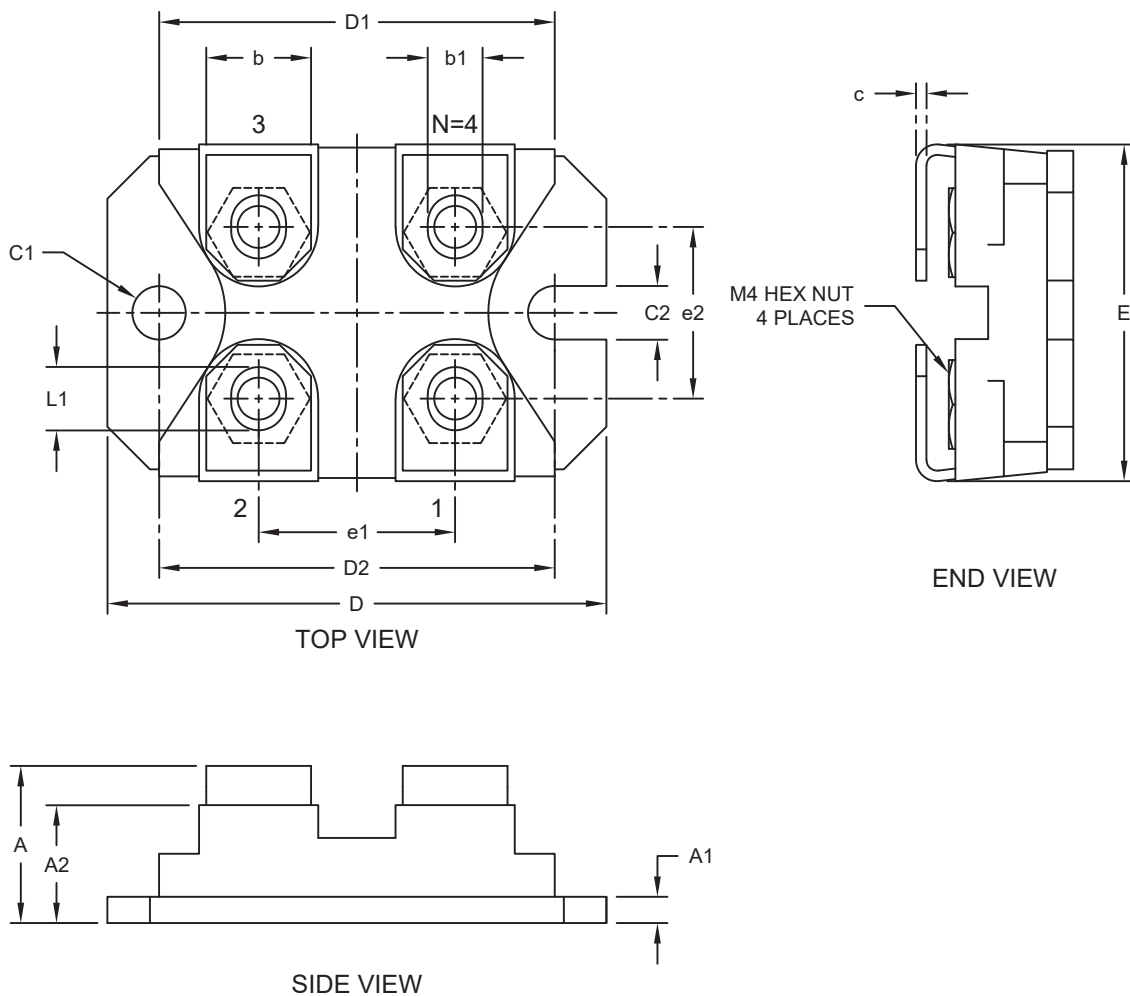
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the SOT-227 package outline of this device.

Figure 3-1. Package Outline Drawing



The following table shows the SOT-227 dimensions and should be used in conjunction with the package outline drawing.

Table 3-1. SOT-227 Dimensions

Dimension Limits		Dimensions (millimeters)	
		Min.	Max.
Number of terminals	N		4
Terminal pitch	e1	14.9	15.1
Terminal pitch	e2	12.6	12.8
Overall height	A	11.8	12.2
Base plate thickness	A1	1.95	2.14

Table 3-1. SOT-227 Dimensions (continued)

Dimension Limits		Dimensions (millimeters)	
		Min.	Max.
Molded package thickness	A2	8.9	9.6
Overall length	D	38.0	38.2
Molded package length	D1	31.5	31.7
Mounting centers	D2	30.1	30.3
Overall width	E	25.2	25.4
Terminal width	b	7.8	8.2
Terminal thickness	c	0.75	0.85
Terminal slot width	b1	4.1	4.3
Terminal slot length	L1	4.8	4.9
Mounting hole diameter	C1	4.0	4.2
Mounting slot width	C2	4.0	4.2

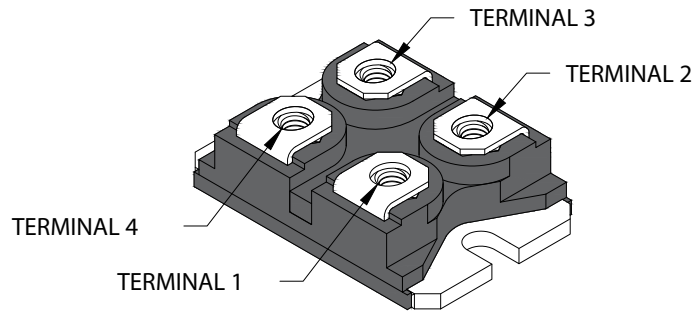
Note:

1. Dimensioning and tolerancing per ASME Y14.5M.

3.2 Terminal Pinout

The following figure illustrates the terminal pinout of this device.

Figure 3-2. Terminal Pinout



The following table shows the electrical signal terminal pinout of this device.

Table 3-2. Electrical Signal Terminal Pinout

Terminal	Definition
TERMINAL 1	Gate
TERMINAL 2	Collector, Diode Cathode
TERMINAL 3	Emitter, Diode Anode
TERMINAL 4	Emitter, Diode Anode

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	02/2025	Document created.

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