



Serial EEPROM

AT21CS Series Reset and Discovery

APPLICATION NOTE

Introduction

This application note discusses the Atmel® AT21CS Series Reset function and the AT21CS Series Discovery function. Additionally, a comparison between the Atmel Single-Wire Discovery event and the Maxim/Dallas One-Wire discovery event is discussed to facilitate the understanding of which device type is on the bus.

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1. Overview

1.1. Atmel Single-Wire Protocol and the AT21CS Series

The AT21CS Series has only two pins, GND and SI/O. The SI/O pin is the only signal between the Master microcontroller and the Slave (the AT21CS Series) hence the name Atmel Single-Wire. The SI/O signal is pulled high using an external pull-up resistor that is tied to the Master's power source. The SI/O signal must idle (rest) at a high state due to the pull up. The open collector (open drain) Master I/O port pin must signal the Slave by pulling SI/O low as seen in the Atmel Single-Wire protocol. Since there is no reset signal pin, the Reset event is achieved as defined in the Atmel Single-Wire protocol. Even though there is no V_{CC} (power pin), the AT21CS Series extracts power from the Atmel Single-Wire protocol sent to it. Data sent to the device over the Single-Wire bus is interpreted by the state of the SI/O pin during specific time intervals or slots.

1.2. Device Reset/Power-up and Discovery Response

A Reset and Discovery Response sequence is used by the Master to reset the device, as well as to perform a general bus call to determine if any devices are present on the bus. This sequence is comprised of two events, a Reset/Discharge event followed by a Discovery query.

The AT21CS Series responds to the Discovery query if the SI/O signal was previously held low for a sufficient amount of time to create a Reset event or a Discharge event. The Reset event is needed to enable the Discovery response from the AT21CS Series as defined in the Atmel Single-Wire protocol. If the AT21CS Series is busy internally executing a command, the Reset event is ignored, and therefore the device does not respond to the Discovery query. The application firmware should utilize the Reset event if the system experienced uncontrolled power brown out events while the device was idle. After power has stabilized, a forced Reset event guarantees the device is ready for operation.

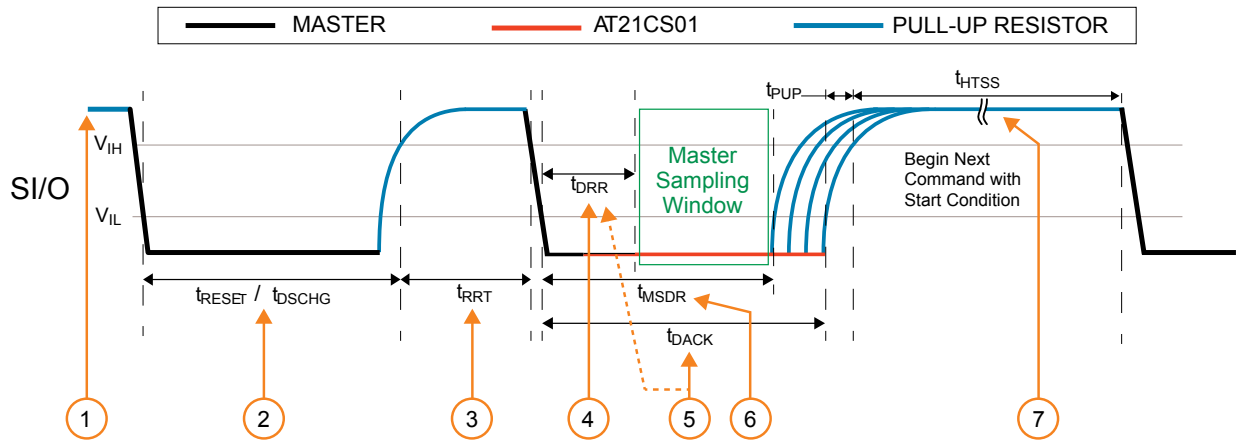
A Discharge event also enables the Discovery response from the AT21CS Series. The Discharge event requires the Master to hold SI/O low for a longer time than for the Reset event. The Discharge event is utilized to override the internal busy state of the device by depleting the internally stored charge necessary for device internal operation.

Note: A Discharge event immediately stops completion of any internal operation. The user should not expect the interrupted operation to have been completed properly. Atmel recommends utilizing only the Discharge event to immediately stop any internal AT21CS Series operations.

The AT21CS Series Discovery response is a feature that distinguishes Atmel Single-Wire devices from other One-Wire protocol devices on the market. The Atmel AT21CS Series Discovery sequence is detailed in the AT21CS Series datasheet. Atmel recommends utilizing this sequence if the system has a mix of One-Wire protocol devices.

2. Atmel Single-Wire Reset/Discharge and Discovery Response Waveform

Figure 2-1. Reset and Discovery Response Waveform



When the system first powers up, the AT21CS Series is in a standby mode waiting for the Master to send the Discovery protocol.

- Event 1** The S/I/O signal is pulled high by the pull up resistor. At power-up, S/I/O follows the V_{CC} ramp-up waveform. This waveform begins after system power is stable.
- Event 2** Master initiates a reset by holding S/I/O low for t_{RESET} , and then releasing S/I/O (stop driving low). Alternately, the Master can hold S/I/O low for t_{DSCHG} to interrupt an internal operation, and then release S/I/O.
- Event 3** S/I/O transitions to the high state after the Master releases S/I/O. After the time specified by t_{RRT} (Reset Recovery Time), the Master drives S/I/O low to request a Discovery Response Acknowledge from the slave device.
- Event 4** The Master continues holding S/I/O low for during the entire t_{DRR} interval.
- Event 5** The slave device detects S/I/O low within the t_{DRR} interval and concurrently holds S/I/O low for t_{DACK} . The slave device releases S/I/O after t_{DACK} .
- Event 6** The Master samples S/I/O state at t_{MSDR} . Since t_{DACK} is longer than t_{MSDR} , the Master sees the correct state on S/I/O before the Slave device releases S/I/O at the end of t_{DACK} . A low inside this window means that the Slave AT21CS Series is present on the bus.
- Event 7** The Master must wait for t_{HTSS} to create a Start condition before continuing with the first command.

The Atmel AT21CSMK100 Single-Wire Memory Product Evaluation Kit was utilized to make oscilloscope captures to illustrate the AT21CS01 reset/discovery response. The duration of the measured datasheet parameters are seen in the waveform measurement window to the top right of a capture.

Note: The DC low level when the Atmel AT90USB1287 host microcontroller in the AT21CSMK100 Kit is driving the S/I/O bus low is slightly higher (still a good V_{IL} level) than when the AT21CS is driving S/I/O low. This is due to the I/O driver strength of the host and the slave. The waveforms were made at pins 5 (S/I/O) and 9 (GND) of the AT21CSMK100 Kit slave socket board.

Figure 2-2. Datasheet t_{RESET} / t_{DSCG} Measurement

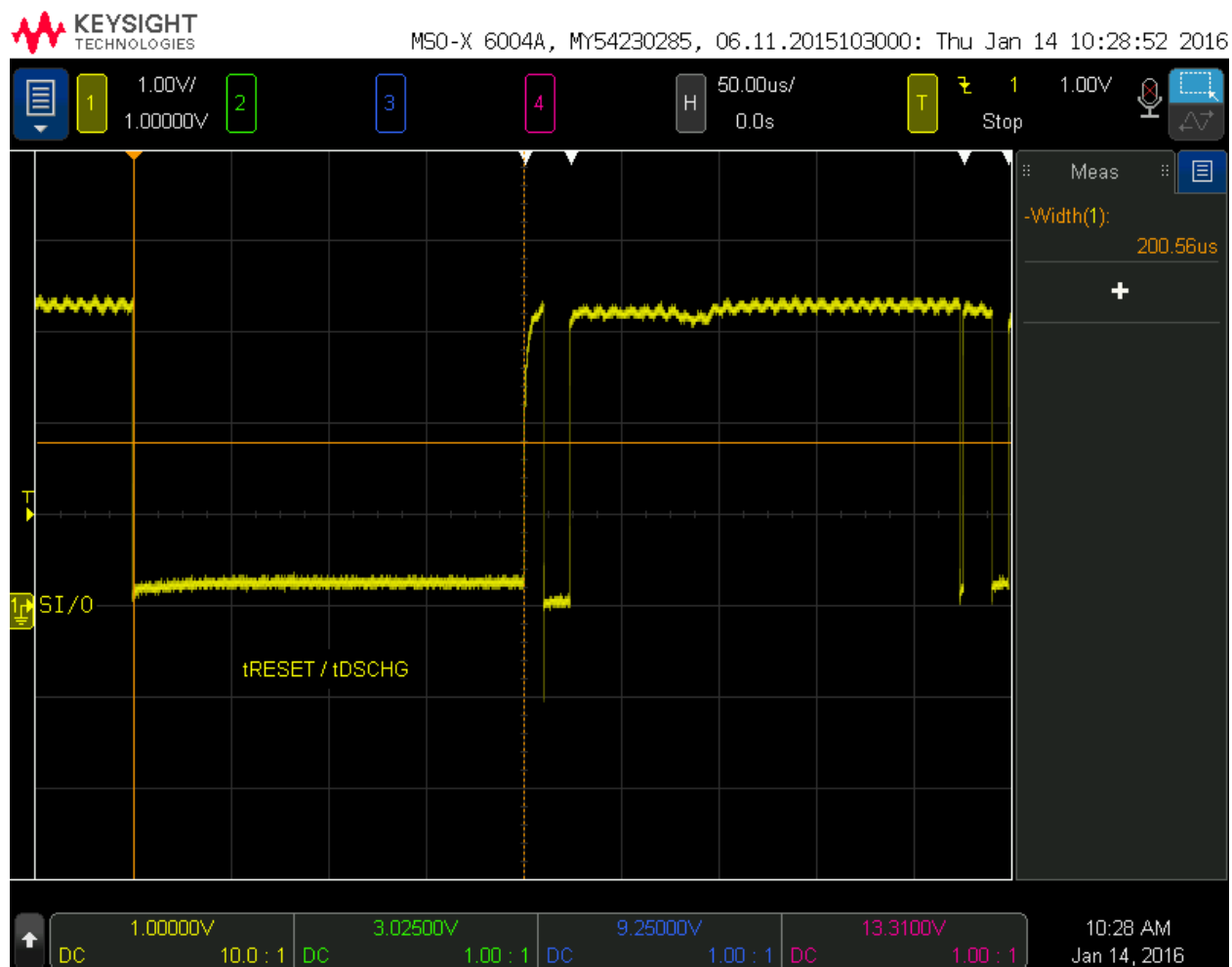


Figure 2-3. Datasheet t_{RRT} Measurement

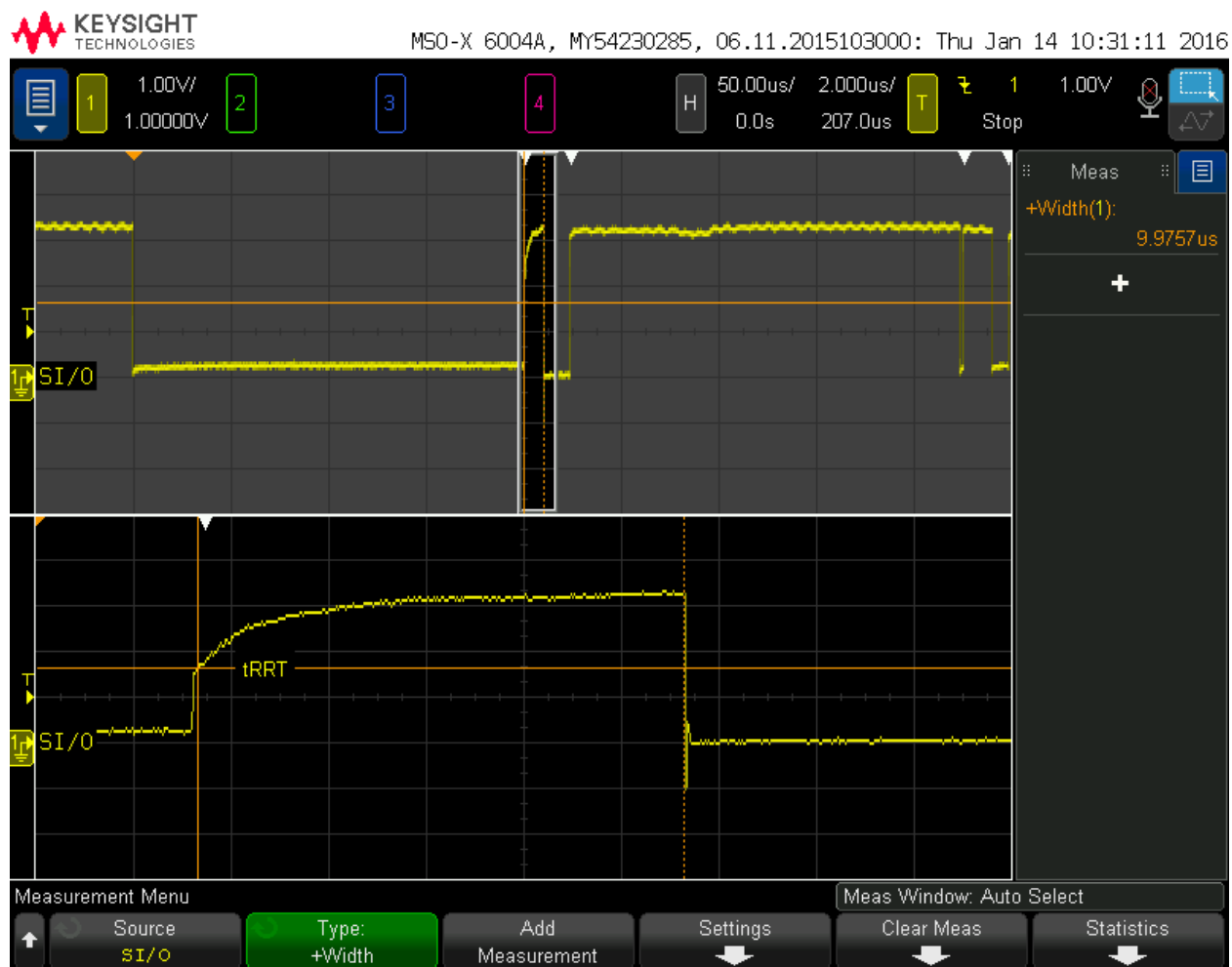
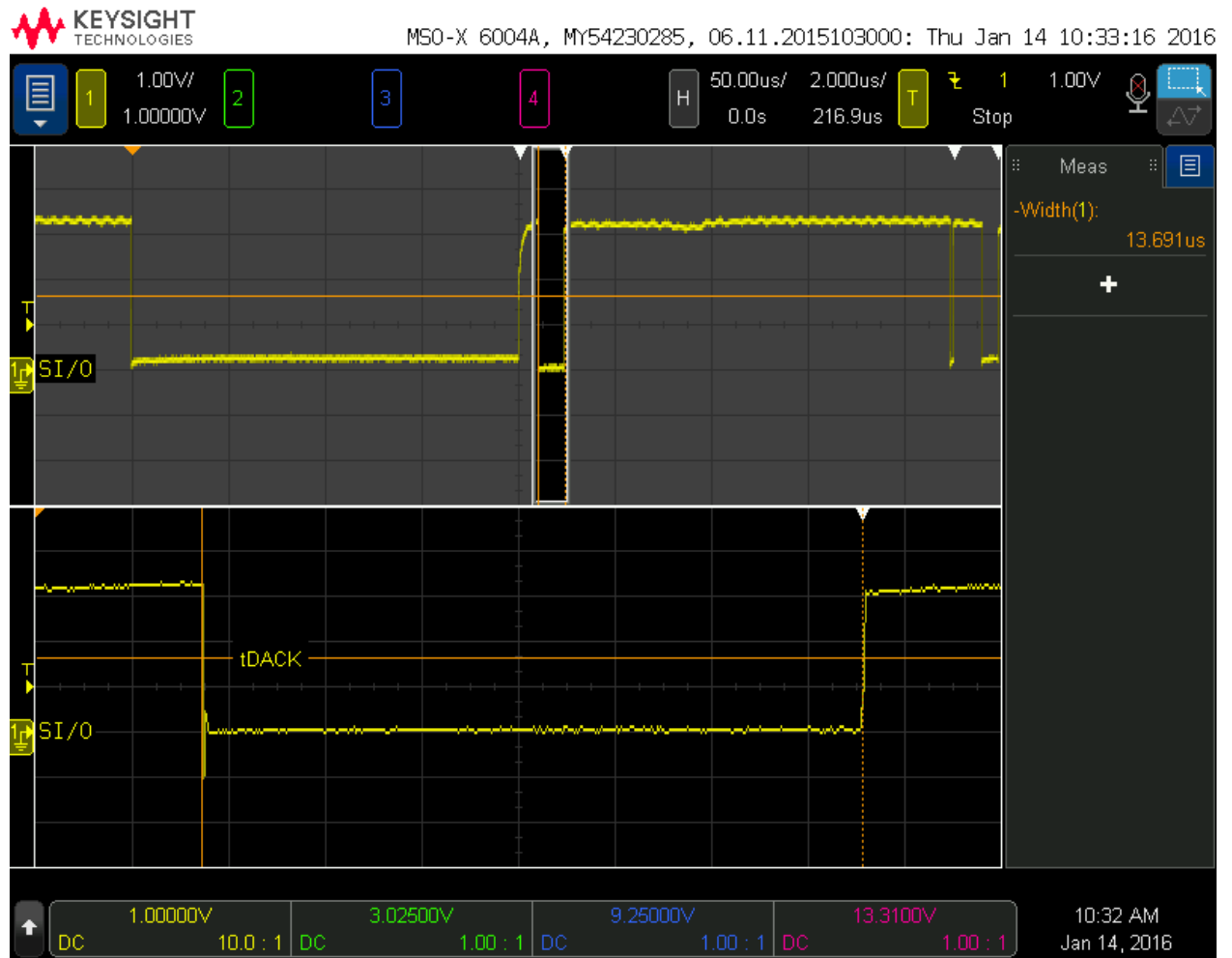


Figure 2-4. Datasheet t_{DACK} Measurement



3. Atmel Single-Wire and Maxim One-Wire Discovery Difference

When initiating communications with both an Atmel Single-Wire device and a Maxim One-Wire device, the Master must drive the I/O signal low (reset/discharge) to begin the Discovery query. After the I/O signal is driven low for the required reset/discharge time, the Master releases the I/O signal. The Atmel device expects the Master to initiate a low on the I/O signal to query for a Discovery Response in comparison to the Maxim device which initiates the low I/O signal to acknowledge it is present on the bus. Therefore, the Master can easily determine which single-wire slave is on the bus by sampling the state of the I/O signal within t_{MSDR} . If the Master initiated the low on the I/O signal and Atmel is present, the I/O signal is low. If the Master did not initiate the low on the I/O signal and the I/O signal is low, Maxim is present.

Figure 3-1. Single-Wire and Maxim One-Wire Discovery Flow

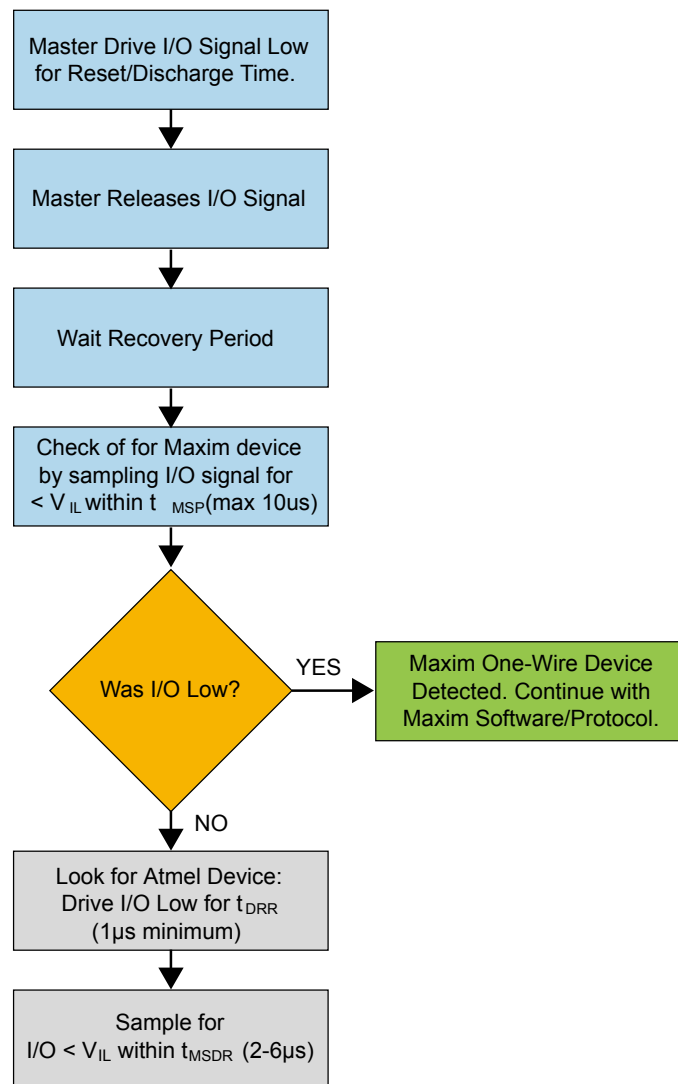


Table 3-1. Reset and Discovery Response Timing

Symbol	Parameter and Condition	Standard Speed ⁽¹⁾		High Speed		Units
		Min	Max	Min	Max	
t _{RESET}	Reset Low Time, Device in Inactive State	480	—	48	—	μs
t _{DSCHG}	Discharge Low Time, Device in Active Write Cycle (t _{WR})	150	—	150	—	μs
t _{RRT}	Reset Recovery Time	N/A	N/A	8	—	μs
t _{DRR}	Discovery Response Request	N/A	N/A	1	2 - t _{PUP} ⁽²⁾	μs
t _{DACK}	Discovery Response Acknowledge Time	N/A	N/A	8	24	μs
t _{MSDR}	Master Strobe Discovery Response Time	N/A	N/A	2	6	μs
t _{HTSS}	SI/O High Time for Start / Stop Condition	N/A	N/A	150	—	μs

Note:

1. Due to the fact that the device defaults to High Speed Mode upon reset, the Reset and Discovery Response Timing after t_{RESET} does not apply for Standard Speed Mode. High Speed Mode timing applies in all cases after t_{RESET}.
2. t_{PUP} is the time required once the SI/O line is released to be pulled up from V_{IL} to V_{IH}. This value is application specific and is a function of the loading capacitance on the SI/O line as well as the R_{PUP} chosen.
3. AC measurement test conditions for the table above:
 - Loading capacitance on SI/O: 100pF
 - R_{PUP} (bus line pull-up resistor to V_{PUP}): 1kΩ; V_{PUP}: 2.7V

4. Revision History

Doc Rev.	Date	Comments
A	02/2016	Initial document release.

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