

2.5V/3.3V 1:10 Differential LVPECL/LVECL/HSTL Clock Driver

Features

- 2.5V and 3.3V Power Supply Options
- Ensured AC Parameters over Temperature:
 - $f_{MAX} = 3 \text{ GHz}$
 - $<25 \text{ ps}$ Output-to-Output Skew
 - $<250 \text{ ps}$ t_r/t_f
 - $<400 \text{ ps}$ Propagation Delay
- Wide Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Differential Design
- VBB Output for Single-Ended Input Applications
- Fully Compatible with Industry-Standard 100K I/O Levels
- Available in 32-Lead TQFP Package

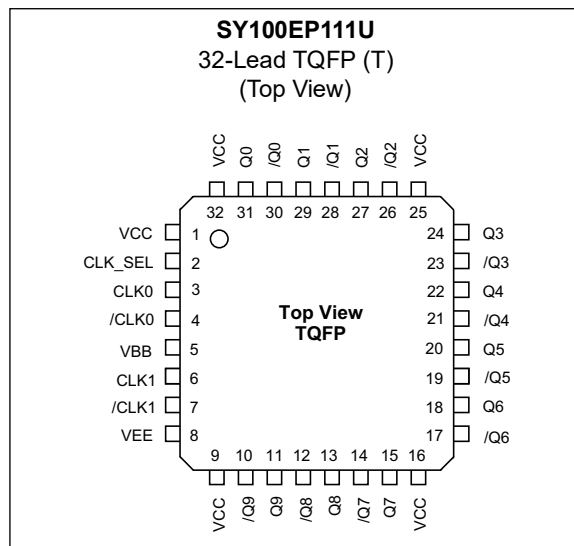
General Description

The SY100EP111U is a high-speed, low skew 1-to-10 differential fanout buffer designed for clock distribution in new, high-performance systems. The internal 2:1 MUX allows the input to select between two differential clock sources.

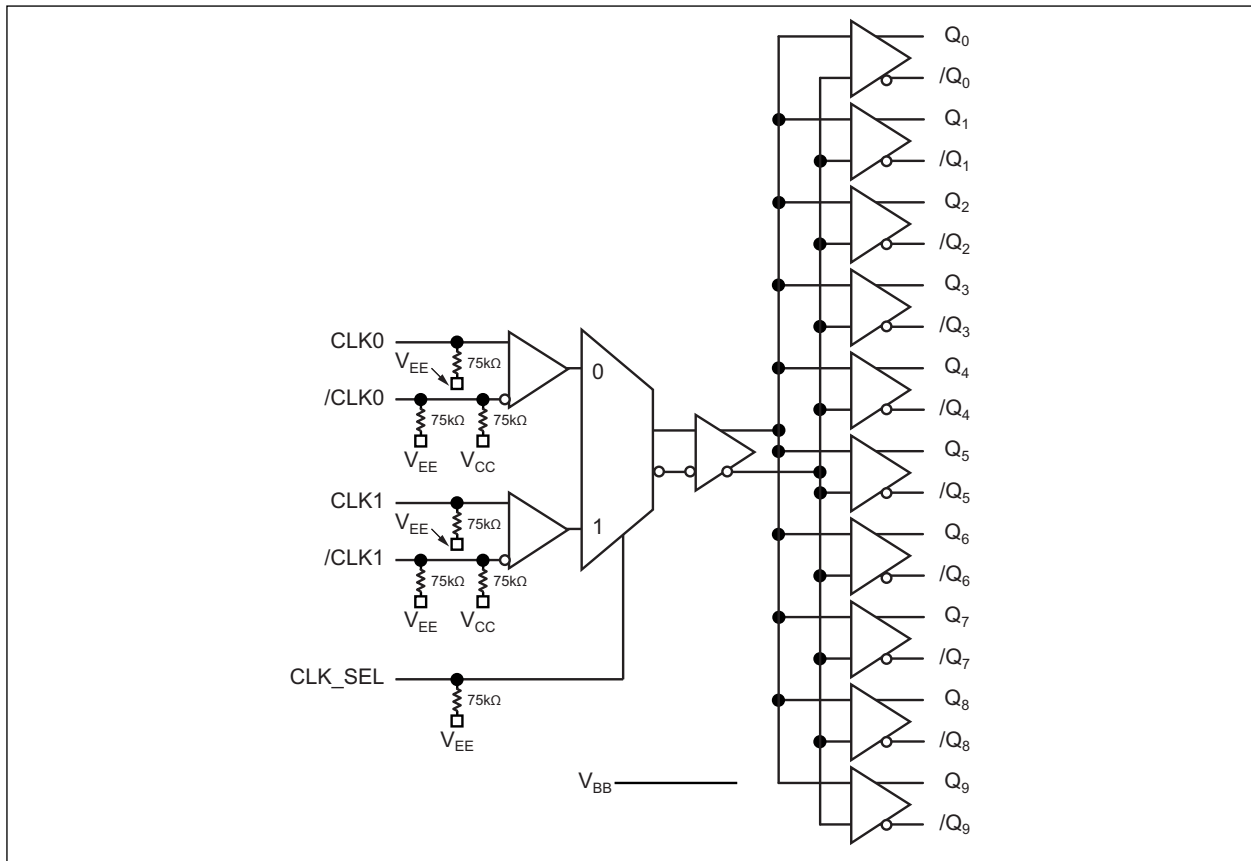
The device is specifically designed for low skew. The interconnect scheme and metal layout are carefully optimized for minimal gate-to-gate skew within the device. Wafer characterization and process control ensure consistent distribution of propagation delay from lot to lot.

The VBB output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using VBB for this purpose, it is recommended that VBB is decoupled to VCC via a $0.01 \mu\text{F}$ capacitor.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage ($V_{CC} - V_{EE}$).....	+6.0V
Input Voltage ($V_{CC} = 0V$, V_{IN} not more negative than V_{EE}).....	-6.0V to 0V
Input Voltage ($V_{EE} = 0V$, V_{IN} not more negative than V_{CC}).....	+6.0V to 0V
Continuous Output Current (I_{OUT}).....	50 mA
Surge Output Current (I_{OUT})	100 mA
Source or Sink Current on VBB Pin (I_{BB} Note 1)	±0.5 mA

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Due to the limited drive capability, use for input of the same package only.

DC ELECTRICAL CHARACTERISTICS

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	2.375	—	3.8	V	LVPECL
		-3.8	—	-2.375	V	LVECL
Power Supply Current	I_{EE}	—	55	120	mA	$T_A = -40^\circ\text{C}$
		—	70	120		$T_A = +25^\circ\text{C}$
		—	85	120		$T_A = +85^\circ\text{C}$
Input High Current	I_{IH}	—	—	150	μA	$V_{IN} = V_{IH}$
Input Low Current	I_{IL}	0.5	—	—	μA	CLK0, CLK1; $V_{IN} = V_{IL}$
		-150	—	—		/CLK0, /CLK1; $V_{IN} = V_{IL}$
Input Capacitance	C_{IN}	—	2	—	pF	—

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained.

LVPECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V \pm 10\%$, $V_{EE} = 0V$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2135	—	2420	mV	Single-Ended
Input Low Voltage	V_{IL}	1355	—	1675	mV	Single-Ended
Output Low Voltage	V_{OL}	1355	1480	1605	mV	50Ω to $V_{CC} - 2V$
Output High Voltage	V_{OH}	2155	2280	2405	mV	50Ω to $V_{CC} - 2V$
Reference Voltage	V_{BB}	1775	1875	1975	mV	Note 2
Input High Voltage Common Mode Range	V_{IHCMR}	1.2	—	V_{CC}	V	Note 3

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output varies 1:1 with V_{CC} .

2: Single-ended input operation is limited $V_{CC} \geq 3.0V$ in LVPECL mode. V_{BB} reference varies 1:1 with V_{CC} .

3: $V_{IHCMR(MIN)}$ varies 1:1 with V_{EE} , $V_{IHCMR(MAX)}$ varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

LVPECL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	1335	—	1620	mV	Single-Ended
Input Low Voltage	V_{IL}	555	—	875	mV	Single-Ended
Output Low Voltage	V_{OL}	555	680	805	mV	50Ω to $V_{CC} - 2V$
Output High Voltage	V_{OH}	1355	1480	1605	mV	50Ω to $V_{CC} - 2V$
Input High Voltage Common Mode Range	V_{IHCMR}	1.2	—	V_{CC}	V	Note 2

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained. Input and output varies 1:1 with V_{CC} .

2: $V_{IHCMR(MIN)}$ varies 1:1 with V_{EE} , $V_{IHCMR(MAX)}$ varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

LVECL DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -2.375V$ to $-3.8V$, $V_{CC} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. [Note 1](#)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	-1165	—	-880	mV	Single-Ended
Input Low Voltage	V_{IL}	-1945	—	-1625	mV	Single-Ended
Output Low Voltage	V_{OL}	-1945	-1820	-1695	mV	50Ω to $V_{CC} - 2V$
Output High Voltage	V_{OH}	-1145	-1020	-895	mV	50Ω to $V_{CC} - 2V$
Reference Voltage	V_{BB}	-1525	-1425	-1325	mV	Note 2
Input High Voltage Common Mode Range	V_{IHCMR}	$V_{EE} + 1.2$		0	V	Note 3

Note 1: 100KEP circuits are designed to meet the DC specifications shown in the table above after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500 lfpm is maintained.

2: Single-ended input operation is limited $V_{EE} \leq -3.0V$ in LVECL mode.

3: $V_{IHCMR(MIN)}$ varies 1:1 with V_{EE} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

HSTL DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 2.375V$ to $3.8V$; $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	1200	—	—	mV	—
Input Low Voltage	V_{IL}	—	—	400	mV	—
Input Crossover Voltage	V_X	680	—	900	mV	—

AC ELECTRICAL CHARACTERISTICS

(LVPECL) $V_{CC} = 2.375$ to $3.8V$, $V_{EE} = 0V$; (LVECL) $V_{EE} = -2.375V$ to $-3.8V$, $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	f_{MAX}	3	—	—	GHz	Note 1
Propagation Delay (Diff.)	t_{PD}	250	350	400	ps	—
Within-Device Skew	t_{SKEW}	—	20	25	ps	Note 2
Part-to-Part Skew		—	85	150	ps	Note 3
Cycle-to-Cycle Jitter	t_{JITTER}	—	0.2	<1	ps _{RMS}	—
Minimum Input Swing	V_{PP}	150	800	1200	mV	Note 4
Output Rise/Fall Time	t_r/t_f	100	170	250	ps	20% to 80%

Note 1: Measured with 750 mV clock signal, 50% duty cycle. All loading with a 50Ω to $V_{CC} - 2.0V$.

2: Input clock to any output (Q0 to Q9); Differential.

3: Measured for same transitions.

4: See Figure 1-1.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	-65	—	+150	$^{\circ}C$	—
Lead Temperature	T_{LEAD}	—	—	+260	$^{\circ}C$	Soldering, 20 sec.
Ambient Temperature Range	T_A	-40	—	+85	$^{\circ}C$	—
Package Thermal Resistances						
Thermal Resistance, TQFP 32-Ld	θ_{JA}	—	50	—	$^{\circ}C/W$	Still-Air
		—	42	—	$^{\circ}C/W$	500 lfpm
	θ_{JC}	—	20	—	$^{\circ}C/W$	Junction-to-Case

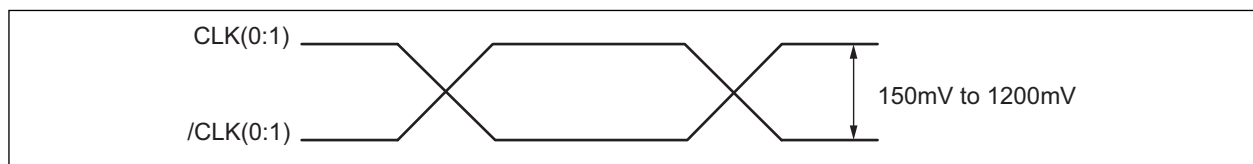


FIGURE 1-1: Timing Waveform.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

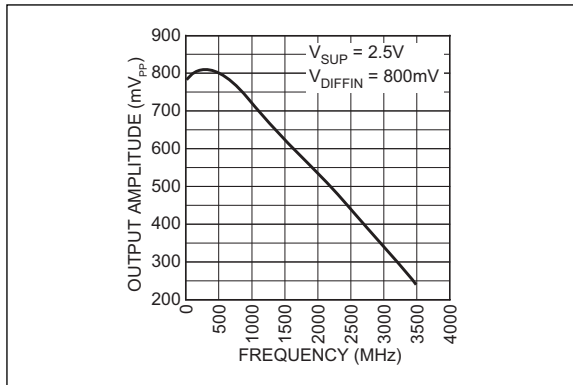


FIGURE 2-1: Frequency Response vs. Output Amplitude.

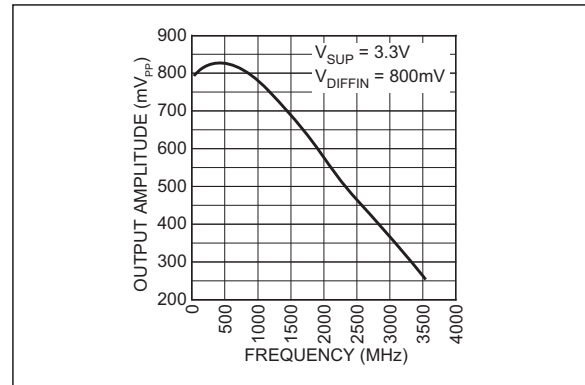


FIGURE 2-2: Frequency Response vs. Output Amplitude.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
3, 4	CLK0, /CLK0	LVPECL, LVECL, HSTL Clock Inputs: CLK0 input includes a 75 k Ω pull-down. Default is low if left floating. /CLK0 includes an internal 75 k Ω pull-up and pull-down. Default state is $V_{CC}/2$.
6, 7	CLK1, /CLK1	LVPECL, LVECL, HSTL Clock Inputs: CLK input includes a 75 k Ω pull-down. Default is low if left floating. /CLK includes an internal 75 k Ω pull-up and pull-down. Default state is $V_{CC}/2$.
31, 29, 27, 24, 22, 20, 18, 15, 13, 11	Q0 to Q9	LVPECL/LVECL Outputs.
30, 28, 26, 23, 21, 19, 17, 14, 12, 10	/Q0 to /Q9	Complementary LVPECL/LVECL Outputs.
2	CLK_SEL	LVPECL/LVECL Clock Select Input: Internal 75 k Ω resistor connected to VEE. When left floating, the default condition is LOW.
5	VBB	Reference Voltage: AC-coupled or single-ended input applications.
1, 9, 16, 25, 32	VCC	Positive Power Supply: Bypass with 0.1 μ F//0.01 μ F low ESR capacitors.
8	VEE	Negative Power Supply: For LVPECL operation, connect to GND.

TABLE 3-2: TRUTH TABLE

CLK_SEL	Active Input
0	CLK0, /CLK0
1	CLK1, /CLK1

4.0 TERMINATION RECOMMENDATIONS

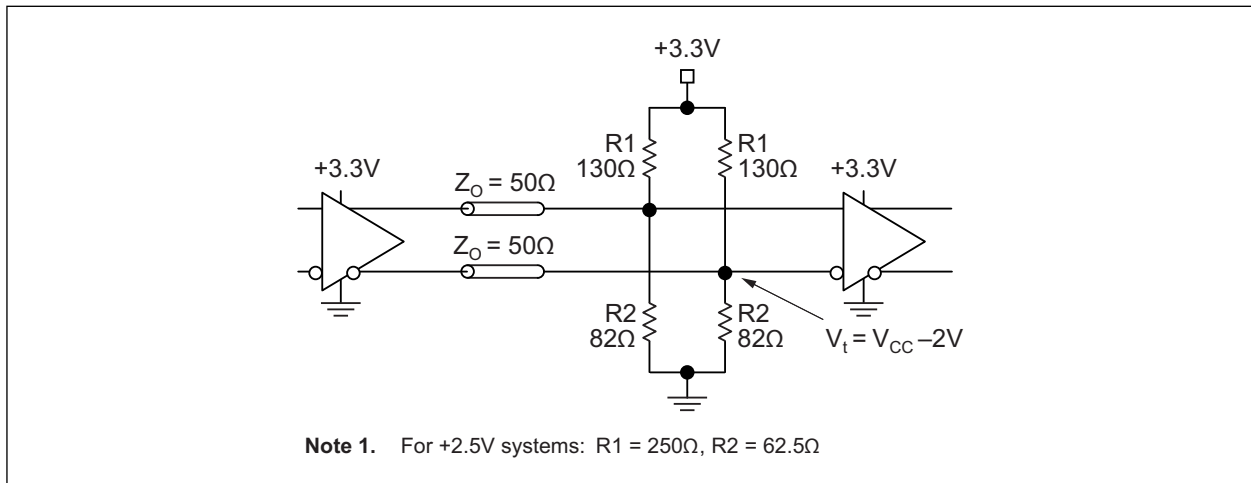


FIGURE 4-1: Parallel Termination: Thevenin Equivalent.

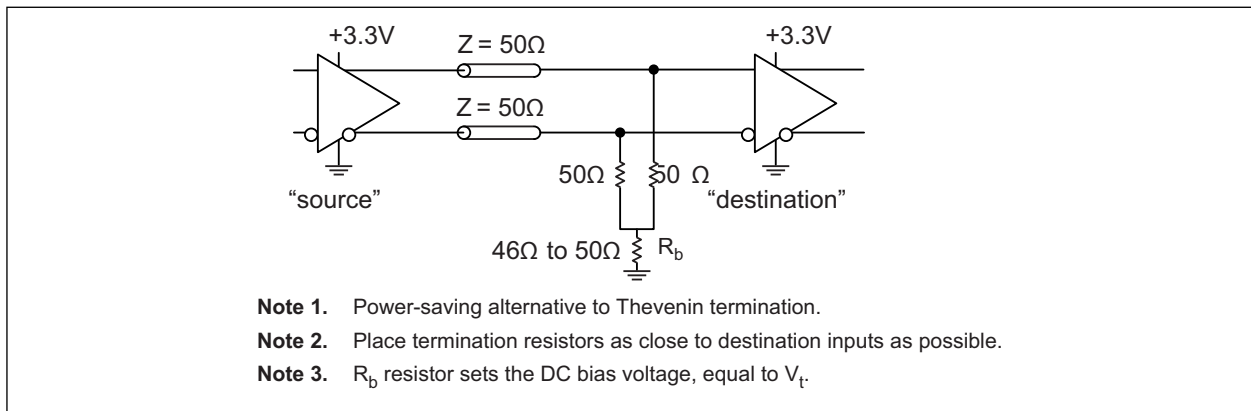


FIGURE 4-2: Parallel Termination: Three-Resistor.

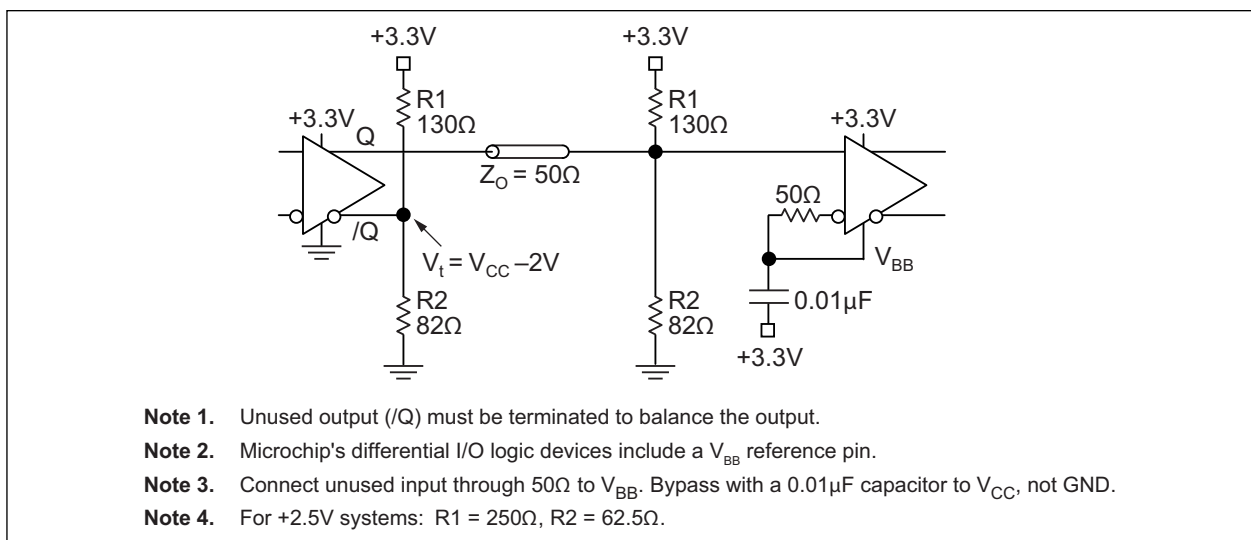
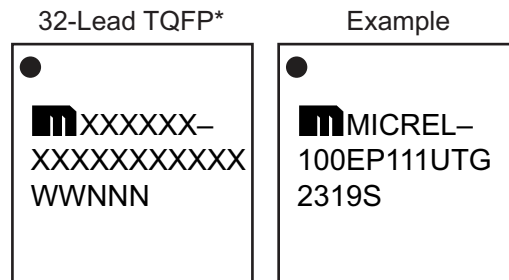


FIGURE 4-3: Terminating Unused I/O.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

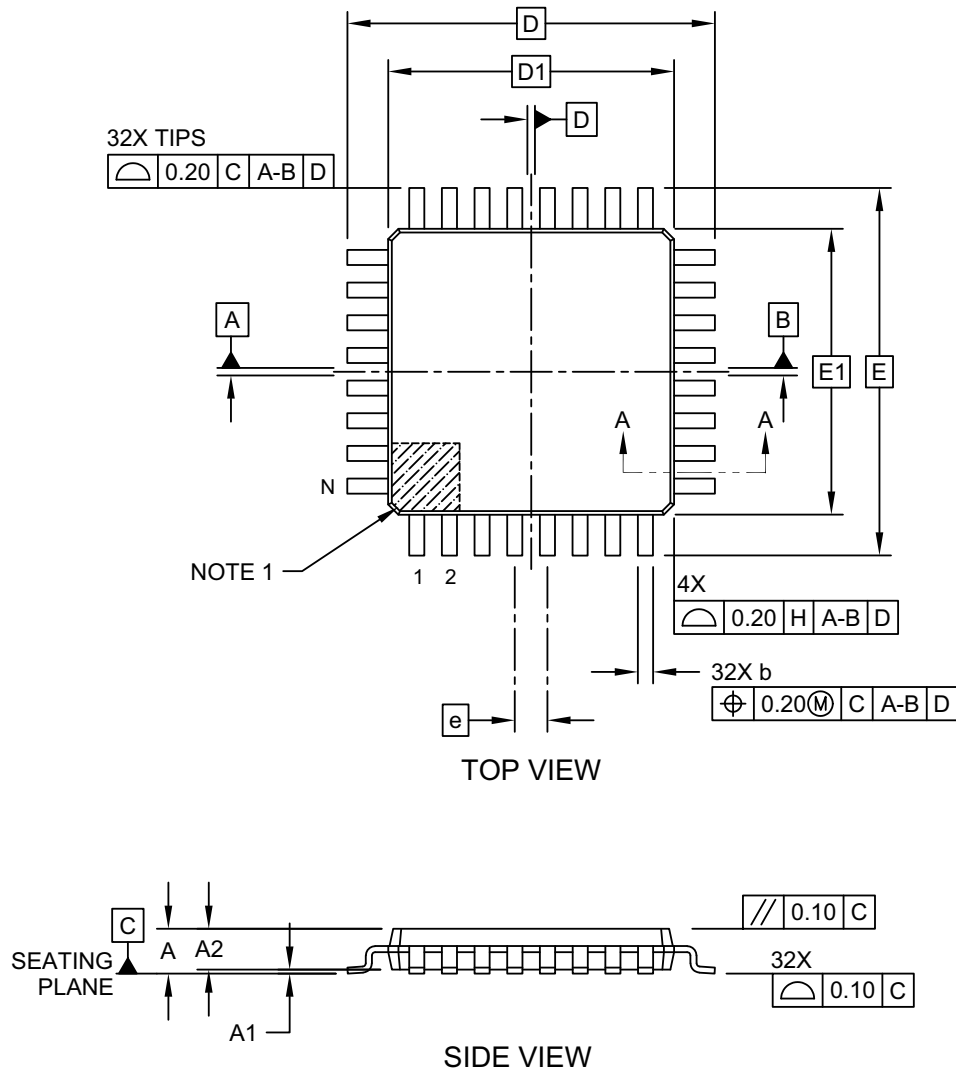


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.		

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
 6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
 2 Characters = NN; 1 Character = N

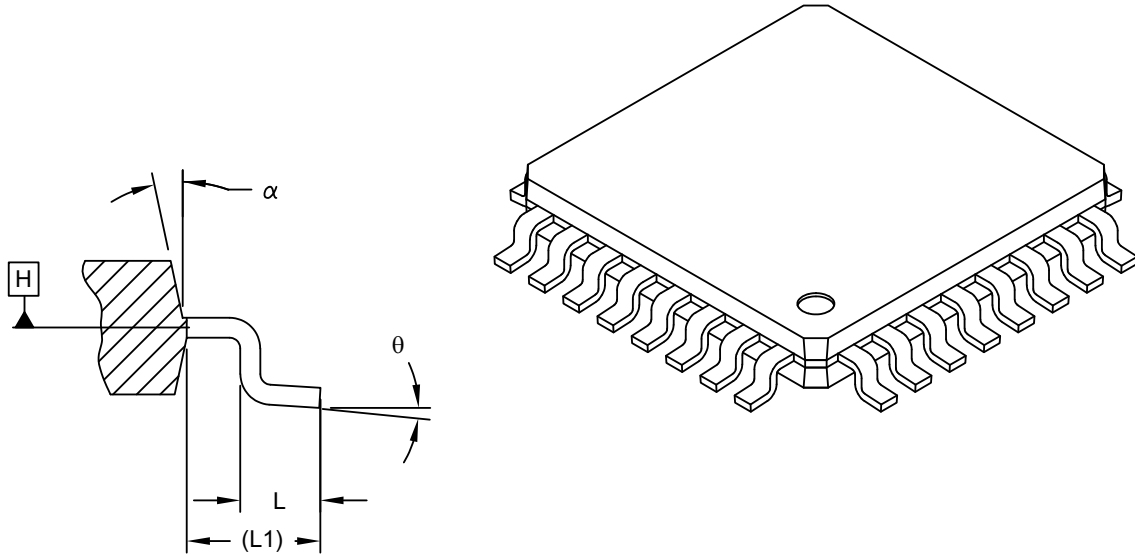
32-Lead Plastic Thin Quad Flatpack (T5X) - 7x7x1.0 mm Body [TQFP] 2.00 mm Footprint; Also Atmel Legacy Global Package Code AUT

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



32-Lead Plastic Thin Quad Flatpack (T5X) - 7x7x1.0 mm Body [TQFP] 2.00 mm Footprint; Also Atmel Legacy Global Package Code AUT

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



SECTION A-A

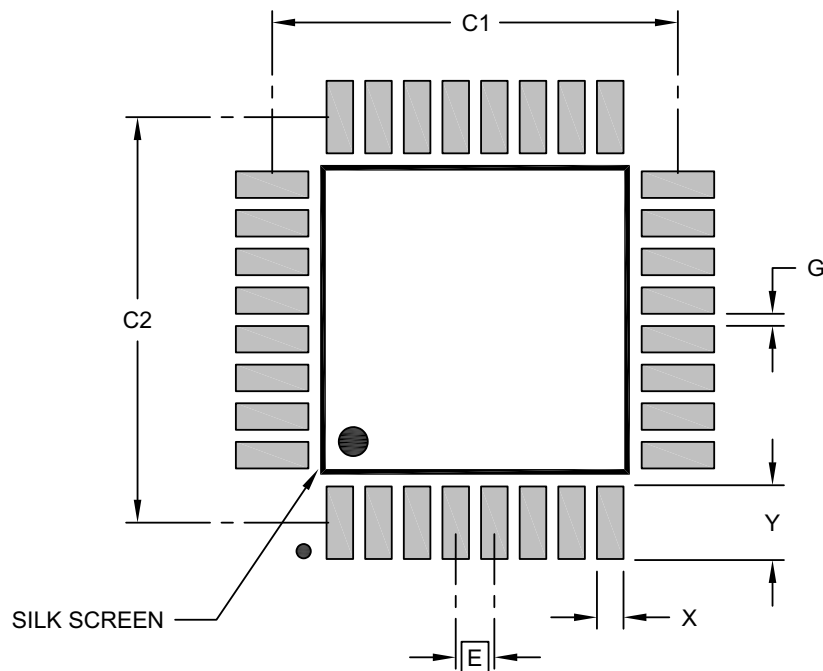
Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	32		
Lead Pitch	e	0.80 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	θ	0°	-	7°
Overall Width	E	9.00 BSC		
Overall Length	D	9.00 BSC		
Molded Package Width	E1	7.00 BSC		
Molded Package Length	D1	7.00 BSC		
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	-	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

32-Lead Plastic Thin Quad Flatpack (T5X) - 7x7x1.0 mm Body [TQFP] 2.00 mm Footprint; Also Atmel Legacy Global Package Code AUT

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X32)	X			0.55
Contact Pad Length (X32)	Y			1.55
Contact Pad to Contact Pad (X28)	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2074-T5X Rev D

APPENDIX A: REVISION HISTORY

Revision A (December 2023)

- Converted Micrel document SY100EP111U to Microchip data sheet template DS20006840A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]	Examples:
Device	Supply Voltage	Package	Temperature Range	Media Type	
Device:	SY100EP111:	2.5V/3.3V 1:10 Differential LVPECL/LVECL/HSTL Clock Driver			a) SY100EP111UTG: SY100EP111, 2.5V/3.3V Supply Voltage, 32-Lead TQFP, –40°C to +85°C Temperature Range, 250/Tray
Supply Voltage:	U	=	2.5V/3.3V		b) SY100EP111UTG-TR: SY100EP111, 2.5V/3.3V Supply Voltage, 32-Lead TQFP, –40°C to +85°C Temperature Range, 1,000/Reel
Package:	T	=	32-Lead TQFP		Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Temperature Range:	G	=	–40°C to +85°C		
Media Type:	<blank> TR	=	250/Tray 1,000/Reel		

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Note the following details of the code protection feature on Microchip products:

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