

2.5V/3.3V/5V 1:2 Differential PECL/LVPECL/ECL Fanout Buffer

Features

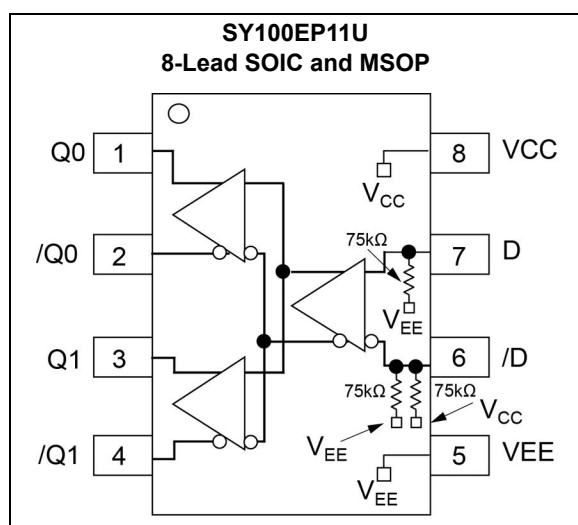
- 2.5V, 3.3V, and 5V Power Supply Options
- Ensured AC Parameters over Temperature:
 - $f_{MAX} > 3.0$ GHz
 - < 20 ps Output-to-Output Skew
 - < 200 ps t_r/t_f
 - < 360 ps Propagation Delay
- Wide Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Available in 8-Lead MSOP and SOIC Packages

General Description

The SY100EP11U is a precision, high-speed 1:2 differential fanout buffer. Having within-device skews and output transition times significantly improved over the EL11V, the EP11U is ideally suited for those applications that require exceptional AC performance.

The differential inputs of the EP11U employ clamping circuitry to maintain stability under open input conditions. If the inputs are left open, the Q outputs will go low.

Package Type



SY100EP11U

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1)	+6V
NECL Power Supply Voltage (V_{EE}) (Note 2)	–6V
PECL Mode Input Voltage (V_{IN}) (Note 3)	+6V
NECL Mode Input Voltage (V_{IN}) (Note 4)	–6V
Continuous Output Current (I_{OUT})	50 mA
Surge Output Current (I_{OUT})	100 mA

† **Notice:** Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1:** $V_{EE} = 0V$.
2: $V_{CC} = 0V$.
3: $V_{EE} = 0V, V_{IN} \leq V_{CC}$.
4: $V_{CC} = 0V, V_{IN} \geq V_{EE}$.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 2.375V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-2.375V$; $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage, PECL	V_{CC}	4.5	5.0	5.5	V	—
		2.375	—	3.8		—
Power Supply Voltage, NECL		-5.5	-5.0	-4.5		—
		-3.8	—	-2.375		—
Power Supply Current	I_{EE}	—	—	44	mA	$T_A = -40^{\circ}C$
		—	30	44		$T_A = +25^{\circ}C$
		—	—	44		$T_A = +85^{\circ}C$
Output High Voltage (Note 2)	V_{OH}	$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V	—
Output Low Voltage (Note 2)	V_{OL}	$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V	—
Input High Voltage (Single-Ended)	V_{IH}	$V_{CC} - 1.225$	—	$V_{CC} - 0.880$	V	—
Input Low Voltage (Single-Ended)	V_{IL}	$V_{CC} - 1.945$	—	$V_{CC} - 1.625$	V	—
Common Mode Range (Note 3)	V_{IHCMR}	$V_{EE} + 2.0$	—	V_{CC}	V	$V_{CC} = 4.5V$ to $5.5V$ or $V_{EE} = -5.5V$ to $-4.5V$
		$V_{EE} + 1.2$	—			$V_{CC} = 2.375V$ to $3.8V$ or $V_{EE} = -3.8V$ to $-2.375V$
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current D	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL} \text{ (Min)}$
Input Low Current /D		-150	—	—		
Input Capacitance, MSOP	C_{IN}	—	1.0	—	pF	$T_A = +25^{\circ}C$
Input Capacitance, SOIC		—	1.35	—		

Note 1: Devices are designed to meet the DC specifications shown in the table above after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2: Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$.

3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1.2V. Single-ended input D pin operation is limited to $V_{CC} \geq 3.0V$ in PECL mode, and to $V_{EE} \leq -3.0V$ in NECL mode.

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AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 2.375V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-2.375V$; $V_{CC} = 0V$;
 $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. All loading with a 50Ω resistor to $V_{CC} - 2.0V$ (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Toggle Frequency (Note 1)	f _{MAX}	3	—	—	GHz	—
Propagation Delay D to Q (Differential)	t _{PLH} , t _{PHL}	170	230	300	ps	T _A = −40°C, V _{CC} = 2.5V or V _{EE} = −2.5V
		140	200	250		T _A = −40°C, V _{CC} = 3.3/5V or V _{EE} = −3.3/−5V
		180	240	310		T _A = +25°C, V _{CC} = 2.5V or V _{EE} = −2.5V
		160	220	270		T _A = +25°C, V _{CC} = 3.3/5V or V _{EE} = −3.3/−5V
		210	270	360		T _A = +85°C, V _{CC} = 2.5V or V _{EE} = −2.5V
		180	240	300		T _A = +85°C, V _{CC} = 3.3/5V or V _{EE} = −3.3/−5V
Within-Device Skew (Note 2)	t _{SKEW}	—	5	20	ps	
Part-to-Part Skew (Note 2)		—	—	110		T _A = −40°C, +25°C V _{CC} = 2.5V or V _{EE} = −2.5V
		—	—	130		T _A = −40°C, +25°C, V _{CC} = 3.3/5V or V _{EE} = −3.3/−5V
		—	—	120		T _A = +85°C V _{CC} = 2.5V or V _{EE} = −2.5V
		—	—	150		T _A = +85°C, V _{CC} = 3.3/5V or V _{EE} = −3.3/−5V

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{CC} = 2.375V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-2.375V$; $V_{CC} = 0V$;
 $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. All loading with a 50Ω resistor to $V_{CC} - 2.0V$ (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
RMS Phase Jitter	t _{JITTER}	—	57	—	fs	625 MHz Integration Range: 12 kHz to 20 MHz
		—	117	—		156.25 MHz Integration Range: 12 kHz to 20 MHz
		—	159	—		100 MHz Integration Range: 12 kHz to 20 MHz
Additive Phase Jitter		—	52	—	fs	625 MHz Integration Range: 12 kHz to 20 MHz
		—	109	—		156.25 MHz Integration Range: 12 kHz to 20 MHz
		—	146	—		100 MHz Integration Range: 12 kHz to 20 MHz
Input Voltage Swing, Differential Configuration, (Note 3)	V _{PP}	150	800	1200	mV	—
Output Rise/Fall Time Q (20% to 80%)	t _r /t _f	70	110	170	ps	T _A = −40°C
		80	120	180		T _A = +25°C
		100	140	200		T _A = +85°C

Note 1: Measured with 750 mV input signal, 50% duty cycle.

2: Skew is measured between outputs under identical transitions.

3: Input swing for which AC parameters are ensured.

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TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	—
Storage Temperature	T_S	-65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Package Thermal Resistance (SOIC)						
Junction-to-Ambient	θ_{JA}	—	160	—	°C/W	Still Air
		—	109	—		500 lfpm
Junction-to-Case	θ_{JC}	—	39	—	°C/W	—
Package Thermal Resistance (MSOP)						
Junction-to-Ambient	θ_{JA}	—	206	—	°C/W	Still Air
		—	155	—		500 lfpm
Junction-to-Case	θ_{JC}	—	39	—	°C/W	—

2.0 ADDITIVE PHASE NOISE PLOTS

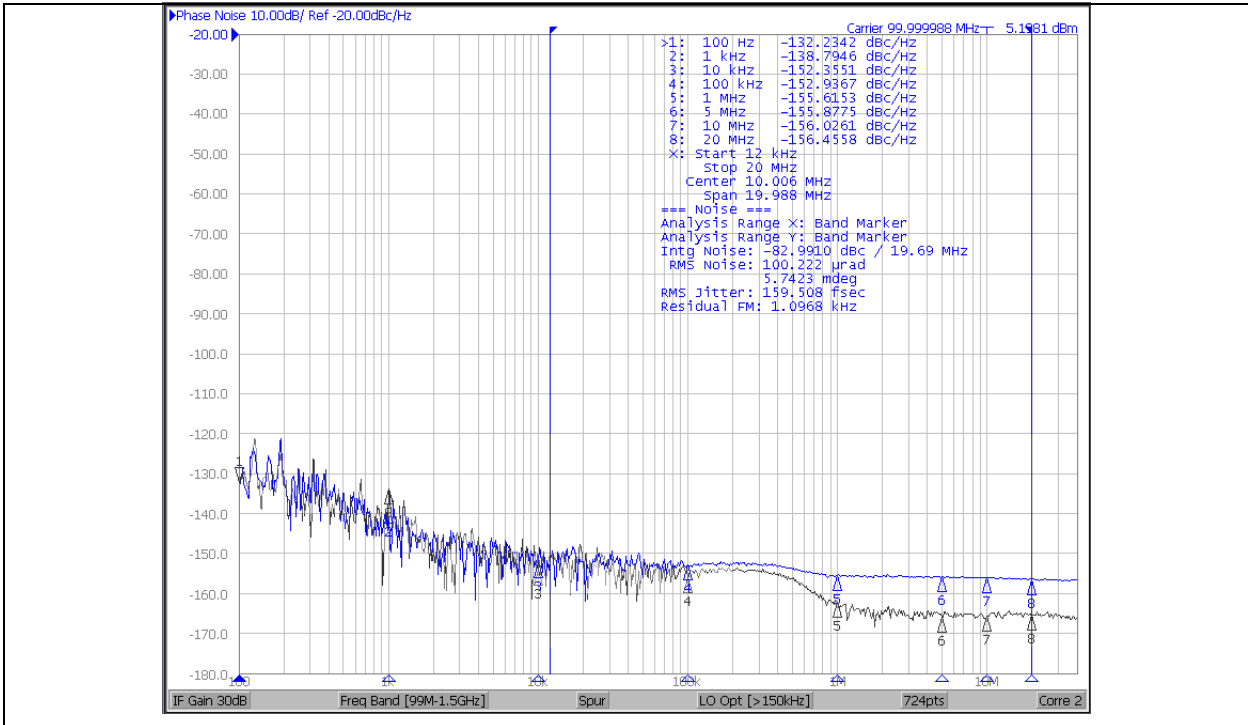


FIGURE 2-1: 100 MHz Phase Jitter.

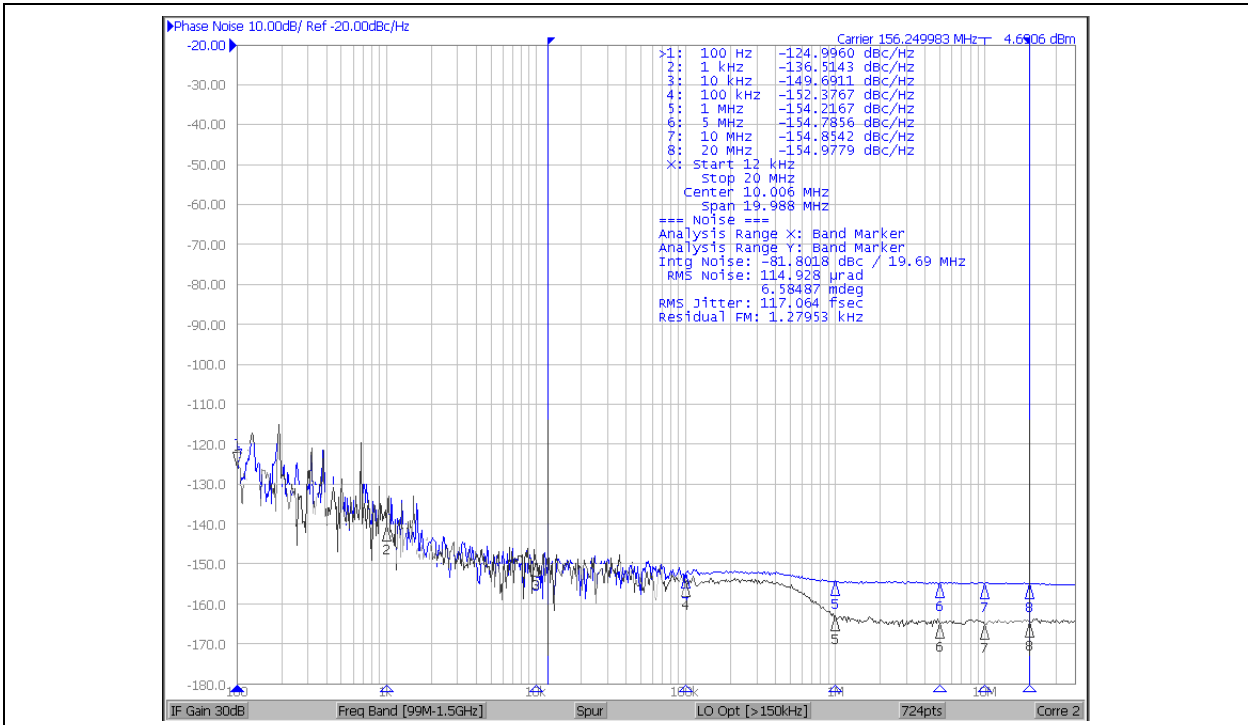


FIGURE 2-2: 156.25 MHz Phase Jitter.

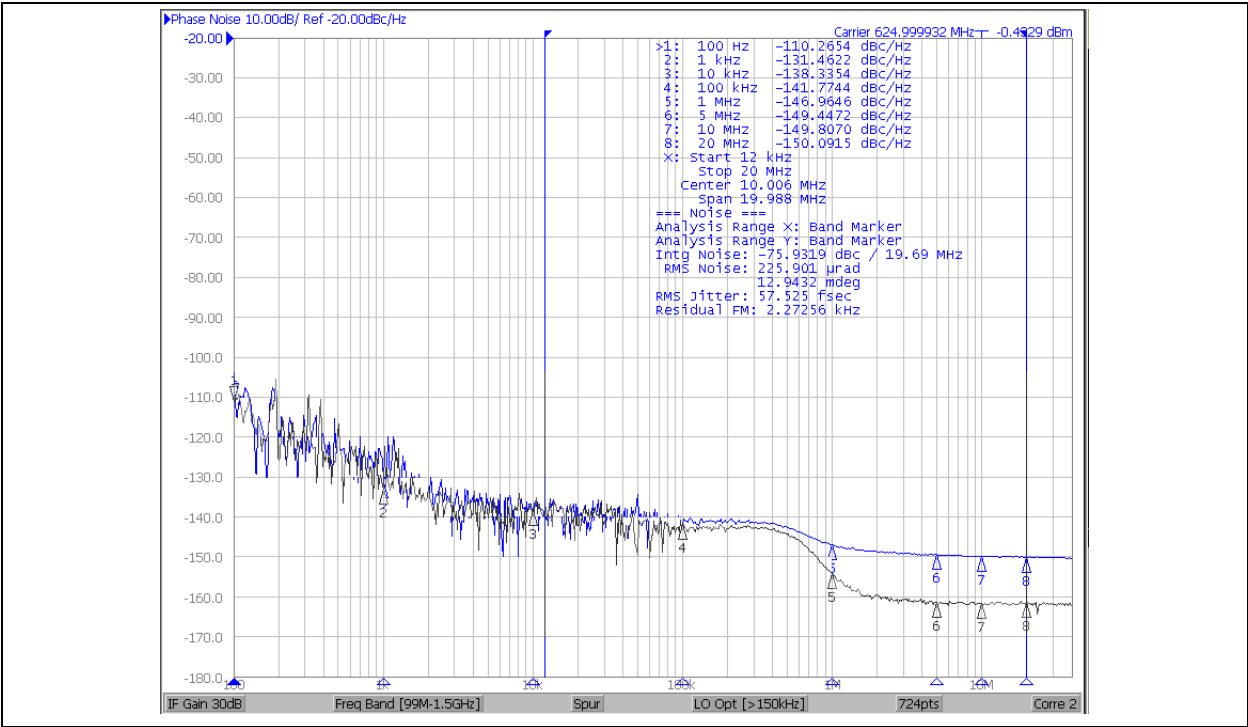


FIGURE 2-3: 625 MHz Phase Jitter.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2, 3, 4	Q0, /Q0, Q1, /Q1	LVPECL, PECL, ECL, Outputs: Terminates to $V_{CC} - 2V$.
5	VEE	Negative Power Supply.
6	/D	LVPECL, PECL, ECL, complementary Clock or Data Input: Internal 75 k Ω pull-up and pull-down resistors. If left open, default is half of supply voltage. When input is not used, it can be left open.
7	D	LVPECL, PECL, ECL, Clock or Data Input: Internal 75 k Ω pull-down resistors. If left floating, pin defaults low, Q goes low.
8	VCC	Positive Supply Voltage.

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4.0 TIMING DIAGRAM

4.1 Input Waveform

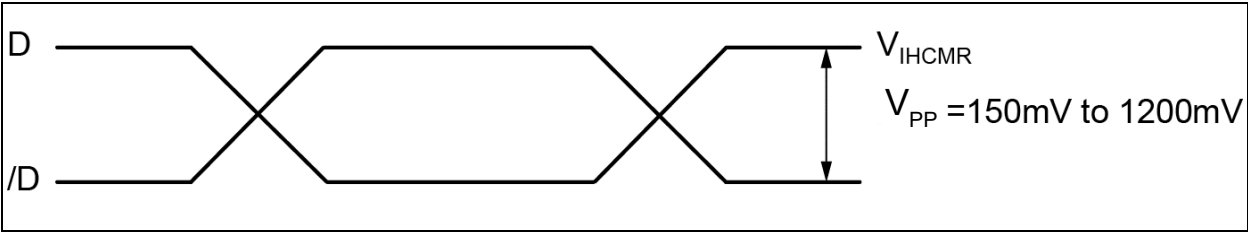


FIGURE 4-1: *Input Waveform.*

5.0 TERMINATION RECOMMENDATIONS

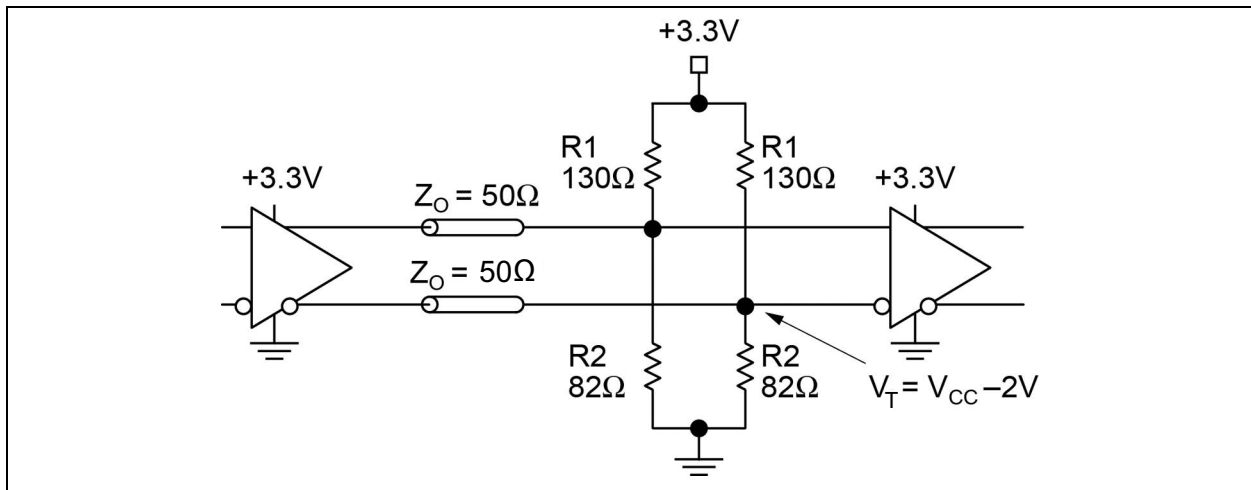


FIGURE 5-1: Parallel Termination - Thevenin Equivalent.

Note: For +2.5V systems: $R_1 = 250\Omega$, $R_2 = 62.5\Omega$

Note: For +5.0V systems: $R_1 = 82\Omega$, $R_2 = 130\Omega$

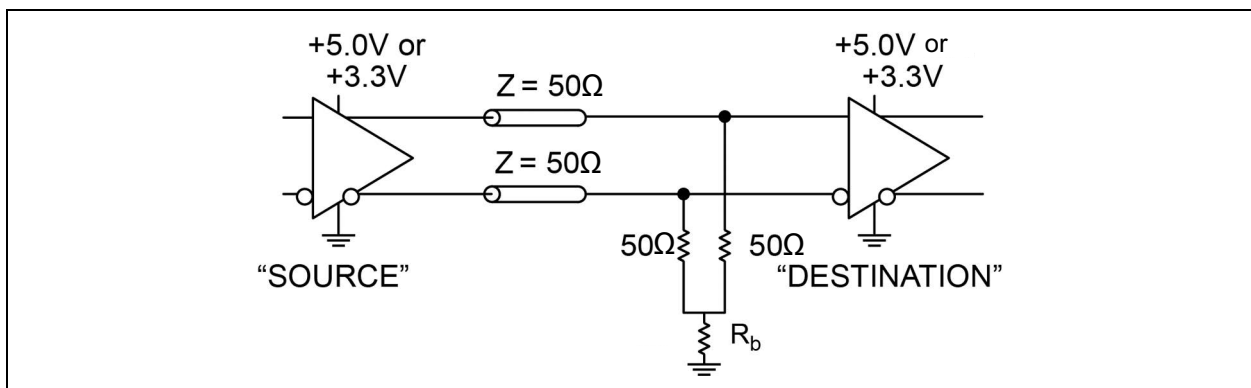


FIGURE 5-2: Three-Resistor Y-Termination.

Note: Power-saving alternative to Thevenin termination

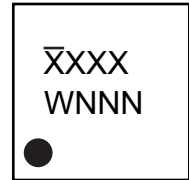
Note: Place termination resistors as close to destination inputs as possible

Note: R_b resistor sets the DC bias voltage equal to V_T . For +3.3V systems $R_b = 46\Omega$ to 50Ω
For +5V systems, $R_b = 110\Omega$

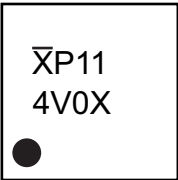
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

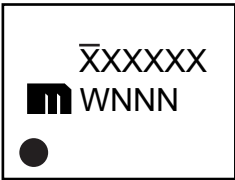
8-Lead MSOP*



Example



8-Lead SOIC*



Example

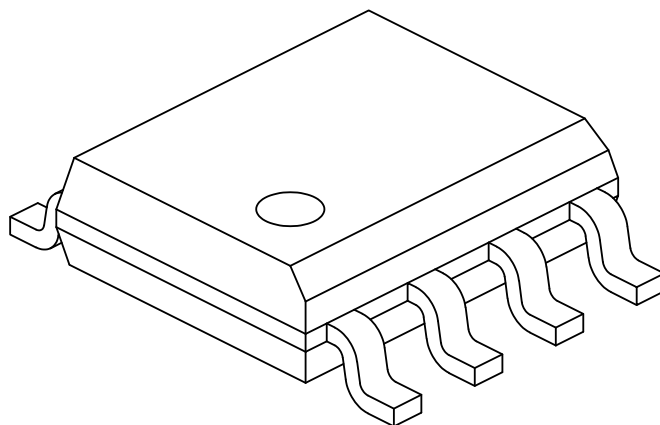


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (̄) and/or Overbar (¯) symbol may not be to scale.	

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8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	—	—	1.75
Molded Package Thickness	A2	1.25	—	—
Standoff §	A1	0.10	—	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	—	0.50
Foot Length	L	0.40	—	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	—	0.25
Lead Width	b	0.31	—	0.51
Lead Bend Radius	R	0.07	—	—
Lead Bend Radius	R1	0.07	—	—
Foot Angle	θ	0°	—	8°
Mold Draft Angle	θ1	5°	—	15°
Lead Angle	θ2	0°	—	—

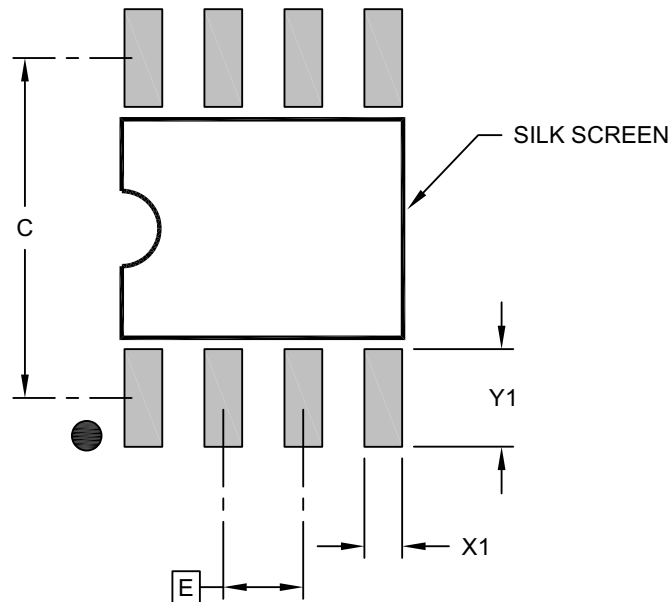
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-3BX Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (3BX) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

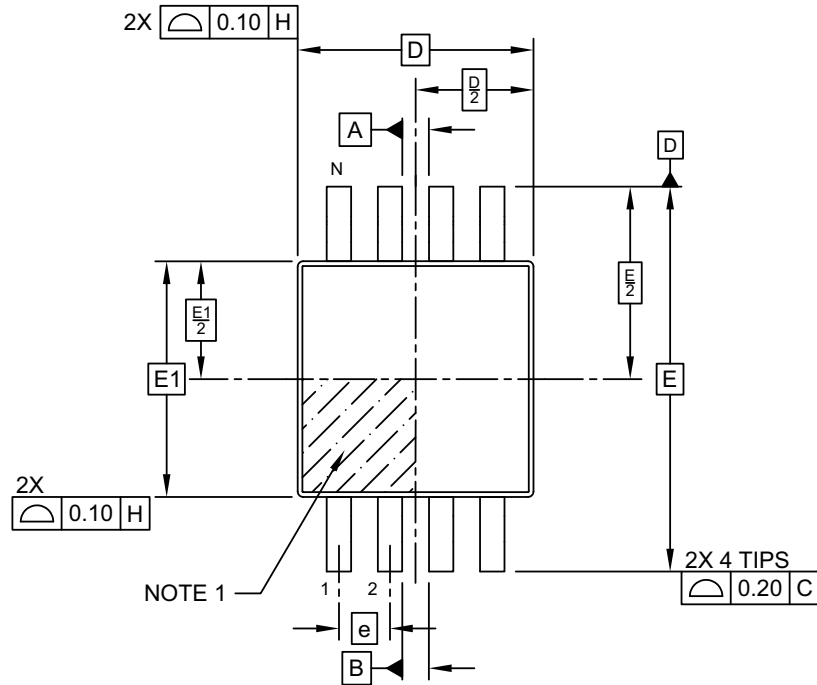
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-3BX Rev K

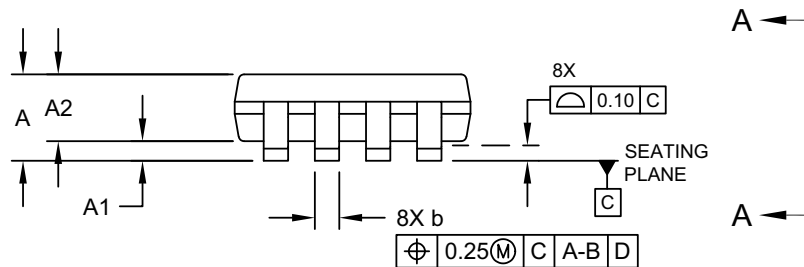
8-Lead MSOP Package Outline and Recommended Land Pattern

8-Lead Plastic Micro Small Outline Package (DMA) - 3x3 mm Body [MSOP] Micrel Legacy Package MSOP-08L

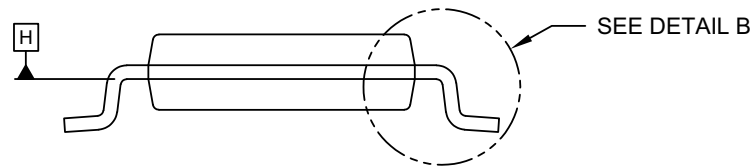
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



TOP VIEW



SIDE VIEW

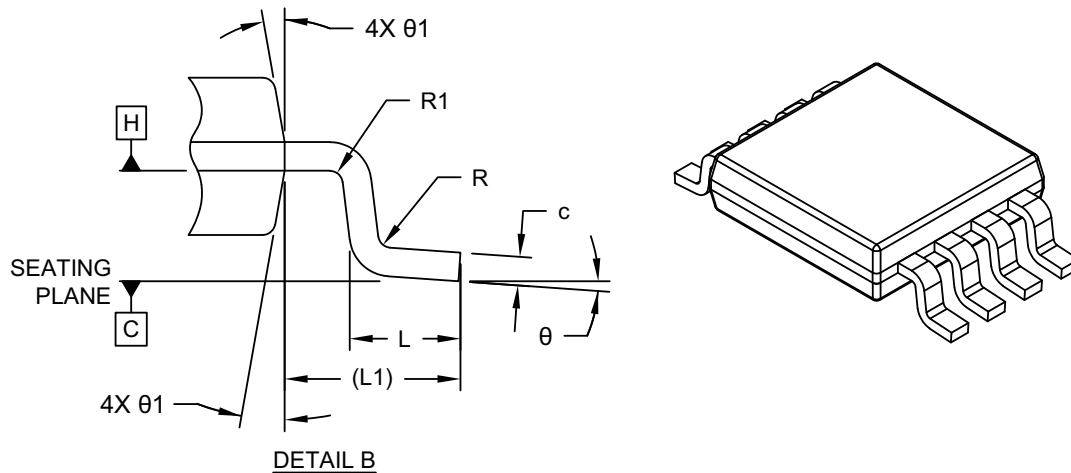


VIEW A-A

Microchip Technology Drawing C04-1082 Rev A Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (DMA) - 3x3 mm Body [MSOP] Micrel Legacy Package MSOP-08L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	0.94	1.02	1.10
Standoff	A1	0.00	—	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D	3.00 BSC		
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Terminal Width	b	0.25	0.30	0.40
Terminal Thickness	c	0.13	0.15	0.23
Terminal Length	L	0.45	0.55	0.70
Footprint	L1	0.95 REF		
Lead Bend Radius	R	0.07	—	—
Lead Bend Radius	R1	0.07	—	—
Foot Angle	θ	0°	—	8°
Mold Draft Angle	θ1	5°	—	15°

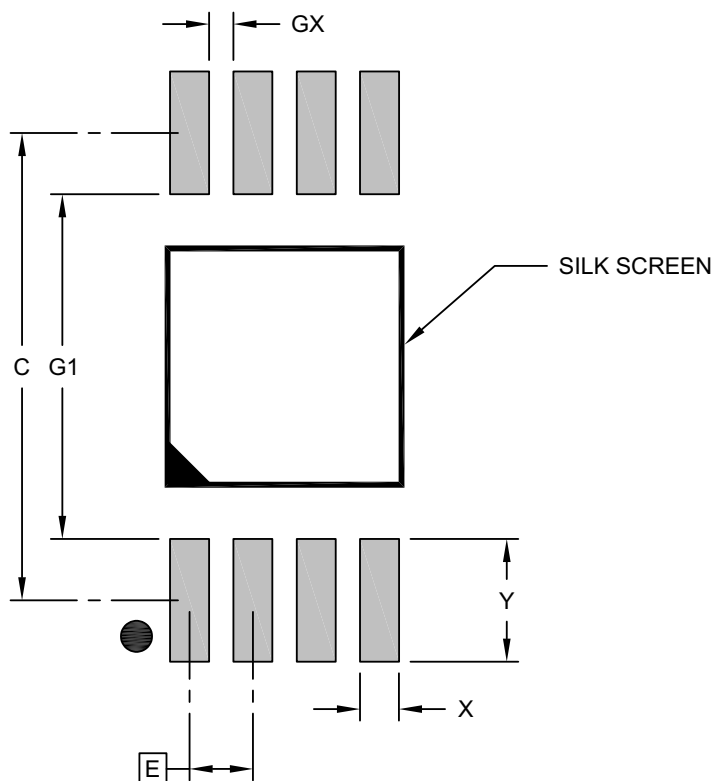
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1082 Rev A Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (DMA) - 3x3 mm Body [MSOP] Micrel Legacy Package MSOP-08L

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.80	
Contact Pad Width (X8)	X			0.40
Contact Pad Length (X8)	Y			1.26
Contact Pad to Contact Pad (X4)	G1	3.54		
Contact Pad to Contact Pad (X6)	GX	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3082 Rev A

APPENDIX A: REVISION HISTORY

Revision A (April 2023)

- Converted Micrel document SY100EP11U to Microchip data sheet DS20006778A.
- Minor text changes throughout.
- Revised [Electrical Characteristics](#) section with updated Electrical tables.
- Revised [Figure 4-1](#) and [Figure 5-2](#).
- [Figure 2-1](#), [Figure 2-2](#), and [Figure 2-3](#) were added in the [Additive Phase Noise Plots](#) section.

SY100EP11U

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	X	X	X	XX
Device	Voltage Option	Package	Temperature Range	Packing Option
Device: SY100EP11: 1:2 Differential PECL/NECL Fanout Buffer				
Voltage Option:	U	=	2.5V/3.3V/5V	
Package:	K	=	8-Lead MSOP	
	Z	=	8-Lead SOIC	
Temperature Range:	G	=	-40°C to +85°C (NiPdAu, Lead-Free)	
Packing Option:	<blank>	=	95/Tube (SOIC option)	
	<blank>	=	100/Tube (MSOP option)	
	TR	=	1,000/Reel	

Examples:

a) SY100EP11UKG: 2.5V/3.3V/5V 1:2 Differential PECL/NECL Fanout Buffer, -40°C to +85°C, 8-Lead MSOP, 100/Tube

b) SY100EP11UKG-TR: 2.5V/3.3V/5V 1:2 Differential PECL/NECL Fanout Buffer, -40°C to +85°C, 8-Lead MSOP, 1000/Reel

c) SY100EP11UZG: 2.5V/3.3V/5V 1:2 Differential PECL/NECL Fanout Buffer, -40°C to +85°C, 8-Lead SOIC, 95/Tube

c) SY100EP11UZG-TR: 2.5V/3.3V/5V 1:2 Differential PECL/NECL Fanout Buffer, -40°C to +85°C, 8-Lead SOIC, 1000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

SY100EP11U

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