USB2514B

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB2514B. These checklist items should be followed when utilizing the USB2514B in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 15. Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB Signals"
- Section 5.0, "USB Connectors"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "Strap Configuration Options"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB2514B implementor should have the following documents on hand:

- *USB2514B Data Sheet*
- *EVB-USB2514BC Evaluation Board User's Guide*
- EVB-USB2514BC Schematics
- Other references on the USB2514B product page at www.microchip.com
- Universal Serial Bus Specification 2.0

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground pins, **GND** (ePAD), should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.4 USB-IF Compliant USB Connectors

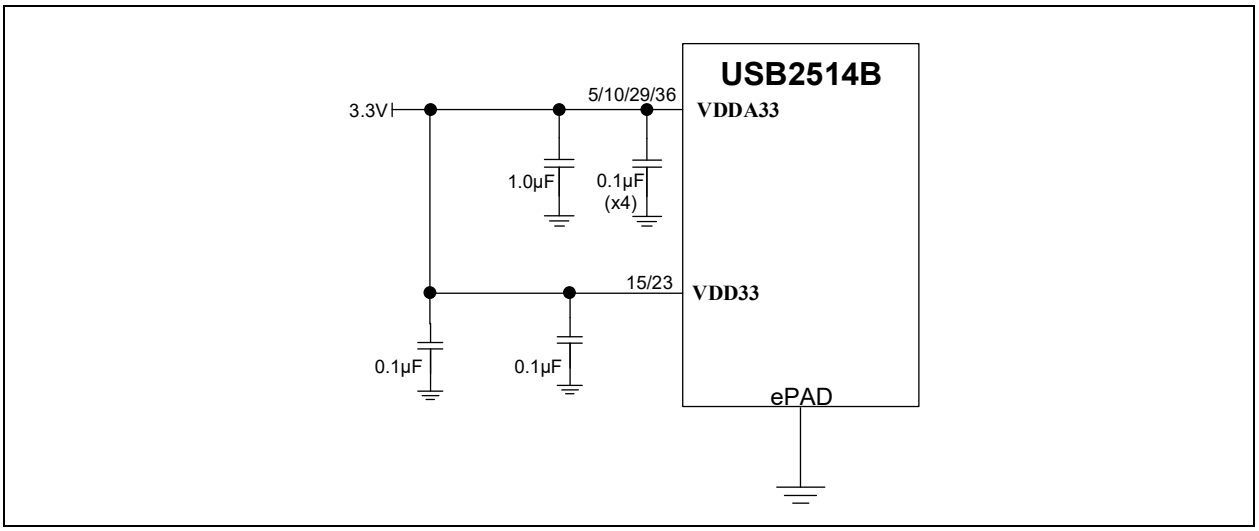
- USB-IF certified USB Connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

3.0 POWER

- The analog supplies (**VDDA33**) are located on pins 5, 10, 29, and 36. These pins all require a connection to a regulated 3.3V power plane. It is recommended to connect a 0.1 µF capacitor close to each **VDDA33** pin, along with a 1.0 µF bulk capacitance which is shared across all **VDDA33** pins. The capacitor size should be SMD_0603 or smaller.
- The **VDD33** pins (pins 15, 23) supply voltage to the digital I/O blocks. The design should include a 0.1 µF capacitor to be placed close to the pin. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 USB SIGNALS

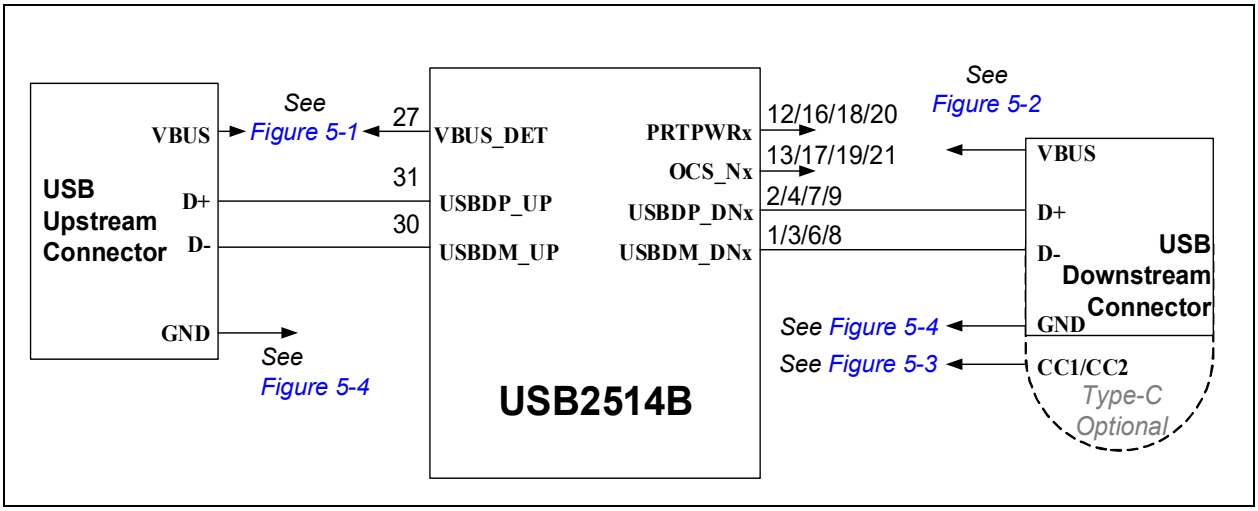
4.1 USB PHY Interface

- **USBDP_UP** (pin 31): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB Connector.
- **USBDM_UP** (pin 30): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM pin of a USB Connector.
- **USBDP_DN1/USBDP_DN2/USBDP_DN3/USBDP_DN4** (pins 2/4/7/9): These pins are the positive (+) signal of the downstream ports USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB Connector.
- **USBDM_DN1/USBDM_DN2/USBDM_DN3/USBDM_DN4** (pins 1/3/6/8): These pins are the negative (–) signal of the downstream port USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM pin of a USB Connector.

Note:	The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I2C configuration registers.

For transmit and receive channel connection details, refer to Figure 4-1.

FIGURE 4-1: USB AND DATA SIGNAL CONNECTIONS



4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

- If any downstream of the USB2514B is unused, it should be disabled. This can be achieved through hub configuration (I2C) or through a port disable strap option.

4.2 USB Protection

- The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories.
  1. TVS protection diodes
     - ESD protection for IEC-61000-4-2 system level tests
  2. Application-targeted protection ICs or galvanic isolation devices
     - DC overvoltage protection for short to battery protection
  3. Common-mode chokes
     - For EMI reduction
- The USB2514B can be used in conjunction with these types of devices, but it is important to understand the negative effect on USB signal integrity that these devices may have and to select components accordingly and follow the implementation guidelines from the manufacturer of these devices. You may also use the following general guidelines for implementing these devices:
  - Select only devices that are designed specifically for high-speed applications. Based on the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
  - These devices should be placed as close to the USB connector as possible.
  - Never branch the USB signals to reach protection device. Always place the protection devices directly on top of the USB differential traces.
  - The effectiveness of TVS devices depends heavily on effective grounding. Always ensure a very low-impedance path to a large ground plane.
  - Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note:	Microchip PHYBoost configuration options are available for compensating the negative effects of these devices. This feature may help overcome marginal failures. It is simplest to determine the appropriate setting using laboratory experiments, such as USB eye diagram tests, on physical hardware.

5.0 USB CONNECTORS

5.1 Upstream Port VBUS and VBUS_DET

The upstream port VBUS line must have no more than 10 µF of total capacitance connected.

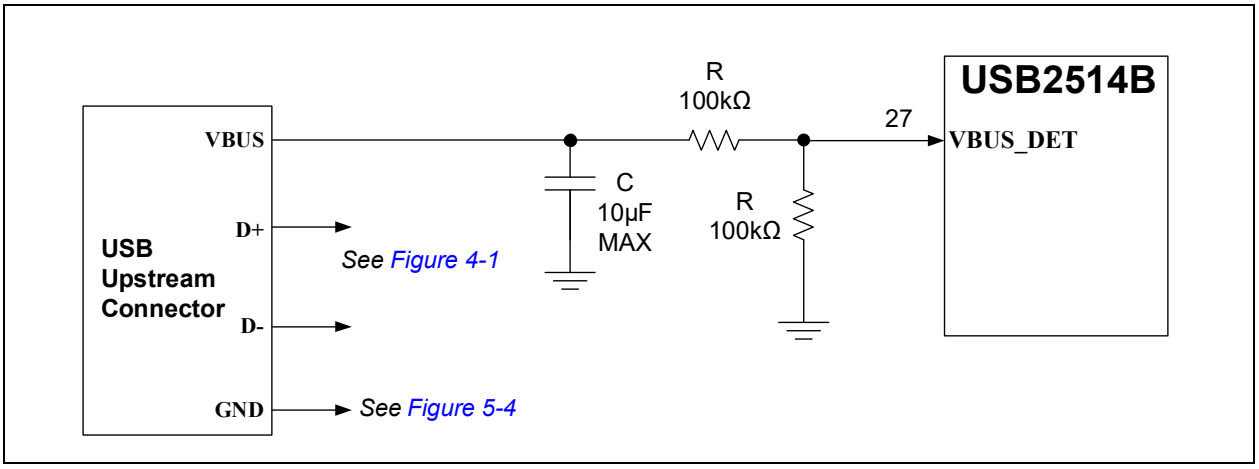
The **VBUS_DET** pin is used by the USB2514B to detect the presence of a USB host. The USB host can also toggle the state of VBUS at any time to force a soft Reset and reconnection of the USB2514B.

It is permissible to tie **VBUS_DET** directly to 3.3V. However, this is not recommended because the ability to force a Reset of the hub from the USB host VBUS toggling is lost.

The recommended implementation is shown in Figure 5-1. Note the precise resistor values are not critical and alternate values may be selected as long as:

- The impedance from the **VBUS** pin of the USB connector to the **VBUS_DET** pin is sufficiently high-impedance to minimize pin leakage when VBUS is present before the Hub IC is powered on.
- A sufficient voltage level is present on the **VBUS_DET** for the full range of VBUS (4.5V to 5.5V).

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS AND VBUS_DET CONNECTIONS



5.2 Downstream Port VBUS and PRTPWRx/OCS_Nx

5.2.1 PRTPWRX

- The **PRTPWRx** pin is an output pin which has the following states:
  1. PORT OFF: **PRTPWRx** drives low. The **PRTPWRx** pin will only transition to the PORT ON state through a specific command from the USB host.
  2. PORT ON: **PRTPWRx** drives low. The **PRTPWRx** pin will only transition to the PORT OFF state if:
     - An overcurrent event is sensed on **OCS_Nx** pin.
     - A command from the USB host is received which instructs the hub to disable power.
     - The hub is reset or experiences a POR event.
- To ensure minimal BOM cost and simplicity, select a port power controller device with a 3.3V logic level, active-high input. If a device that operates from a 5V logic level is selected, the **PRTPWRx** signal may need to be boosted using external logic. If a port power controller with active-low input is selected, the **PRTPWRx** signal needs to be inverted using external logic.

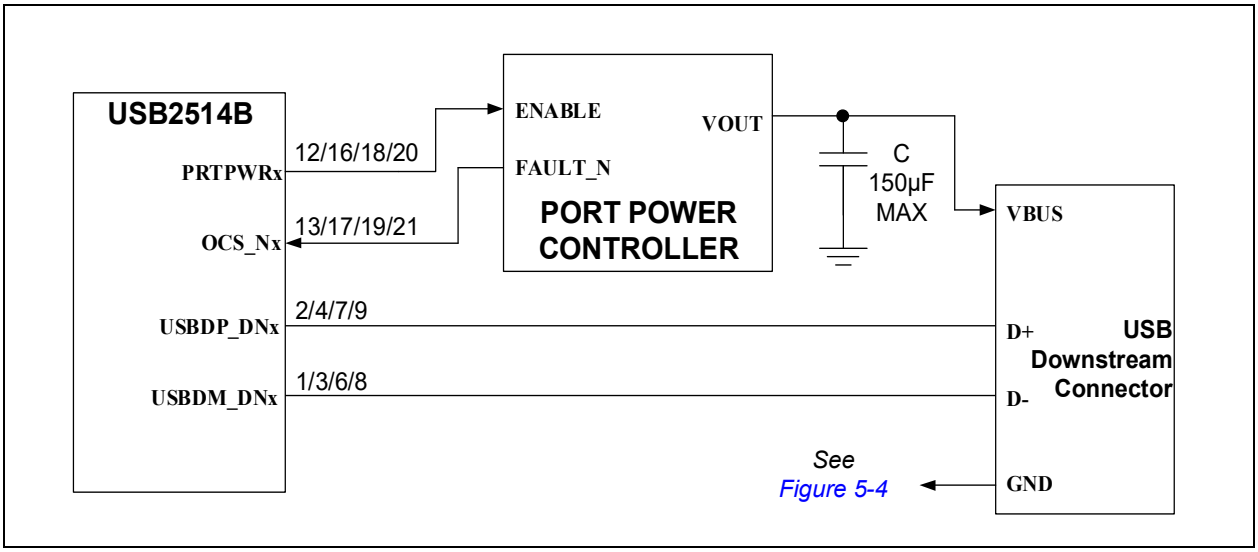
5.2.2 OCS_NX

- The **OCS_Nx** pin is an input buffer which monitors overcurrent events. The pin includes an internal pull-up resistor to the 3.3V domain, so an external pull-up resistor is not required. The pin state is ignored when the port is in the PORT OFF state. When the port is in the PORT ON state, an overcurrent event is detected if the state of the pin is detected as low (below the V_{ILI} voltage). When an overcurrent event is detected, the port automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

- To ensure minimal BOM cost and simplicity, select a port power controller device with an active-low, open-drain FAULT indicator output. If a port power controller with active-high FAULT indicator output is selected, the **OCS_Nx** signal needs to be inverted using external logic.

A typical VBUS port power control implementation is shown in Figure 5-2.

FIGURE 5-2: DOWNSTREAM VBUS AND PORT POWER CONNECTIONS



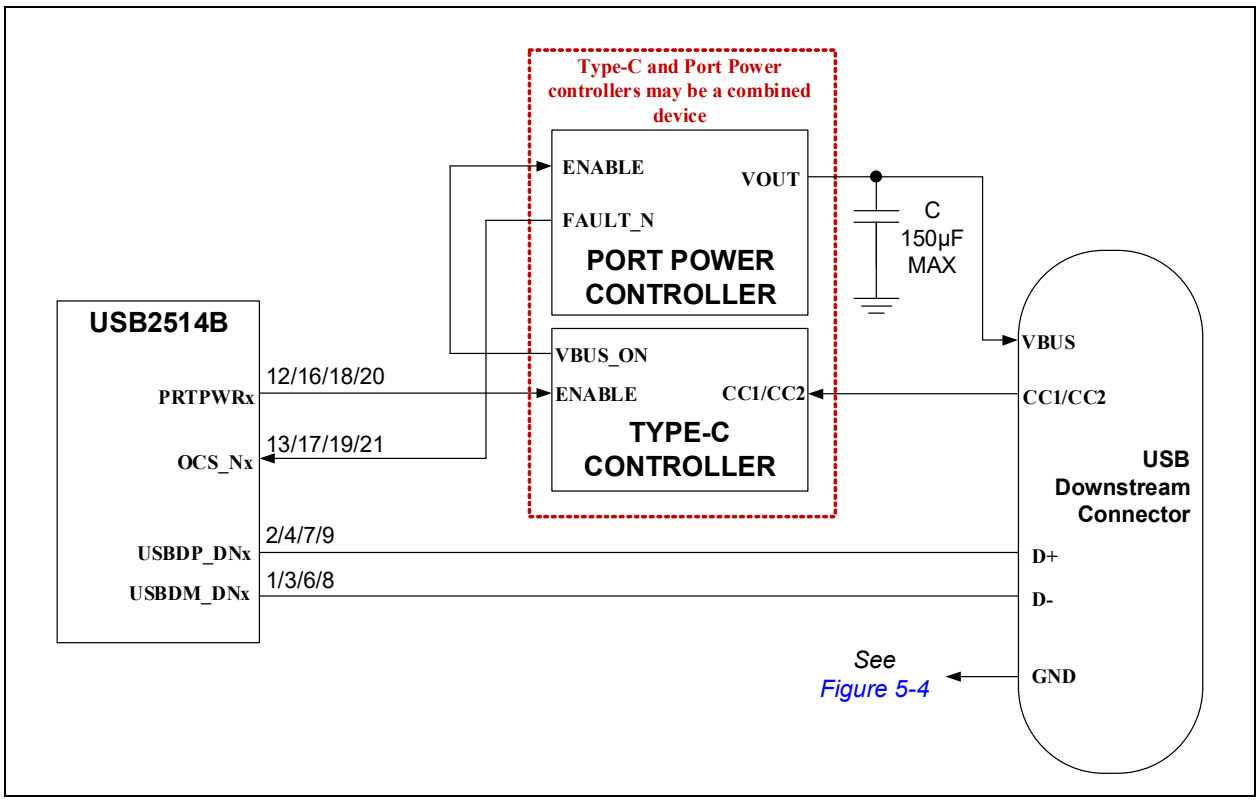
Note: The implementation, as shown in Figure 5-2, assumes that the port power controller has an active-high enable input and an active-low, open-drain-style FAULT indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 Downstream Port Type-C Support

- The USB2514B may be used with Type-C as the downstream port. This requires a Type-C port controller or combined port power controller and Type-C port controller. The USB2514B simply controls the Type-C port controller in the same way as it would control a standard Type-A port power controller. It does not require any kind of Type-C port status information from the Type-C port controller. The **PRTPWRx** signal should be connected to an enable pin on the Type-C controller and the **OCS_Nx** signal should connect to the FAULT indicator output of the port power controller.
- If the Type-C controller and the port power controller are separate devices, the Type-C controller must control the enable pin of the port power controller. The **PRTPWRx** should not directly control the VBUS enable signal of the port power controller.
- A Type-C controller may be configured to signal a 500 mA, 1.5A, or 3.0A port power capability. The selected port power controller should be sized accordingly.

A typical implementation is shown in Figure 5-3.

FIGURE 5-3: DOWNSTREAM VBUS AND PORT POWER CONNECTIONS WITH A TYPE-C PORT



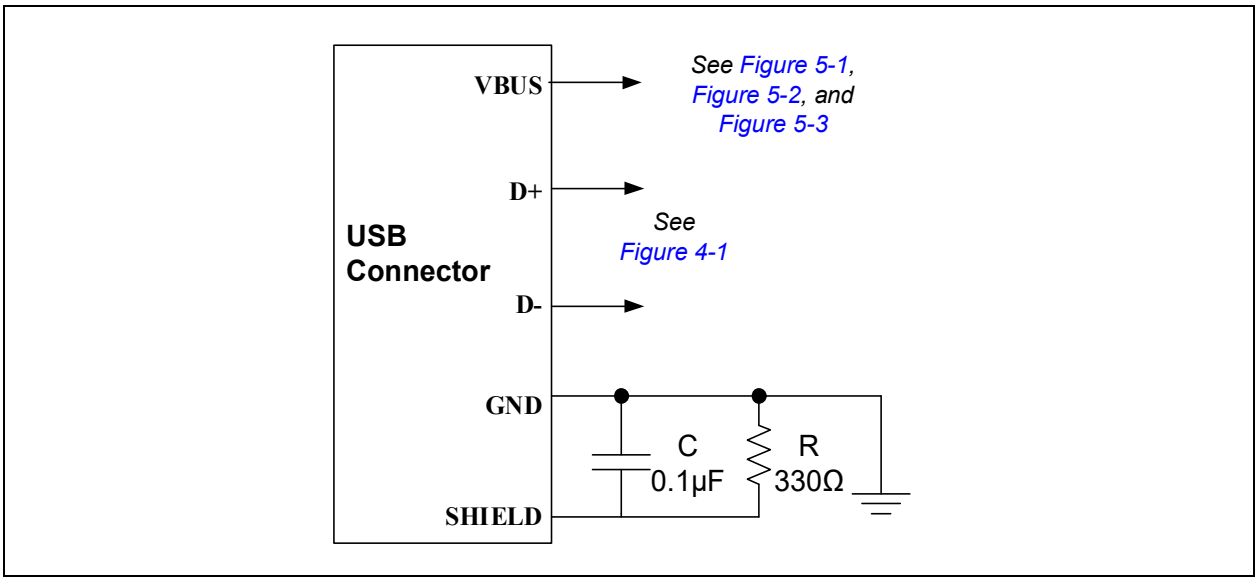
Note: The implementation, as shown in Figure 5-3, assumes that the Type-C controller has an active-high enable input, and the port power controller has an active-low, open-drain-style FAULT indicator. External polarity inversion through buffers or FETs may be required if the Type-C controller and/or port power controller has different I/O characteristics.

5.4 GND Recommendations

- The **GND** pins of the USB connector must be connected to the PCB with a low-impedance path directly to a large GND plane.
- The **SHIELD** pins of the USB connector may be connected in one of two ways:
  - [Recommended] To GND through a resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
  - Directly to the GND plane.

The recommended implementation is shown in Figure 5-4.

FIGURE 5-4: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



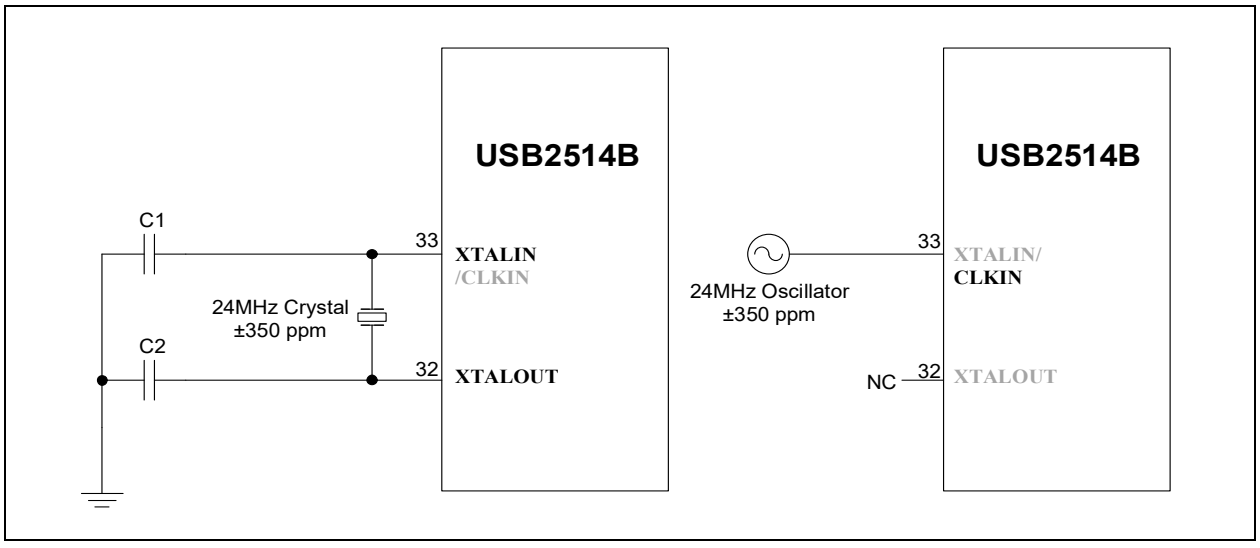
6.0 CLOCK CIRCUIT

6.1 Crystal and External Clock Connection

A 24.000-MHz (±350 ppm) reference clock is the source for the USB interface and for all other functions of the device. (See Figure 6-1.) For exact specifications and tolerances, refer to the latest version of the *USB2514B Data Sheet*.

- **XTALIN/CLKIN** (pin 33) connects to either one terminal of the crystal or to an external 24 MHz clock when a crystal is not used.
- **XTALOUT** (pin 32) is the other terminal of the crystal circuit with 1.2V p-p output and a weak (< 1 mA) driving strength. When an external clock source is used to drive **XTALIN/CLKIN**, leave this pin unconnected.
- The crystal loading capacitor values are system dependent, based on the total C_L specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit. A commonly used formula for calculating the appropriate physical C_1 and C_2 capacitor values is:
  - $C_L = ((C_{X1})(C_{X2}) / (C_{X1} + C_{X2}))$
  - Where: CL is the specification from the crystal data sheet, $C_{X1} = C_{stray} + C_1$, $C_{X2} = C_{stray} + C_2$.
  - Note that C_{stray} is the stray/parasitic capacitance due to PCB layout. It can be assumed to be very small, within the 1 pF to 2 pF range, and then verified by physical experiments in the laboratory if PCB simulation tools are not available.

FIGURE 6-1: CRYSTAL AND OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 RBIAS Resistor

- **RBIAS** (pin 35) on the USB2514B must connect to ground through a 12 kΩ resistor with a tolerance of 1%. This is used to set up critical bias currents for the internal circuitry. This should be placed as close to the IC pin as possible, and be given a dedicated, low-impedance path to a ground plane.

7.2 Board Power Supplies

7.2.1 POWER RISE TIME

- The power rail voltage and rise time should adhere to the supply rise time specifications as defined in the *USB2514B Data Sheet*.
- If a monotonic/fast power rail rise cannot be assured, then the **RESET_N** signal should be controlled by a Reset supervisor and only released when the power rail has reached a stable level.

7.2.2 CURRENT CAPABILITY

- It is important to size the 5V and 3.3V power rails appropriately. The 5V power supply must be capable of supplying sufficient power for all exposed USB ports concurrently without drooping below the minimum voltage permissible in the USB specification:
  - 500 mA per-port for USB2 Ports
  - 1.5A or 3.0A per Type-C port (depending on setting of the Type-C controller)
- The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that a 3.3V power rail be sized such that is able to supply the maximum power consumption specifications as displayed in the *USB2514B Data Sheet*.

7.3 Reset Circuit

- **RESET_N** (pin 26) is an active-low Reset input. This signal resets all logic and registers within the USB2514B. A hardware Reset (**RESET_N** assertion) is not required following power-up. Refer to the latest copy of the *USB2514B Data Sheet* for Reset timing requirements. Figure 7-1 shows a recommended Reset circuit for powering up the USB2514B when Reset is triggered by the power supply. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

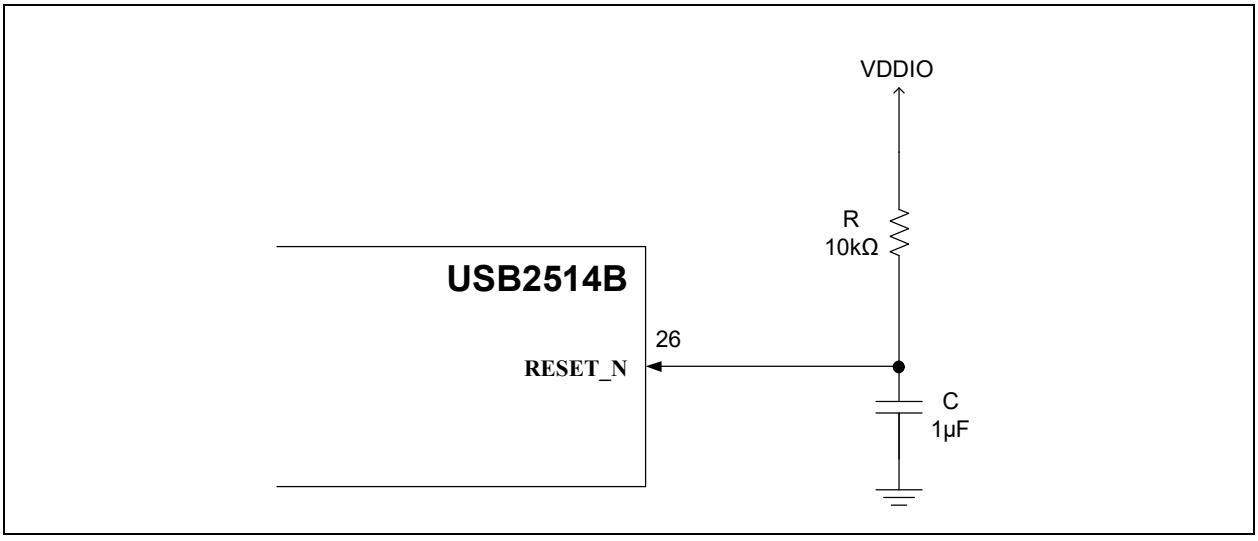
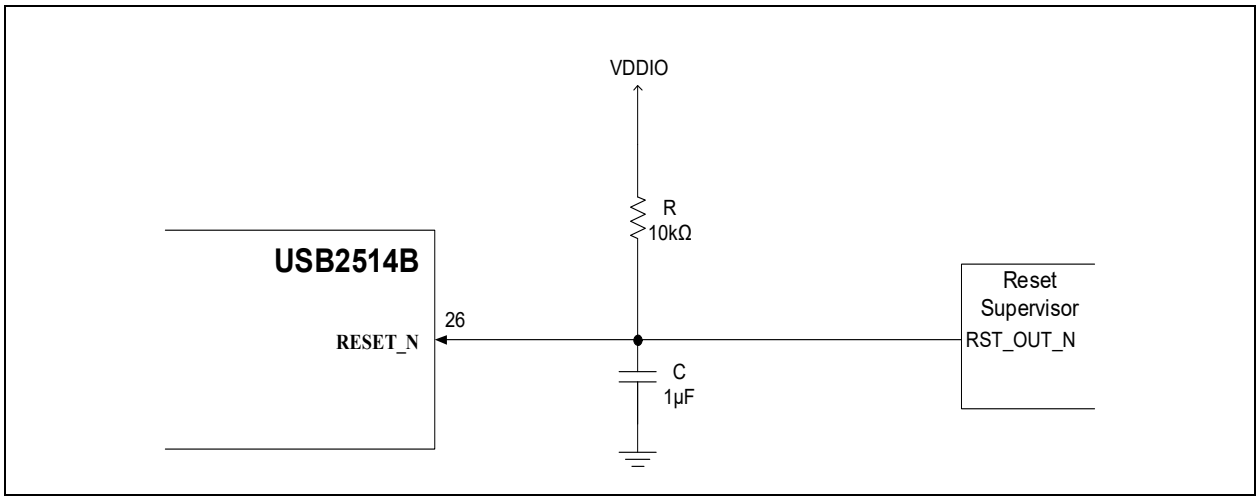


Figure 7-2 details the recommended Reset circuit for applications where Reset is driven by an external CPU/MCU. The Reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm Reset after power-up. The values for the “R” resistor and “C” capacitor are not critical and may be adjusted per individual system needs or preferences.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 STRAP CONFIGURATION OPTIONS

- The USB2514B can be configured through **CFG_SEL**[1:0] (pins 25 and 24) in one of four operating modes. (See Table 8-1.) When Strap Option is enabled (**CFG_SEL0** = 0), **NON_REM**[1:0] (pins 22 and 28), configure the presence of permanently attached devices on the downstream ports. Similarly, **BC_EN**[4:1] pins enable or disable the battery charging protocol on each downstream port, respectively.

Note:	Note that **CFG_SEL**[1:0] and **NON_REM**[1:0] pins have no internal terminations and must be terminated with the use of external resistors. Either pin can be driven low with an external 100 kΩ pull-down resistor to ground, or a 10 kΩ pull-up resistor to **VDD33**.

TABLE 8-1: OPERATION MODE CONFIGURATION STRAPS

CFG_SEL1	CFG_SEL0	Description
0	0	Strap Options enabled, Self-Powered Operation enabled, Individual Power Switching and Individual Overcurrent Sensing
0	1	Strap Options disabled, all registers configured by MCU over SMBus
1	0	Strap Options enabled, Bus-Powered Operation enabled, Individual Power Switching and Individual Overcurrent Sensing
1	1	Strap Options Disabled, all registers configured by I2C EEPROM

8.1 Non Removable Port Settings

- In a typical USB2514B application, downstream ports are routed to a user-accessible USB connector, and hence the downstream port should be configured as a removable port. The following guidelines can be used to determine which setting to use:
  - If the port is routed to a user-accessible USB connector, it is **removable**.
  - If the port is routed to a permanently attached an embedded USB device on the same PCB, or non user-accessible wiring or cable harness, it is **non-removable**.
- The removable or non-removable device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host may use to understand if a port is a user-accessible port or a permanently attached device. Under standard operating conditions, the USB host may or may not modify its operation based on this information. Certain USB compliance tests are impacted by this setting, so designs which undergo USB compliance testing and certification must ensure that the configuration settings are correct.
- Non-removable port settings can be configured via:
  - EEPROM
  - I2C-based SOC/MCU
  - Hardware strap options
- To configure this feature via hardware strap options, Strap Option mode must be enabled (**CFG_SEL0** = 0). The USB2514B has two configuration strap option pins, **NON_REM**[1:0], which can be used to set the non-removable configurations for certain downstream ports, see Table 8-2.

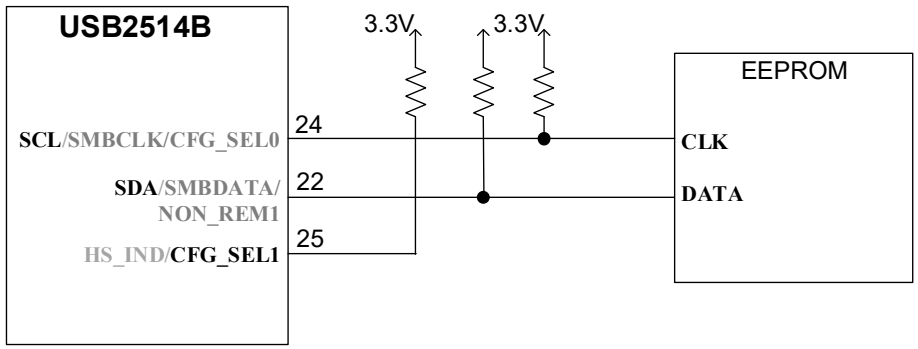
TABLE 8-2: NON REMOVABLE PORT CONFIGURATION STRAPS (CFG_SEL0 = 0)

NON_REM1	NON_REM0	Description
0	0	All downstream ports are removable.
0	1	Port 1 is non-removable.
1	0	Port 1 and Port 2 are non-removable.
1	1	Port 1, Port 2, and Port 3 are non-removable.

8.2 Configuration via EEPROM (CFG_SEL1 = 1, CFG_SEL0 = 1)

When configuring via EEPROM, the USB2514B operates as an I2C controller at a fixed 58.6 kHz speed. The EEPROM must be organized for 256 x 8-bit operation, and the entire register set from 0x00 to 0xFF must be replicated in the EEPROM device. See Figure 8-1. The default values should be obtained from the *USB2514B Data Sheet*.

FIGURE 8-1: RECOMMENDED CONNECTIONS IF CONFIGURED VIA EEPROM



Note: The EEPROM device must be programmed on board or preprogrammed before PCB assembly. The USB2514B does not have a programming/USB pass-through mechanism.

8.3 Configuration via MCU/SoC Device (CFG_SEL1 = 0, CFG_SEL0 = 1)

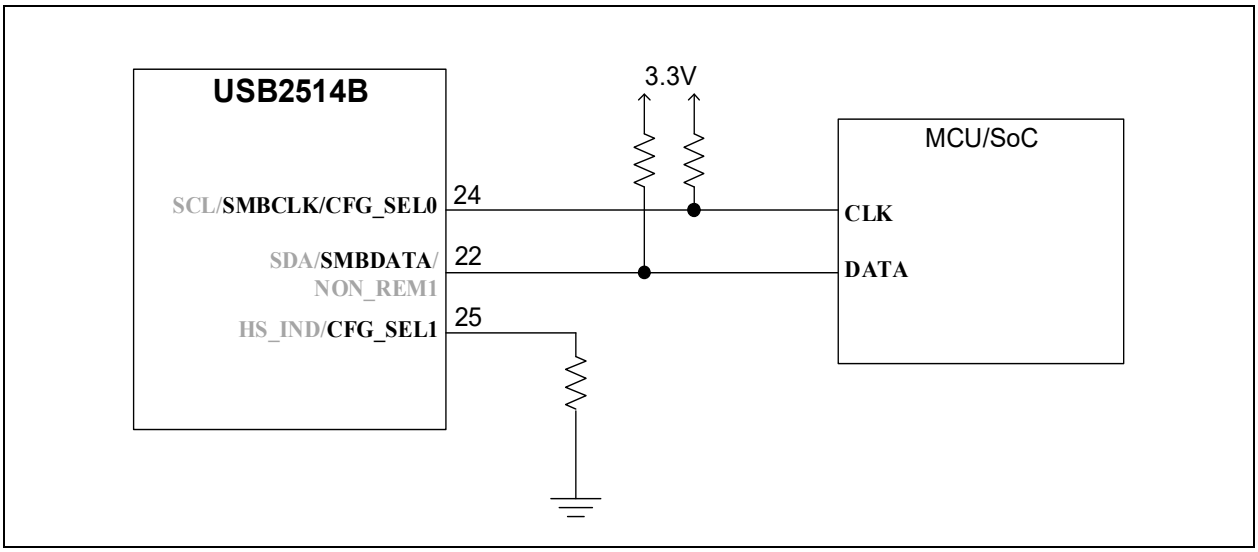
8.3.1 MCU/SOC OPERATION SUMMARY

- By default, the USB2514B executes based on internal register defaults, and an external MCU/SoC device is not explicitly required. If settings which differ from the internal defaults are required by the application, an external MCU/SoC may be used to modify the register settings. Only the specific settings which need to be modified from the default need to be changed.
- The USB2514B supports only one address option: 010_1100b.

8.3.2 MCU/SOC CONNECTION DIAGRAMS

The recommended schematic connections for an MCU/SOC memory device are shown in Figure 8-2.

FIGURE 8-2: RECOMMENDED CONNECTIONS IF CONFIGURED VIA MCU/SOC



8.4 Self-Powered/Bus-Powered Settings (Available via SMBus Configuration Only)

By default, the hub is configured as self-powered. The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the Upstream USB connector's **VBUS** pin and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is **bus-powered**.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is **self-powered**.
- If the hub is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely **self-powered** (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a self-powered hub to 100 mA. Any device which connects to a self-powered hub that declares it needs more than 100 mA will be prevented from operating by the USB host.

The USB2514B also supports dynamic self-powered and bus-powered operation via the **LOCAL_PWR** control input pin. This feature must be enabled via EEPROM or SMBus configuration (DYNAMIC bit in CFG1 register). Once enabled, the **LOCAL_PWR** pin works as:

- 1: Self-powered – No downstream port power restrictions will be in place.
- 0: Bus-powered – Downstream port power restrictions will be enforced by the USB host.

The **LOCAL_PWR** cannot be changed dynamically. To change the mode of operation, the pin state must be changed, then the hub must be reset for the hub to communicate the new mode of operation descriptors to the USB host.

8.5 Port Disable Straps

This feature is enabled in Strap Option mode (CFG_SEL0 = 0). In this mode, the downstream port x can be disabled through pull-up resistors on both **USBDP_DNx** and **USBDM_DNx** pins. This connection can be made directly to the 3.3V power net, or through a pull-up resistor. The pins may also be shorted together as well to simplify the layout.

Note:	Both USB D+ and D– signals must be pulled high to effectively disable the port. If only 1 pin is pulled to 3.3V, the port will not be disabled.

NOTES:

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	The grounds are tied together.		
	Section 2.4, "USB-IF Compliant USB Connectors"	USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"		The **VDD33** and **VDDA33** are within the range of 3.0V to 3.6V. 0.1 µF capacitors are connected to each power pin as close as possible, along with a 1.0 µF shared capacitor.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	The USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 4.2, "USB Protection"	The ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance, the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	The Upstream Port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.2, "Downstream Port VBUS and PRTPWRx/OCS_Nx"	If the downstream ports are standard Type-A ports, the **PRTPWRx** and **OCS_Nx** are properly connected to the Enable pin of the downstream port power controller and the FAULT indicator output of the port power controller.		
	Section 5.3, "Downstream Port Type-C Support"	If the downstream ports are standard Type-C ports, the **PRTPWRx** is properly connected to the enable pin of the Type-C port controller, and the **OCS_Nx** is connected to the FAULT indicator output of the port power controller.		
	Section 5.4, "GND Recommendations"	Verify if the USB connector is properly connected to PCB ground on both the **GND** pins and the **SHIELD** pins. It is recommended that an RC filter be placed in between the **SHIELD** pins and PCB ground.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 6.0, "Clock Circuit"	Section 6.1, "Crystal and External Clock Connection"	The crystal or clock is 24.000 MHz (±350 ppm).		
		If a single-ended lock is used, it is connected to **XTALIN** while leaving **XTALOUT** floating.		
		If a crystal is used, ensure the loading capacitors are appropriately sized for the crystal loading requirement.		
Section 7.0, "Power and Startup"	Section 7.1, "RBIAS Resistor"	A 12.0 kΩ 1% resistor is connected between the **RBIAS** pin and PCB ground.		
	Section 7.2, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V to 3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet.		
		If the rise time requirement cannot be met, the **RESET_N** line is held low until the power regulators reach a steady state.		
	Section 7.3, "Reset Circuit"	Ensure that the **RESET_N** signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		
Section 8.0, "Strap Configuration Options"	Section 8.1, "Non Removable Port Settings"	For all ports which do not route to user-exposed USB connectors, ensure that the port is configured to be non-removable via EEPROM, SoC/MCU, or hardware strap.		
	Section 8.2, "Configuration via EEPROM (CFG_SEL1 = 1, CFG_SEL0 = 1)"	If configuring via EEPROM, EEPROM is connected to the correct pins and that CFG_SEL0 = 1, CFG_SEL1 = 1.		
	Section 8.3, "Configuration via MCU/SoC Device (CFG_SEL1 = 0, CFG_SEL0 = 1)"	If configuring via SoC/MCU, SoC/MCU is connected to the correct pins and that CFG_SEL0 = 1, CFG_SEL1 = 0.		
	Section 8.4, "Self-Powered/Bus-Powered Settings (Available via SMBus Configuration Only)"	The Self-Powered/Bus-Powered settings are correct, and hardware is designed appropriately. For Self-Powered applications, all power for the board is derived from an external power supply. For Bus-Powered applications, all power for the board is derived from VBUS sourced by the connected USB host.		
	Section 8.5, "Port Disable Straps"	If any USB ports are unused, they are properly disabled by either strapping D+ and D– to 3.3V in hardware, or disabled via EEPROM or SoC/MCU.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004541A (05-19-22)	Initial release	

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