AN3764

Parallel Interfaces for LAN9253 and LAN9254

Author: *Parthiv Pandya*
Microchip Technology Inc.

INTRODUCTION

The LAN9253 and LAN9254 devices enable EtherCAT® via a parallel bus interface called a Host Bus Interface (HBI). This connects to a microcontroller (MCU) or a microprocessor (MPU). The interface provides Multiplexed mode where address and data are transferred on the same pins, and Demultiplexed mode where address and data are transferred on separate address and data pins.

This application note discusses the HBI, its different modes, and the mode performance differences for LAN9253 and LAN9254 devices.

Sections

This document includes the following topics:

References

Consult the following documents for details on the specific parts referred to in this document.

- *LAN9253 Data Sheet* (www.microchip.com/DS00003421)
- *LAN9254 Data Sheet* (www.microchip.com/DS00003422)

Terms and Abbreviations

- HBI – Host Bus Interface
- MCU – Microcontroller
- MPU – Microprocessor
- PDI – Process Data Interface

HOST BUS INTERFACE

The Host Bus Interface (HBI) is an SRAM-style memory interface. It supports native 8-bit and 16-bit cycles, and indexed (address pointer register), demultiplexed (LAN9254 only), and multiplexed accesses. The external pins are connected via the Pin Multiplexer.

HBI Features

The following are the features of the LAN9253 and LAN9254 HBI:

- 8-bit or 16-bit external bus (static selection)
- 32-bit internal registers
- Indexed register access
- Three index/data register banks, each with independent BYTE/WORD to DWORD conversion
- Direct FIFO data addressing with independent BYTE/WORD to DWORD conversion
- Register configurable endianness per data register and FIFO access
- Multiplexed address/data bus
- Single or dual address phases
- Direct FIFO data addressing
- Dynamic endianness
- Demultiplexed address (LAN9254 only)
- Reduced cycle time
- Dynamic endianness

PIN CONNECTIONS IN HBI MODES

LAN9253 HBI Pin Connections

TABLE 1: LAN9253 HBI PIN FUNCTIONS

Number of Pins	Name	Symbol	Description
1	Read	RD	This pin is the host bus read strobe. Normally active low, the polarity can be changed via configuration register settings.
	Read or Write	RD_WR	This pin is the host bus direction control. Used in conjunction with the **ENB** pin, it indicates a read or write operation. The normal polarity is read when 1, write when 0 (R/nW), but can be changed via configuration register settings.
1	Write	WR	This pin is the host bus write strobe. Normally active low, the polarity can be changed via configuration register settings.
	Enable	ENB	This pin is the host bus data enable strobe. Used in conjunction with the **RD_WR** pin, it indicates the data phase of the operation. Normally active low, the polarity can be changed via configuration register settings.
1	Chip Select	CS	This pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via configuration register settings.

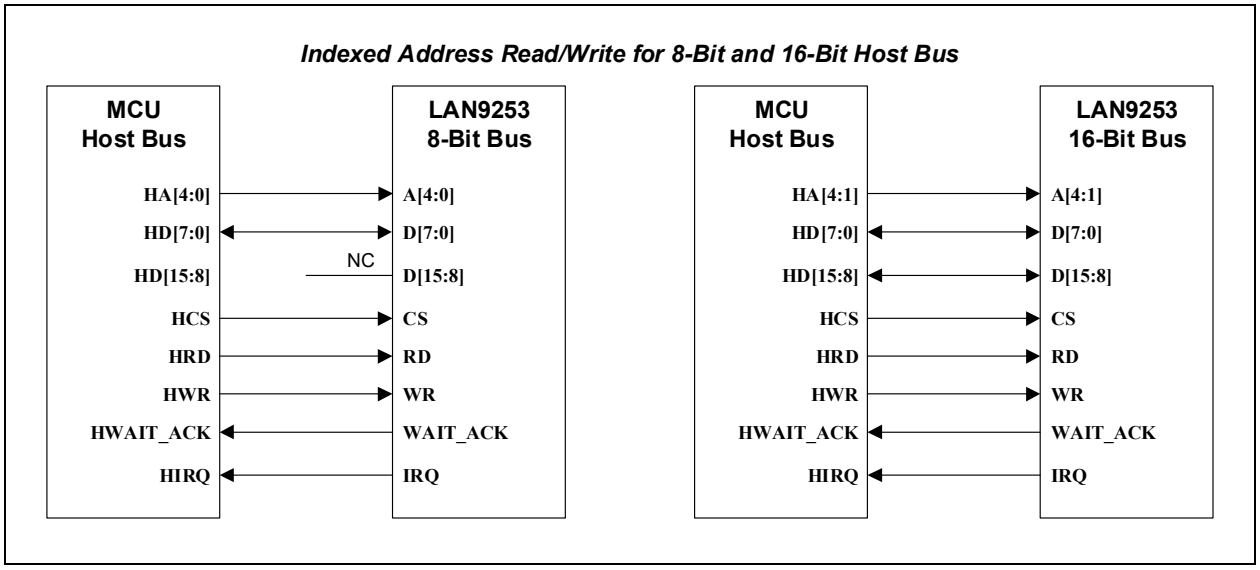
TABLE 1: LAN9253 HBI PIN FUNCTIONS (CONTINUED)

Number of Pins	Name	Symbol	Description
2	Byte Enable	BE1 BE0	In 16-bit Data mode, these pins indicate which bytes are to be written or read. In 8-bit Data mode, these pins are not used. These pins are only available in Multiplexed mode. Normally active low, the polarity can be changed via configuration register settings.
5	Address	A[4:0]	These pins provide the address for Indexed Address mode. In 16-bit Data mode, bit 0 is not used. Address bit 0 is shared with data bit 15.
16	Data	D[15:0]	These pins are the host bus data bus for Non-Multiplexed Address modes. In 8-bit Data mode, bits 15-8 are not used. Their input and output drivers are disabled. Address bit 0 is shared with data bit 15.
	Address and Data	AD[15:0]	These pins are the host bus address/data bus for Multiplexed Address mode. Bits 15-8 provide the upper byte of address for Single Phase Multiplexed Address mode. Bits 7-0 provide the lower byte of address for Single Phase Multiplexed Address mode, and both bytes of address for Dual Phase Multiplexed Address mode. In 8-bit Data Dual Phase Multiplexed Address mode, bits 15-8 are not used. Their input and output drivers are disabled.
1	Address Latch Enable High	ALEHI	This pin indicates the address phase for Multiplexed Address modes. It is used to load the higher address byte in Dual Phase Multiplexed Address mode. Normally active low (address saved on rising edge), the polarity can be changed via configuration register settings.
	EEPROM Emulation ALELO Polarity Strap 0	EE_EMUL_ ALELO_POL	During EEPROM Emulation mode, if the default PDI selection is set to HBI Multiplexed 1 Phase, this strap is used to set the HBI ALE polarity until the EEPROM configuration data has been loaded.
1	Address Latch Enable Low	ALELO	This pin indicates the address phase for Multiplexed Address modes. It is used to load both address bytes in Single Phase Multiplexed Address mode and the lower address byte in Dual Phase Multiplexed Address mode. Normally active low (address saved on rising edge), the polarity can be changed via configuration register settings.
1	Wait/Acknowledge	WAIT_ACK	This pin indicates when the host bus cycle may be finished. This pin is tri-state when the device is not selected. Normally push-pull, the buffer type can be changed to open-drain via configuration register settings. Normally active low indicating wait, for push-pull operation, the polarity can be changed via configuration register settings. This pin is disabled when both bits are low.

LAN9253 Host Bus Interface Indexed Mode and Pins

The LAN9253 provides one 8-bit or 16-bit Indexed mode HBI. The connection between MCU and LAN9253 is shown in Figure 1.

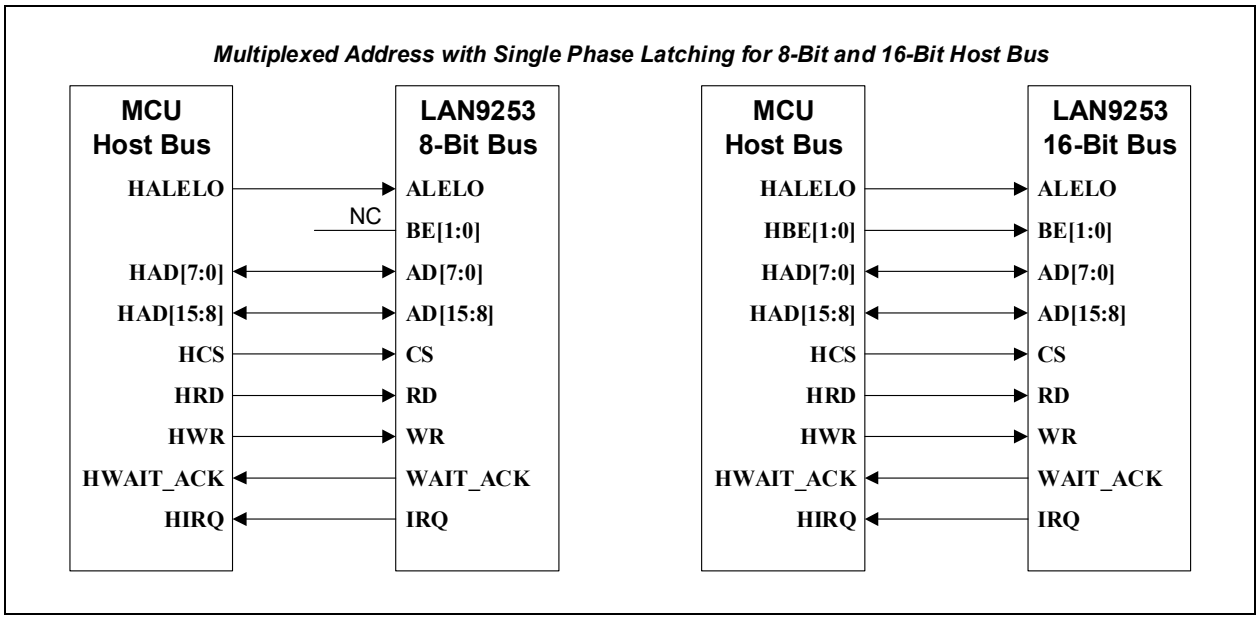
FIGURE 1: CONNECTION BETWEEN LAN9253 AND MCU USING 8-BIT AND 16-BIT HBI



Multiplexed Address with Single Phase Latching for 8-Bit and 16-Bit Host Bus Interface

The LAN9253 provides one multiplexed address with single phase latching for 8-bit and 16-bit HBI. The connection between MCU and LAN9253 is shown in Figure 2.

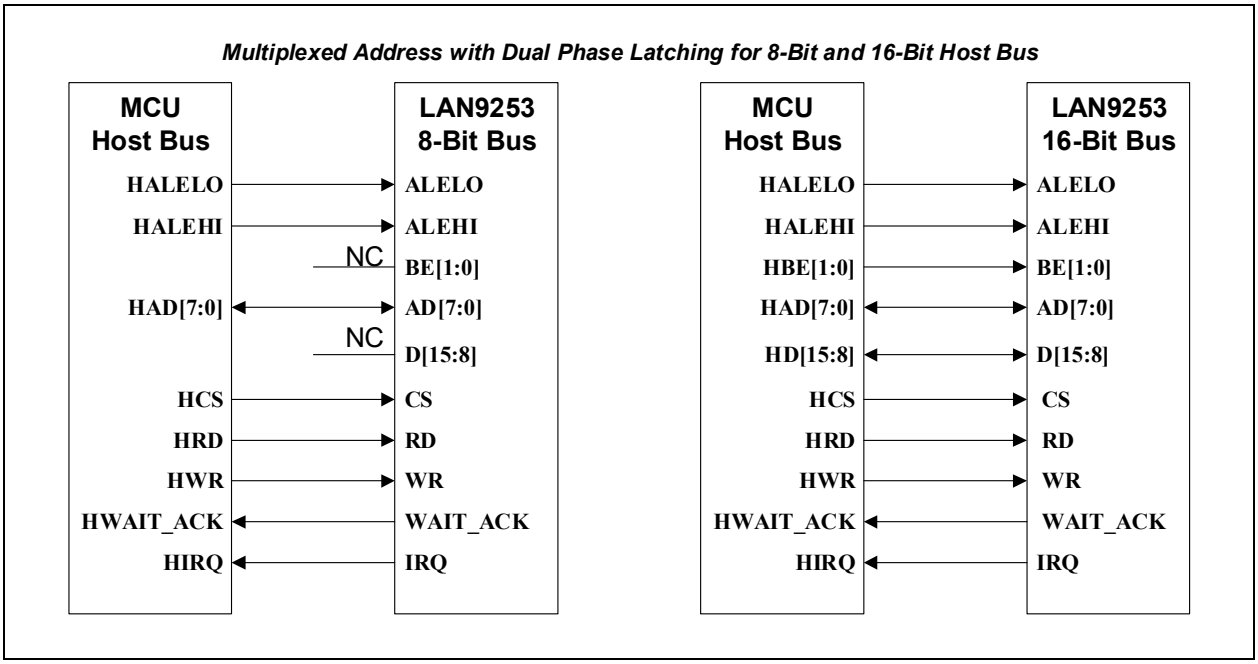
FIGURE 2: CONNECTION BETWEEN LAN9253 AND MCU USING MULTIPLEXED ADDRESS SINGLE PHASE LATCHING MODE FOR 8-BIT AND 16-BIT HBI



Multiplexed Address with Dual Phase Latching for 8-Bit and 16-Bit Host Bus Interface

The LAN9253 provides one multiplexed address with dual phase latching for 8-bit and 16-bit HBI. The connection between MCU and LAN9253 is shown in Figure 3.

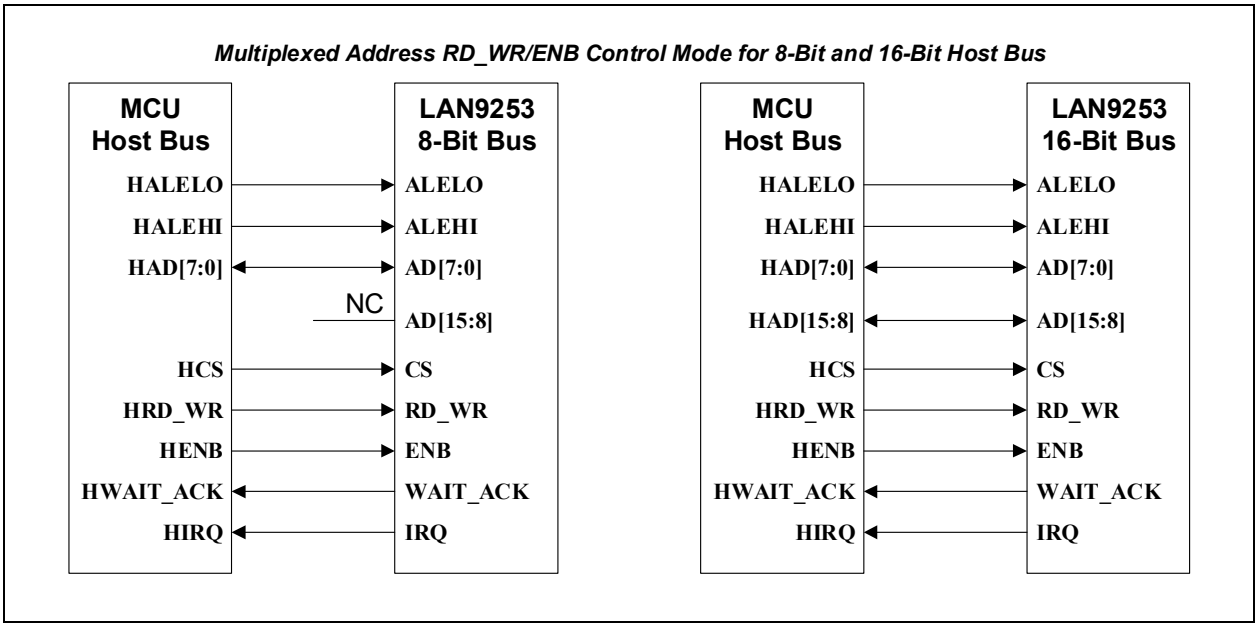
FIGURE 3: CONNECTION BETWEEN LAN9253 AND MCU USING MULTIPLEXED ADDRESS DUAL PHASE LATCHING MODE FOR 8-BIT AND 16-BIT HBI



Multiplexed Address RD_WR/ENB Control Mode for 8-Bit and 16-Bit Host Bus Interface

The LAN9253 provides one multiplexed address RD_WR/ENB control mode for 8-bit and 16-bit HBI. The connection between MCU and LAN9253 is shown in Figure 4.

FIGURE 4: CONNECTION BETWEEN LAN9253 AND MCU USING MULTIPLEXED ADDRESS RD_WR/ENB CONTROL MODE FOR 8-BIT AND 16-BIT HBI



LAN9254 HBI Pin Connections

TABLE 2: LAN9254 HBI PIN FUNCTIONS

Number of Pins	Name	Symbol	Description
1	Read	RD	This pin is the host bus read strobe. Normally active low, the polarity can be changed via configuration register settings.
	Read or Write	RD_WR	This pin is the host bus direction control. Used in conjunction with the **ENB** pin, it indicates a read or write operation. The normal polarity is read when 1, write when 0 (R/nW), but can be changed via configuration register settings.
1	Write	WR	This pin is the host bus write strobe. Normally active low, the polarity can be changed via configuration register settings.
	Enable	ENB	This pin is the host bus data enable strobe. Used in conjunction with the **RD_WR** pin, it indicates the data phase of the operation. Normally active low, the polarity can be changed via configuration register settings.
1	Chip Select	CS	This pin is the host bus chip select and indicates that the device is selected for the current transfer. Normally active low, the polarity can be changed via configuration register settings.
2	Byte Enable	BE1 BE0	In 16-bit Data mode, these pins indicate which bytes are to be written or read. In 8-bit Data mode, these pins are not used. These pins are only available in Multiplexed mode. Normally active low, the polarity can be changed via configuration register settings.
16	Address	A[15:0]	These pins provide the address for Indexed and Demultiplexed Address modes. In 16-bit Data mode, bit 0 is not used. Address bit 0 is shared with data bit 15. In Indexed Address mode, A[15:5] are not used.
16	Data	D[15:0]	These pins are the host bus data bus for Non-Multiplexed Address modes. In 8-bit Data mode, bits 15-8 are not used. Their input and output drivers are disabled. Address bit 0 is shared with data bit 15.
	Address and Data	AD[15:0]	These pins are the host bus address/data bus for Multiplexed Address mode. Bits 15-8 provide the upper byte of address for Single Phase Multiplexed Address mode. Bits 7-0 provide the lower byte of address for Single Phase Multiplexed Address mode and both bytes of address for Dual Phase Multiplexed Address mode. In 8-bit Data Dual Phase Multiplexed Address mode, bits 15-8 are not used. Their input and output drivers are disabled.

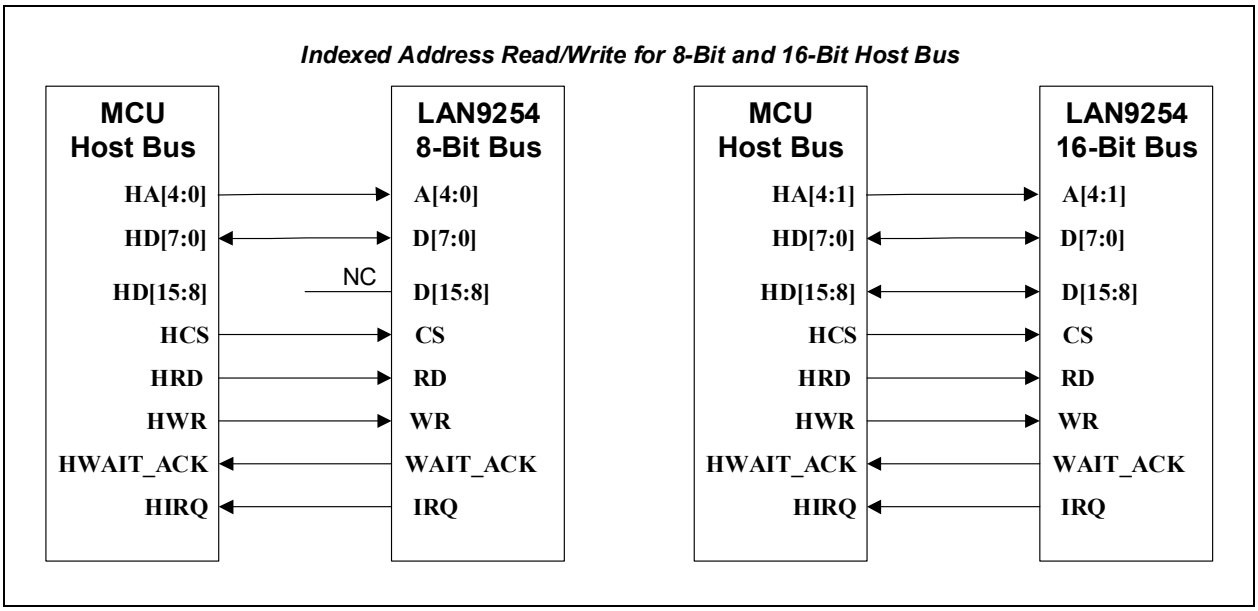
TABLE 2: LAN9254 HBI PIN FUNCTIONS (CONTINUED)

Number of Pins	Name	Symbol	Description
1	Address Latch Enable High	ALEHI	This pin indicates the address phase for Multiplexed Address modes. It is used to load the higher address byte in Dual Phase Multiplexed Address mode. Normally active low (address saved on rising edge), the polarity can be changed via configuration register settings.
	EEPROM Emulation ALELO Polarity Strap 0	EE_EMUL_ ALELO_POL	During EEPROM Emulation mode, if the default PDI selection is set to HBI Multiplexed 1 Phase, this strap is used to set the HBI ALE polarity until the EEPROM configuration data has been loaded.
1	Address Latch Enable Low	ALELO	This pin indicates the address phase for Multiplexed Address modes. It is used to load both address bytes in Single Phase Multiplexed Address mode and the lower address byte in Dual Phase Multiplexed Address mode. Normally active low (address saved on rising edge), the polarity can be changed via configuration register settings.
1	Wait/Acknowledge	WAIT_ACK	This pin indicates when the host bus cycle may be finished. This pin is tri-state when the device is not selected. Normally push-pull, the buffer type can be changed to open-drain via configuration register settings. Normally active low indicating wait, for push-pull operation, the polarity can be changed via configuration register settings. This pin is disabled when both bits are low.
1	Endianness Select	END_SEL	This pin provides the endianness control for Demultiplexed Address mode. A high on the pin selects big endian mode and a low on the pin selects little endian mode. This can be dynamically changed or held static.

LAN9254 Host Bus Interface Indexed Mode and Pins

The LAN9254 provides one 8-bit or 16-bit Indexed mode HBI. The connection between MCU and LAN9254 is shown in Figure 5.

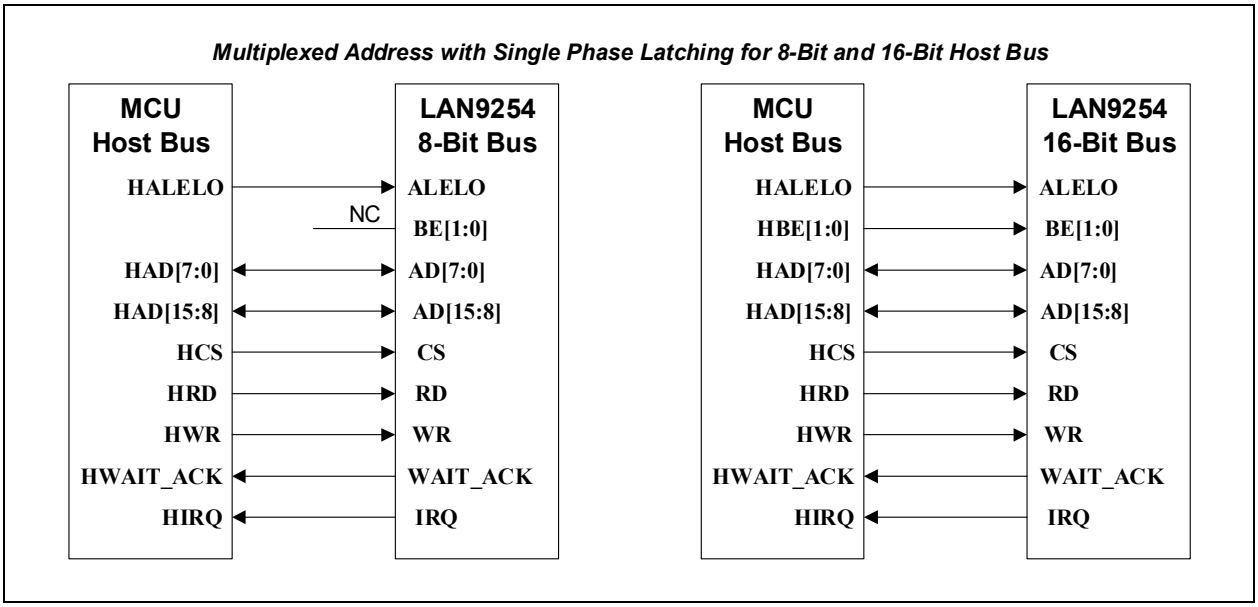
FIGURE 5: CONNECTION BETWEEN LAN9254 AND MCU USING 8-BIT AND 16-BIT HBI



Multiplexed Address with Single Phase Latching for 8-Bit and 16-Bit Host Bus Interface

The LAN9254 provides one multiplexed address with single phase latching for 8-bit and 16-bit HBI. The connection between MCU and LAN9254 is shown in Figure 6.

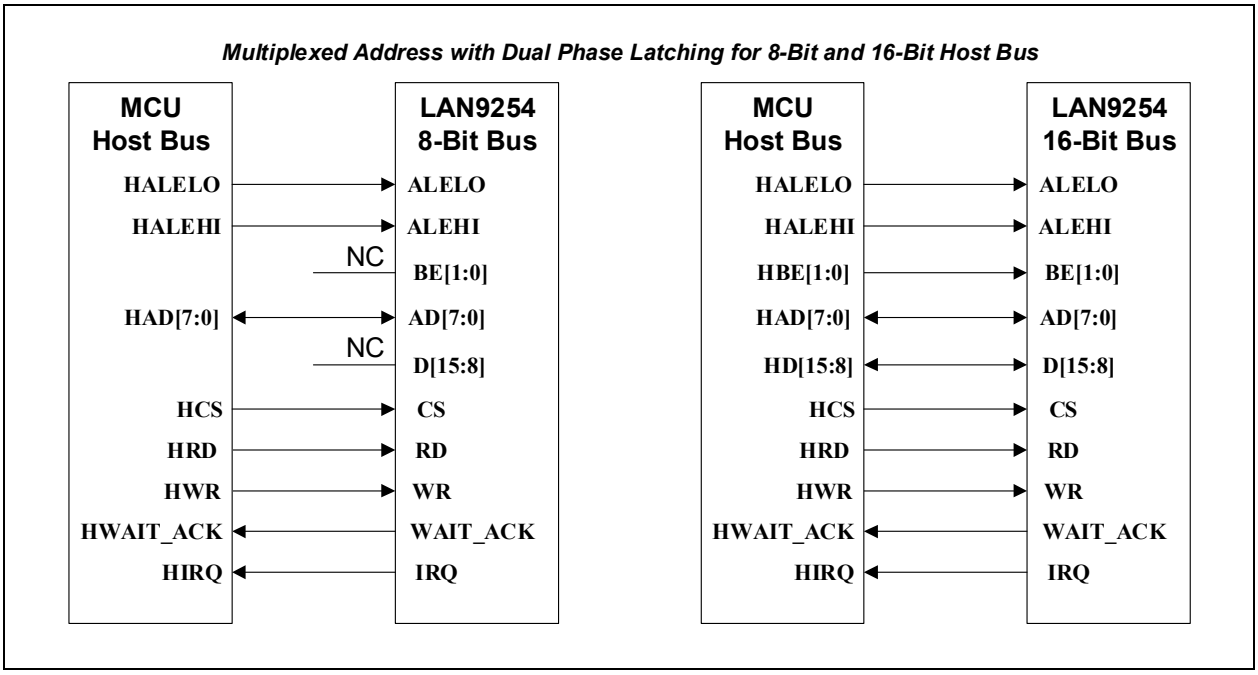
FIGURE 6: CONNECTION BETWEEN LAN9254 AND MCU USING MULTIPLEXED ADDRESS SINGLE PHASE LATCHING MODE FOR 8-BIT AND 16-BIT HBI



Multiplexed Address with Dual Phase Latching for 8-Bit and 16-Bit Host Bus Interface

The LAN9254 provides one multiplexed address with dual phase latching for 8-bit and 16-bit HBI. The connection between MCU and LAN9254 is shown in Figure 7.

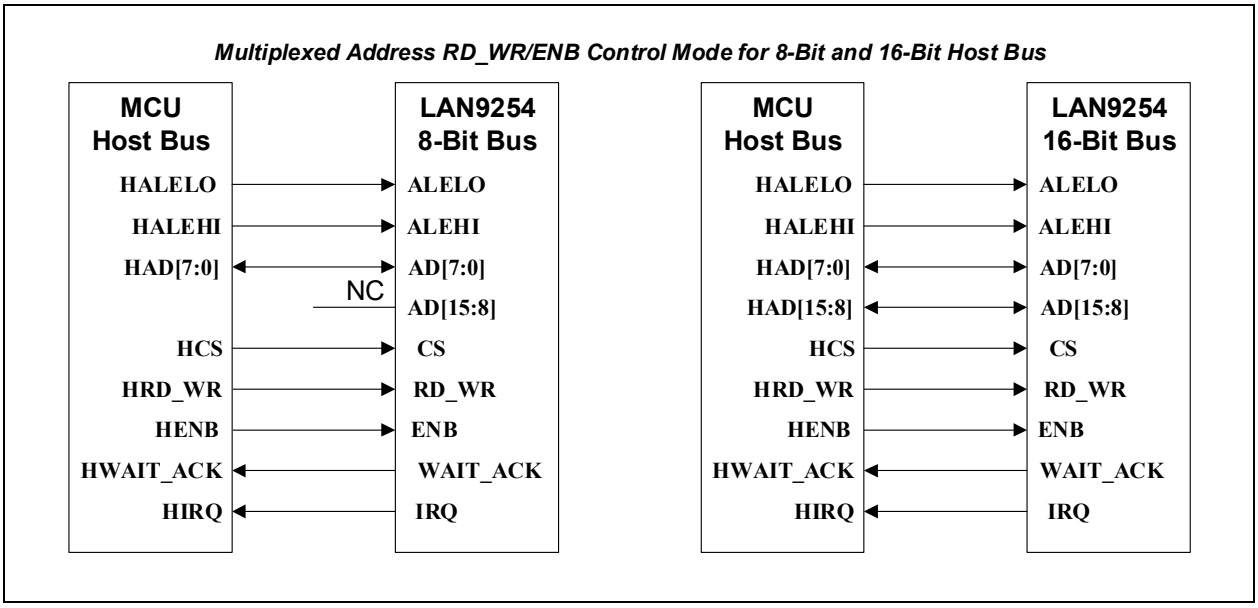
FIGURE 7: CONNECTION BETWEEN LAN9254 AND MCU USING MULTIPLEXED ADDRESS DUAL PHASE LATCHING MODE FOR 8-BIT AND 16-BIT HBI



Multiplexed Address RD_WR/ENB Control Mode for 8-Bit and 16-Bit Host Bus Interface

The LAN9254 provides one multiplexed address RD_WR/ENB control mode for 8-bit and 16-bit HBI. The connection between MCU and LAN9254 is shown in Figure 8.

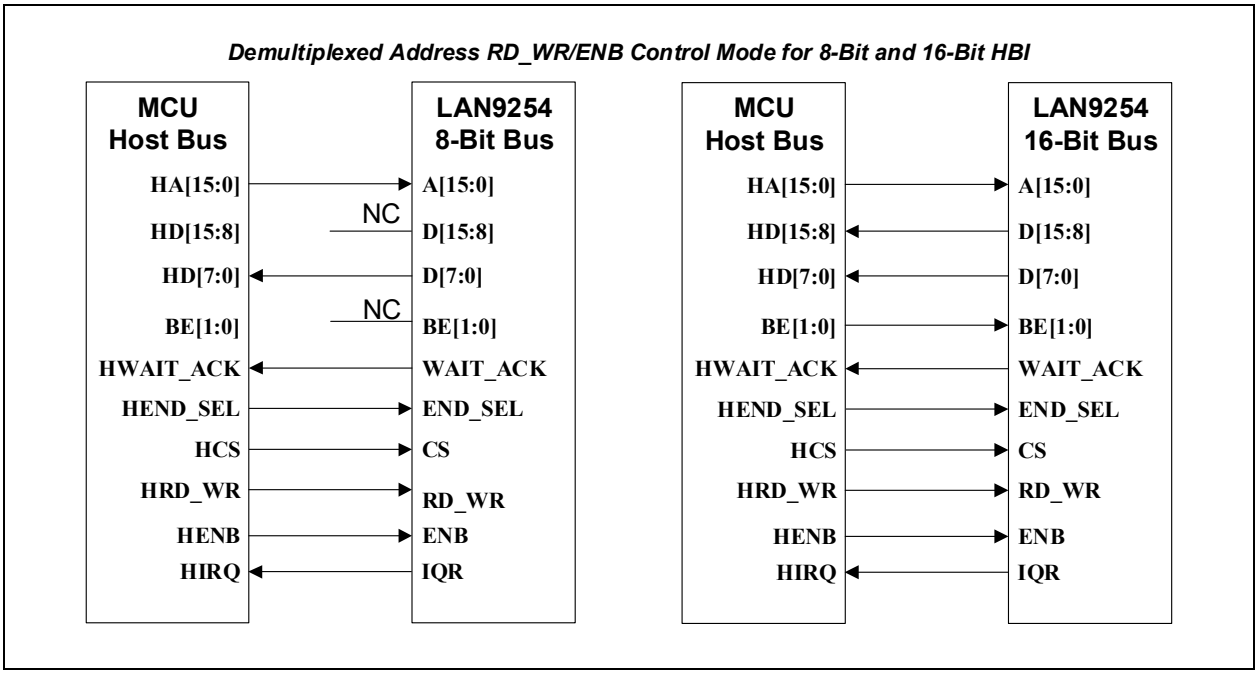
FIGURE 8: CONNECTION BETWEEN LAN9254 AND MCU USING MULTIPLEXED ADDRESS RD_WR/ENB CONTROL MODE FOR 8-BIT AND 16-BIT HBI



Demultiplexed Address RD_WR/ENB Control Mode for 8-Bit and 16-Bit HBI

The LAN9254 provides one Demultiplexed Address RD_WR/ENB Control mode for 8-bit and 16-bit HBI. The connection between MCU and LAN9254 is shown in Figure 9.

FIGURE 9: CONNECTION BETWEEN LAN9254 AND MCU USING DEMULTIPLEXED ADDRESS RD_WR/ENB CONTROL MODE FOR 8-BIT AND 16-BIT HBI



HBI PDI CONFIGURATION

Process Data Interface (PDI) Registers

The PDI Configuration Register (0x0150) and the PDI Extended Configuration Register (0x0152:0x0153) are initialized from the contents of the EEPROM. The LAN9253 and LAN9254 data sheets describe these registers in detail.

HBI Configuration

The 2-port or 3-port configuration must first be selected using the Chip Mode configuration. The mode of the chip is controlled by the CHIP_MODE[1:0] configuration straps as shown in Table 3.

TABLE 3: CHIP MODE SELECTION

CHIP_MODE[1:0]	Mode
0x	2-Port mode: Port 0 = PHY A, Port 1 = PHY B
10	3-Port Downstream mode: Port 0 = PHY A, Port 1 = PHY B, Port 2 = MII
11	3-Port Upstream mode: Port 0 = MII, Port 1 = PHY B, Port 2 = PHY A

Note 1: Chip modes 10 and 11 are not supported in Parallel Interface.

Once the mode of the chip is selected, the PDI in use is selected by the Process Data Interface (PDI_SELECT) field of the PDI Control Register. The valid choices are shown in Table 4.

TABLE 4: PDI MODE SELECTION

PDI_SELECT	PDI Mode	EtherCAT® Direct Mapped Mode
0x88	HBI Multiplexed 1 Phase 8-bit	No
0x89	HBI Multiplexed 1 Phase 16-bit	No
0x8A	HBI Multiplexed 2 Phase 8-bit	No
0x8B	HBI Multiplexed 2 Phase 16-bit	No
0x8C	HBI Indexed 8-bit	No
0x8D	HBI Indexed 16-bit	No
0x8E	HBI Demultiplexed 8-bit	No
0x8F	HBI Demultiplexed 16-bit	No
0x90	HBI Multiplexed 1 Phase 8-bit	Yes
0x91	HBI Multiplexed 1 Phase 16-bit	Yes
0x92	HBI Multiplexed 2 Phase 8-bit	Yes
0x93	HBI Multiplexed 2 Phase 16-bit	Yes
0x94	HBI Multiplexed 2 Phase 16-bit	Yes
0x95	HBI Indexed 16-bit	Yes
0x96	HBI Demultiplexed 8-bit	Yes
0x97	HBI Demultiplexed 16-bit	Yes

HBI Sub-Configuration

The PDI Configuration Register and the Extended PDI Configuration Register are used for the HBI configuration straps as shown in Table 5. The PDI Configuration Register and the Extended PDI Configuration Register are initialized from the contents of the EEPROM. The data sheet provides information about these configuration registers.

TABLE 5: ETHERCAT® CORE EEPROM CONFIGURABLE REGISTERS

Register	Bits	EEPROM Word/[Bits]
PDI Control Register (0140h)	[7:0] Process Data Interface (PDI_SELECT)	0 / [7:0]
ESC Configuration Register (0141h)	[7] (unused)	—
	[6] Enhanced Link Port 2	0 / [14]
	[5] Enhanced Link Port 1	0 / [13]
	[4] Enhanced Link Port 0	0 / [12]
	[3] Distributed Clocks Latch In Unit Note: Bit 3 is NOT set by EEPROM.	—
	[2] Distributed Clocks SYNC Out Unit Note: Bit 2 is NOT set by EEPROM.	—
	[1] Enhanced Link Detection All Ports	0 / [9]
	[0] Device Emulation (control of AL Status Register)	0 / [8]
PDI Configuration Register (0150h) HBI Mode	[7] HBI ALE Qualification	1 / [7]
	[6] HBI Read/Write Mode	1 / [6]
	[5] HBI Chip Select Polarity	1 / [5]
	[4] HBI Read, Read/Write Polarity	1 / [4]
	[3] HBI Write, Enable Polarity	1 / [3]
	[2] HBI ALE Polarity	1 / [2]
	[1] HBI WAIT_ACK Polarity	1 / [1]
	[0] HBI WAIT_ACK Buffer Type	1 / [0]
Sync/Latch PDI Configuration Register (0151h)	[7] SYNC1 Map	1 / [15]
	[6] SYNC1/LATCH1 Configuration	1 / [14]
	[5:4] SYNC1 Output Driver/Polarity	1 / [13:12]
	[3] SYNC0 Map	1 / [11]
	[2] SYNC0/LATCH0 Configuration	1 / [10]
	[1:0] SYNC0 Output Driver/Polarity	1 / [9:8]
Pulse Length of SyncSignals Register (0982h-0983h)	[15:0] Pulse length of SyncSignals	2 / [15:0]
Extended PDI Configuration Register (0152h-0153h) HBI Modes	[15:3] RESERVED	3 / [15:3]
	[2] HBI BE1/BE0 Polarity	3 / [2]
	[1] Perform Internal Write	3 / [1]
	[0] Read WAIT_ACK Removal Delay	3 / [0]
Configured Station Alias Register (0012h-0013h)	[15:0] Configured Station Alias Address	4 / [15:0]

TABLE 5: ETHERCAT® CORE EEPROM CONFIGURABLE REGISTERS (CONTINUED)

Register	Bits	EEPROM Word/[Bits]
MII Management Control/Status Register (0510h-0511h)	[2] MI Link Detection	5 / [15]
ASIC Configuration Register (0142h-0143h)	[15] MI Link Detection	
	[14] ERRLED Enable	5 / [14]
	[13:8] RESERVED	5 / [13:8]
	[7] MI Write Gigabit Register 9 Enable	5 / [7]
	[6] STATE_RUNLED Mode Select	5 / [6]
	[5:0] RESERVED	5 / [5:0]
RESERVED Register (0144h-0145h)	[15:0] RESERVED	6 / [15:0]

HBI PERFORMANCE

The section examines the difference in performance between multiplexed and demultiplexed interfaces of LAN9253 and LAN9254 devices.

Several factors that affect the HBI performance include the number of bits of the register being accessed, the HBI configuration mode, and if Direct or Indirect Addressing Mapping mode is being used for the EtherCAT Core Registers.

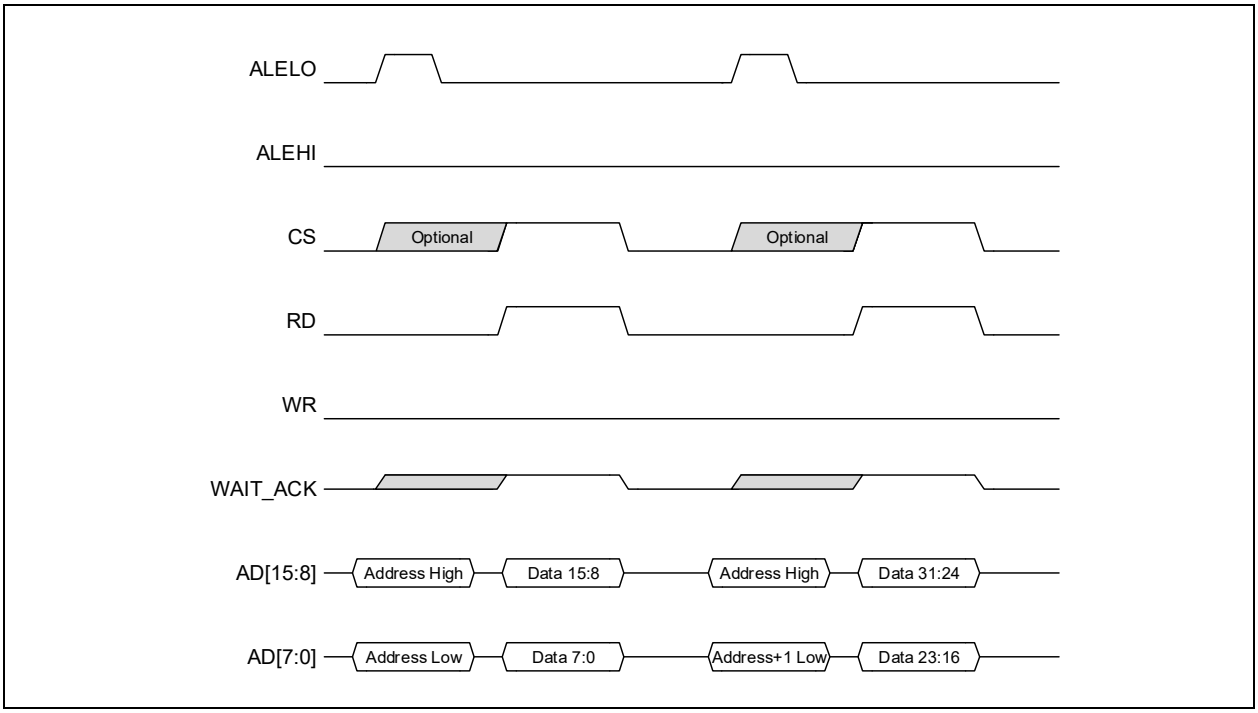
For these results, the fastest HBI mode on the LAN9254, which is Demultiplexed Addressing and Direct Addressing Mapping mode, are discussed. For the LAN9253, the fastest mode is Multiplexed Addressing and Direct Addressing Mapping mode. The examples are for addressing 16-bit registers.

LAN9253 Multiplexed Address Mode Configuration

LAN9253 MULTIPLEXED READ TIMING

The read access time or the time to read 16-bit of data is shown in Figure 10.

FIGURE 10: MULTIPLEXED ADDRESSING WITH SINGLE PHASE LATCHING - 16-BIT READ



The read cycle time to read 16-bit of data is shown in Figure 11.

FIGURE 11: MULTIPLEXED ADDRESSING READ CYCLE TIMING

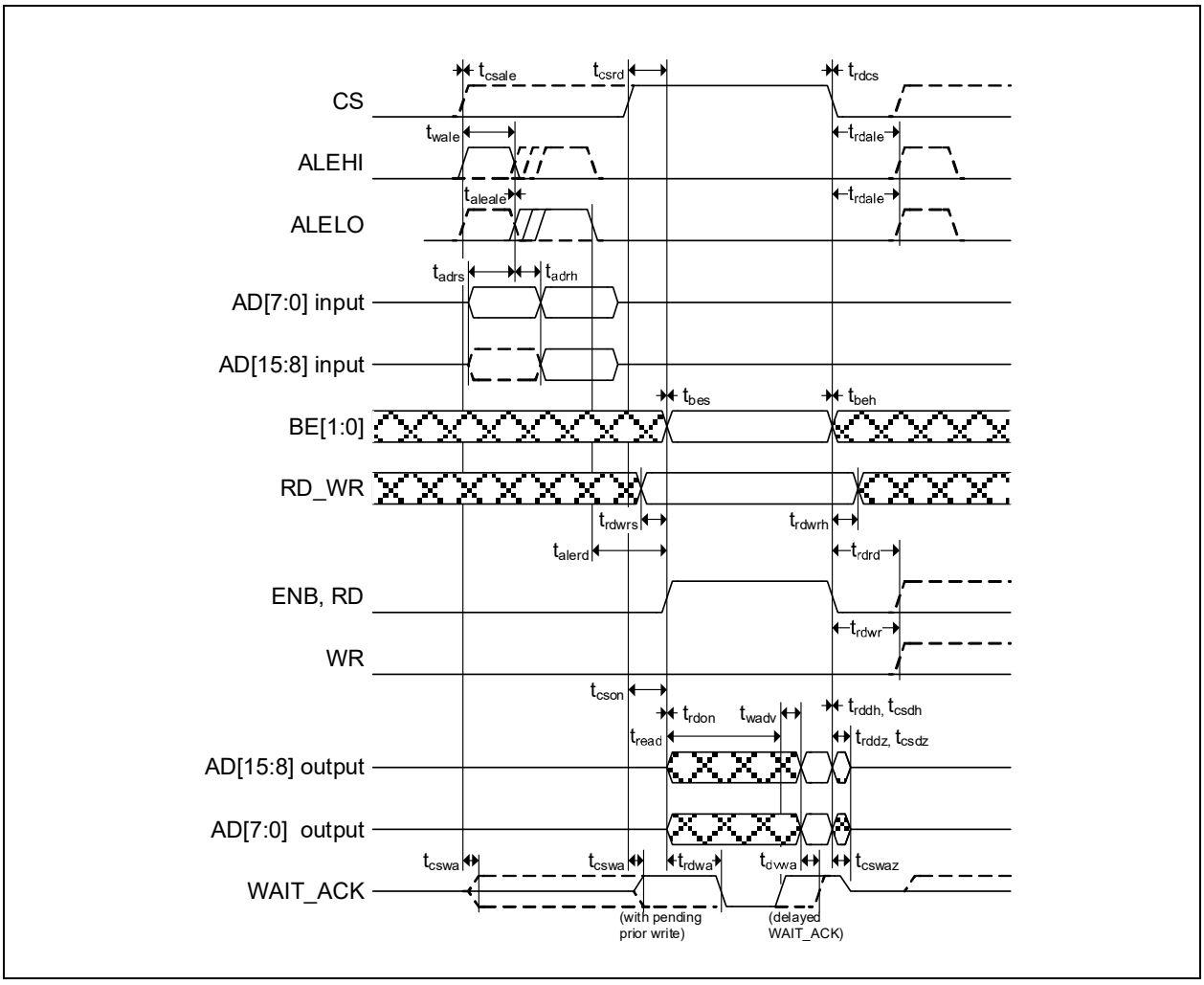


Table 6 shows the timing required to read 16-bit of data.

TABLE 6: MULTIPLEXED ADDRESSING READ CYCLE TIMING

Symbol	Description	Time (ns)
t_{adrs}	Address Setup to ALELO, ALEHI Inactive	10
t_{alerd}	ALELO, ALEHI Inactive to RD or ENB Active	5
t_{read}	RD or ENB Active to WAIT_ACK Inactive (16 bit read, no prior write)	315
t_{wadv}	WAIT_ACK Inactive to Data Valid - Normal WAIT_ACK	5
t_{rdrd}	RD or ENB Deassertion Time before Next RD or ENB	13
Total		**348**

LAN9253 MULTIPLEXED WRITE TIMING (NON-POSTED WRITES)

Figure 12 and Figure 13 show the access time and cycle time to write 16-bit of data using non-posted writes.

FIGURE 12: MULTIPLEXED ADDRESSING WITH SINGLE PHASE LATCHING - 16-BIT WRITE

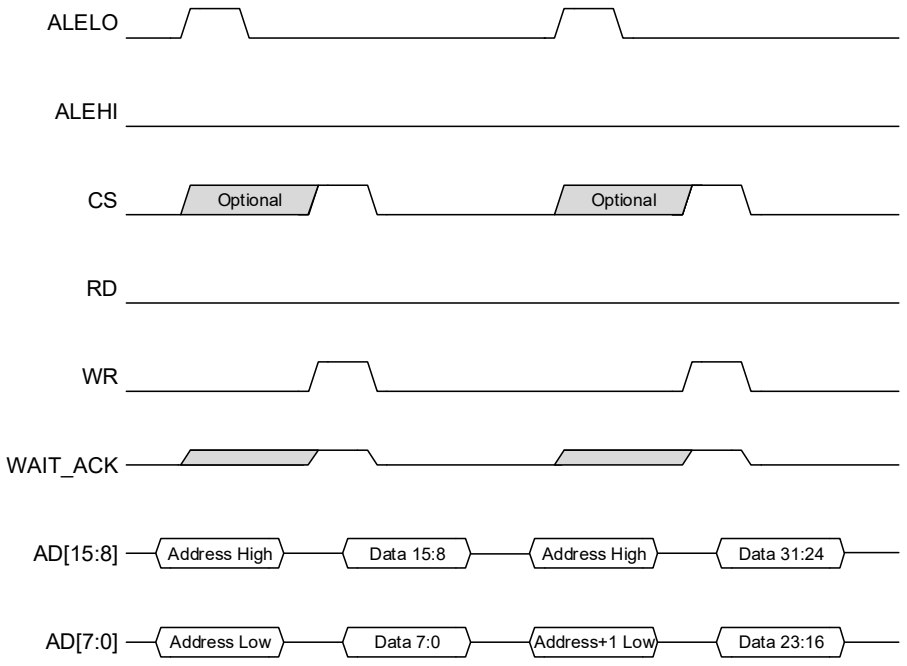


FIGURE 13: MULTIPLEXED ADDRESSING WRITE CYCLE TIMING

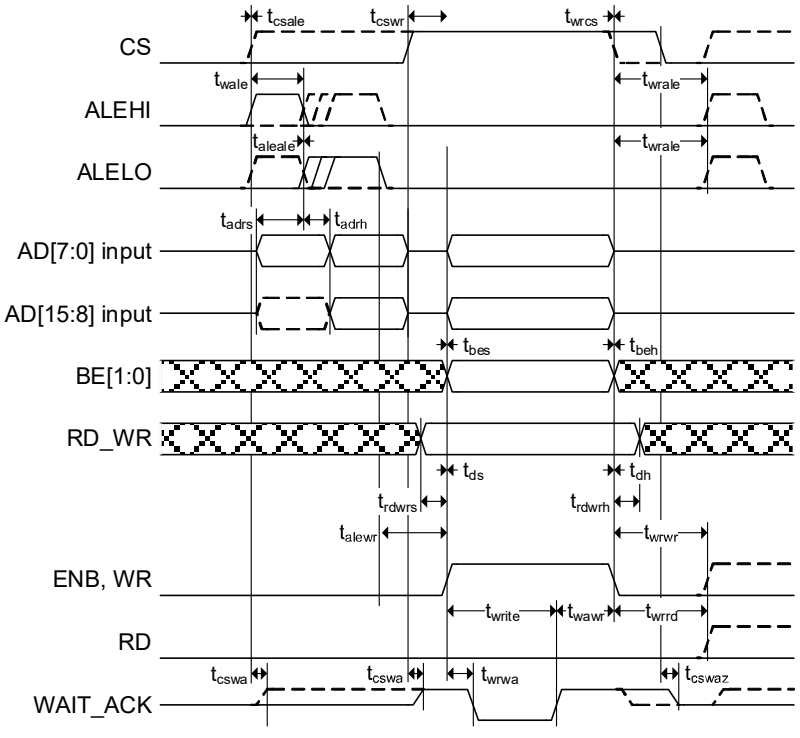


Table 7 shows the timing required to write 16-bit of data.

TABLE 7: MULTIPLEXED ADDRESSING WRITE CYCLE TIMING

Symbol	Description	Time (ns)
t_{adrs}	Address Setup to ALELO, ALEHI Inactive	10
t_{alewr}	ALELO, ALEHI Inactive to WR or ENB Active	5
t_{write}	WR or ENB Active to WAIT_ACK Inactive - Pending prior 16-bit write	280
t_{wawr}	WAIT_ACK Inactive to WR or ENB Inactive	0
t_{wrwr} (Note 1)	WR or ENB Deassertion Time before Next WR or ENB	13
Total		**308**

Note 1: t_{wrwr} should be 160 ns for EtherCAT core registers.

LAN9254 Demultiplexed Address Mode Configuration

LAN9254 DEMULTIPLEXED READ TIMING

Figure 14 shows the read access time to read 16-bit of data.

FIGURE 14: DEMULTIPLEXED ADDRESSING - 16-BIT READ

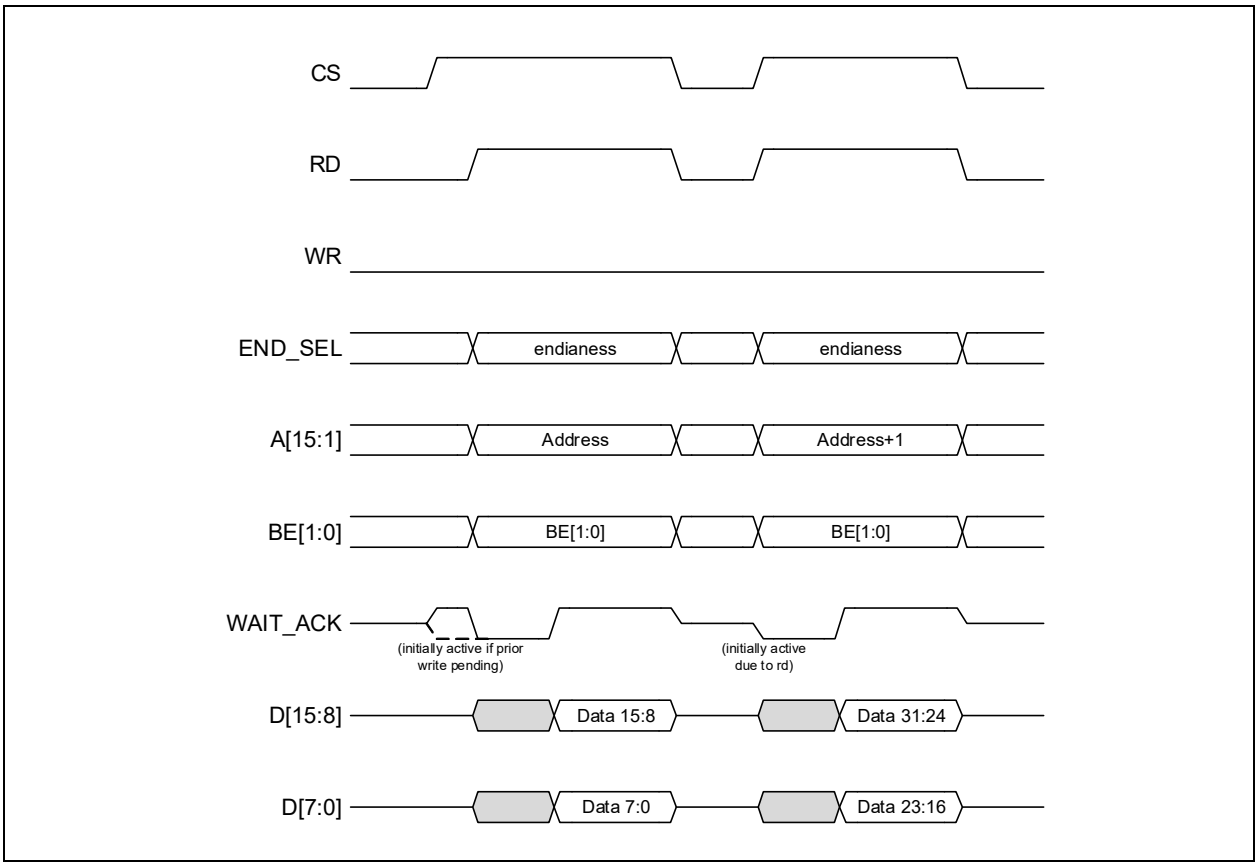


Figure 15 shows the read cycle time to read 16-bit of the data.

FIGURE 15: DEMULTIPLEXED ADDRESSING READ CYCLE TIMING

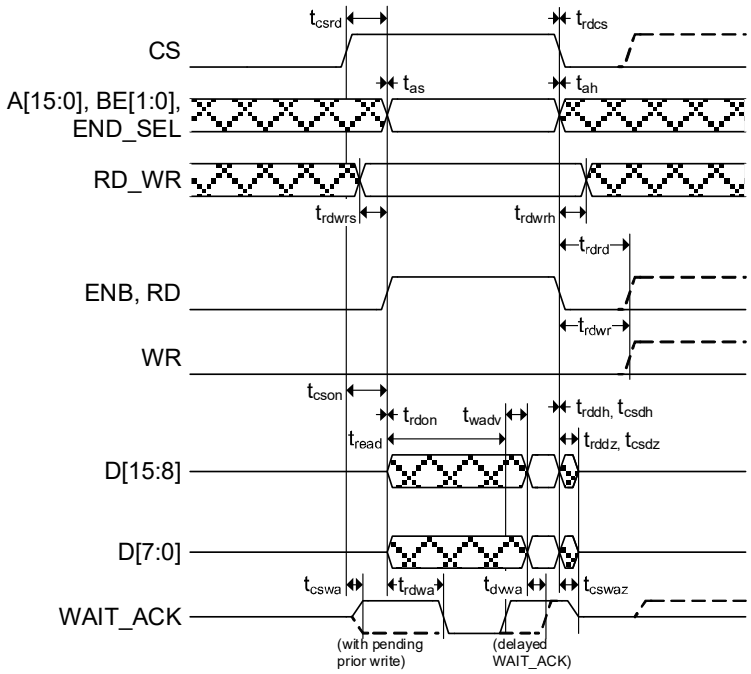


Table 8 shows the timing required to read 16-bit of data.

TABLE 8: DEMULTIPLEXED ADDRESSING READ CYCLE TIMING

Symbol	Description	Time (ns)
t_{csrd}	CS Setup to RD or ENB Active	0
t_{read}	RD or ENB Active to WAIT_ACK Inactive (16 bit read, no prior write)	315
t_{wadv}	WAIT_ACK Inactive to Data Valid - Normal WAIT_ACK	5
t_{rdrd}	RD or ENB Deassertion Time before Next RD or ENB	13
Total		**333**

LAN9254 DEMULTIPLEXED WRITE TIMING (NON-POSTED WRITES)

Figure 16 shows the non-posted write access time to write 16-bit of data.

FIGURE 16: DEMULTIPLEXED ADDRESSING - 16-BIT NON-POSTED WRITE

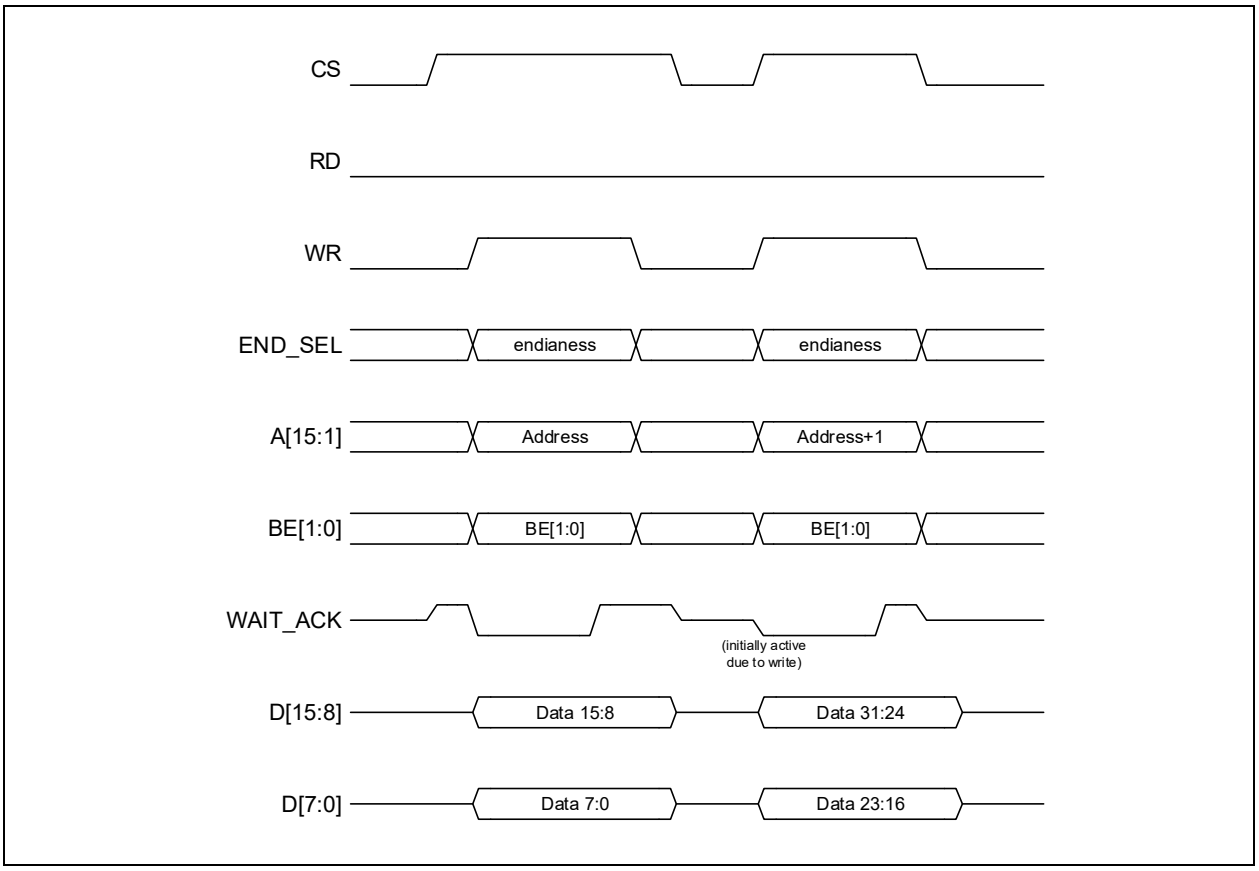


Figure 17 shows the non-posted write cycle time to write 16-bit of data.

FIGURE 17: DEMULTIPLEXED ADDRESSING NON-POSTED WRITE CYCLE TIMING

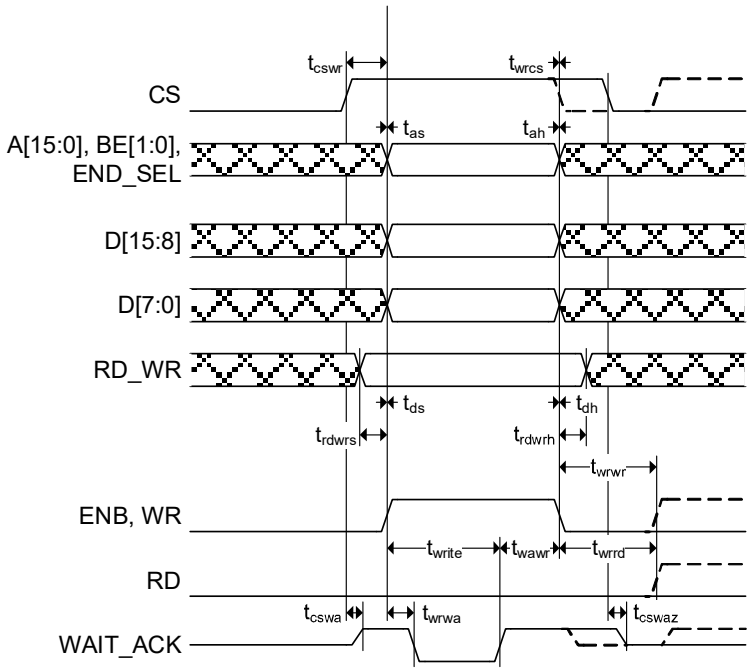


Table 9 shows the timing required to write 16-bit of data.

TABLE 9: DEMULTIPLEXED ADDRESSING WRITE CYCLE TIMING

Symbol	Description	Time (ns)
t_{cswr}	CS Setup to WR or ENB Active	0
t_{write}	WR or ENB Active to WAIT_ACK Inactive - Pending prior 16-bit write	280
t_{wawr}	WAIT_ACK Inactive to WR or ENB Inactive	0
t_{wrwr}	WR or ENB Deassertion Time before Next WR or ENB	13
Total		**293**

SUMMARY

This application note describes the HBI PDI read and write access timings and shows that the demultiplex EtherCAT direct mapped registers read and write access timings are the least among all the available options.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003764A (12-17-20)	Initial release	

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