AN4784

LAN8840 Register Definitions

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1.0 INTRODUCTION

The LAN8840 Register Definitions application note provides a description of all customer-facing registers within the LAN8840 device and is meant for clarification of functionality during design and debugging.

2.0 SECTIONS

This application note covers the following sections:

- Section 4.0, Register Maps
- Section 5.0, Register Definitions

3.0 REFERENCES

Consult the following documents for details on the specific parts referred to in this application note. The first three references include high-level descriptions intended for software design and configuration:

- *LAN8840 Data Sheet*
- *LAN8840 Hardware Design Checklist*

3.1 Register Nomenclature

Table 1 describes the register bit attributes used throughout this document.

TABLE 1: REGISTER BIT TYPES

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read only:** Read only. Writes have no effect.
WO	**Write only:** If a register or bit is write-only, reads will return unspecified data.
W1S	**Write One to Set:** Writing a one sets the value. Writing a zero has no effect.
W1C	**Write One to Clear:** Writing a one clears the value. Writing a zero has no effect.
WAC	**Write Anything to Clear:** Writing anything clears the value.
RC	**Read to Clear:** Contents are cleared after the read. Writes have no effect.
LL	**Latch Low:** Clear on read of register.
LH	**Latch High:** Clear on read of register.
SC	**Self-Clearing:** Contents is self-cleared after the being set. Writes of zero have no effect. Contents can be read.
RO/LH	**Read Only, Latch High:** This mode is used by the Ethernet PHY registers. Bits with this attribute will stay high until the bit is read. After a read, the bit will remain high, but will change to low if the condition that caused the bit to go high is removed. If the bit has not been read, the bit will remain high regardless of if its cause has been removed.
NASR	**Not Affected by Software Reset.** The state of NASR bits does not change on assertion of a software Reset.
RESERVED	**Reserved Field:** Reserved fields must be written with zeros, unless otherwise indicated, to ensure future compatibility. The value of reserved bits is not guaranteed on a read.

4.0 REGISTER MAPS

The register space within the LAN8840 consists of two distinct areas.

- Standard Registers (Direct register access)
- MDIO Manageable Device (MMD) Registers (Indirect register access)

The LAN8840 supports the following standard registers. These registers are accessed through the SMI (MDIO/MDC) interface.

TABLE 2: STANDARD REGISTERS

Index (in decimal)	Index (in hex)	Register Name
IEEE-Defined Registers		
0	0	Basic Control Register
1	1	Basic Status Register
2	2	Device Identifier 1 Register
3	3	Device Identifier 2 Register
4	4	Auto-Negotiation Advertisement Register
5	5	Auto-Negotiation Link Partner Base Page Ability Register
6	6	Auto-Negotiation Expansion Register
7	7	Auto-Negotiation Next Page TX Register
8	8	Auto-Negotiation Next Page RX Register
9	9	Auto-Negotiation Master Slave Control Register
10	Ah	Auto-Negotiation Master Slave Status Register
11-12	Bh-Ch	RESERVED
13	Dh	MMD Access Control Register
14	Eh	MMD Access Address/Data Register
15	Fh	Extended Status Register
Vendor-Specific Registers		
16	10h	RESERVED
17	11h	PCS Loopback Swap/Polarity Control Register
18	12h	LinkMD Cable Diagnostic Register
19	13h	Digital PMA/PCS Status Register
20	14h	RESERVED
21	15h	RXER Counter Register
22	16h	LED Mode Select Register
23	17h	LED Behavior Register
24	18h	RESERVED
25	19h	Output Control Register
26	1Ah	KSZ9031 LED Mode Register
27	1Bh	Interrupt Status Register
28	1Ch	Auto-MDI/MDI-X Register
29	1Dh	Software Power Down Control Register
30	1Eh	External Loopback Register
31	1Fh	Control Register

The device supports the following MMD device addresses and their associated register addresses, which make up the indirect MMD registers.

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
1	225	E1h	Mean Slicer Error Register
	226	E2h	DCQ Mean Square Error Register
	227	E3h	DCQ Mean Square Error Worst Case Register
	228	E4h	DCQ SQI Register
	229	E5h	DCQ Peak MSE Register
	230	E6h	DCQ Control Register
	231	E7h	DCQ Configuration Register
	232-238	E8h-EEh	DCQ SQI Table Registers
2	0	0h	Common Control Register
	1	1h	Strap Status Register
	2	2h	Operation Mode Strap Override Register
	3	3h	Operation Mode Strap Register
	4	4h	Clock Invert and Control Signal Pad Skew Register
	5	5h	RGMII RX Data Pad Skew Register
	6	6h	RGMII TX Data Pad Skew Register
	7	7h	RESERVED
	8	8	Clock Pad Skew Register
	9	9	Self-Test Packet Count LO Register
	10	Ah	Self-Test Packet Count HI Register
	11	Bh	Self-Test Status Register
	12	Ch	Self-Test Frame Count Enable Register
	13	Dh	Self-Test PGEN Enable Register
	14	Eh	Self-Test Enable Register
	15	Fh	RESERVED
	16	10h	Wake-On-LAN Control Register
	17	11h	Wake-On-LAN-MAC-LO Register
	18	12h	Wake-On-LAN-MAC-MI Register
	19	13h	Wake-On-LAN-MAC-HI Register
	20	14h	Customized-Pkt-0-CRC-LO Register
	21	15h	Customized-Pkt-0-CRC-HI Register
	22	16h	Customized-Pkt-1-CRC-LO Register
	23	17h	Customized-Pkt-1-CRC-HI Register
	24	18h	Customized-Pkt-2-CRC-LO Register
	25	19h	Customized-Pkt-2-CRC-HI Register
	26	1Ah	Customized-Pkt-3-CRC-LO Register
	27	1Bh	Customized-Pkt-3-CRC-HI Register
	28	1Ch	Customized-Pkt-0-MASK_LL Register
	29	1Dh	Customized-Pkt-0-MASK_LH Register
	30	1Eh	Customized-Pkt-0-MASK_HL Register
	31	1Fh	Customized-Pkt-0-MASK_HH Register
	32	20h	Customized-Pkt-1-MASK_LL Register
	33	21h	Customized-Pkt-1-MASK_LH Register

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	34	22h	Customized-Pkt-1-MASK_HL Register
	35	23h	Customized-Pkt-1-MASK_HH Register
	36	24h	Customized-Pkt-2-MASK_LL Register
	37	25h	Customized-Pkt-2-MASK_LH Register
	38	26h	Customized-Pkt-2-MASK_HL Register
	39	27h	Customized-Pkt-2-MASK_HH Register
	40	28h	Customized-Pkt-3-MASK_LL Register
	41	29h	Customized-Pkt-3-MASK_LH Register
	42	2Ah	Customized-Pkt-3-MASK_HL Register
	43	2Bh	Customized-Pkt-3-MASK_HH Register
	44	2Ch	Wake-on-LAN Control Status Register
	45	2Dh	Wake-on-LAN Custom Packet Receive Status Register
	46	2Eh	Wake-on-LAN Magic Packet Receive Status Register
	47	2Fh	Wake-on-LAN Data Module Status Register
	48	30h	Customized Pkt-0 Received CRC-L Register
	49	31h	Customized Pkt-0 Received CRC-H Register
	50	32h	Customized Pkt-1 Received CRC-L Register
	51	33h	Customized Pkt-1 Received CRC-H Register
	52	34h	Customized Pkt-2 Received CRC-L Register
	53	35h	Customized Pkt-2 Received CRC-H Register
	54	36h	Customized Pkt-3 Received CRC-L Register
	55	37h	Customized Pkt-3 Received CRC-H Register
	56-59	38h-3B	RESERVED
	60	3Ch	Self-Test Correct Count LO Register
	61	3Dh	Self-Test Correct Count HI Register
	62	3Eh	Self-Test Error Count LO Register
	63	3Fh	Self-Test Error Count HI Register
	64-75	40h-4Bh	RESERVED
	76	4Ch	RX DLL Control Register
	77	4Dh	TX DLL Control Register
	78-89	4Eh-59h	RESERVED
	90	5Ah	1000M Fast Link Down Enable Register
	91-110	5Bh-6Eh	RESERVED
	111	6Fh	Driving Strength, Fast Link Down, S2P RX PCS Select Setting Register
	112-127	70h-7Fh	RESERVED
	128	80h	General Purpose IO Enable Register (GPIO_EN)
	129	81h	General Purpose IO Direction Register (GPIO_DIR)
	130	82h	General Purpose IO Buffer Type Register (GPIO_BUF)
	131	83h	General Purpose IO Data Select 1 Register (GPIO_DATA_SEL1)
	132	84h	General Purpose IO Data Select 2 Register (GPIO_DATA_SEL2)
	133	85h	General Purpose IO Data Register (GPIO_DATA)
	134	86h	General Purpose IO Interrupt Status Register (GPIO_INT_STS)
	135	87h	General Purpose IO Interrupt Enable Register (GPIO_INT_EN)
	136	88h	General Purpose IO Interrupt Polarity Register (GPIO_INT_POL)
	137-255	89h-FFh	RESERVED

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	256	100h	PTP Command and Control Register (PTP_CMD_CTL)
	257	101h	PTP General Configuration Register (PTP_GENERAL_CONFIG)
	258	102h	PTP Reference Clock Configuration Register (PTP_REF_CLK_CFG)
	259	103h	PTP Interrupt Status Register (PTP_INT_STS)
	260	104h	PTP Interrupt Enable Register (PTP_INT_EN)
	261	105h	PTP Modification Error Register (PTP_MOD_ERR)
	262	106h	PTP LTC Set Seconds High Register (PTP_LTC_SET_SEC_HI)
	263	107h	PTP LTC Set Seconds Mid Register (PTP_LTC_SET_SEC_MID)
	264	108h	PTP LTC Set Seconds Low Register (PTP_LTC_SET_SEC_LO)
	265	109h	PTP LTC Set Nanoseconds High Register (PTP_LTC_SET_NS_HI)
	266	10Ah	PTP LTC Set Nanoseconds Low Register (PTP_LTC_SET_NS_LO)
	267	10Bh	PTP LTC Set Sub-Nanoseconds High Register (PTP_LTC_SET_SUBNS_HI)
	268	10Ch	PTP LTC Set Sub-Nanoseconds Low Register (PTP_LTC_SET_SUBNS_LO)
	269	10Dh	PTP LTC Rate Adjustment High Register (PTP_LTC_RATE_ADJ_HI)
	270	10Eh	PTP LTC Rate Adjustment Low Register (PTP_LTC_RATE_ADJ_LO)
	271	10Fh	PTP LTC Temporary Rate Adjustment High Register (PTP_LTC_TEMP_RATE_-ADJ_HI)
	272	110h	PTP LTC Temporary Rate Adjustment Low Register (PTP_LTC_TEMP_RATE_-ADJ_LO)
	273	111h	PTP LTC Temporary Rate Duration High Register (PTP_LTC_TEMP_RATE_DU-RATION_HI)
	274	112h	PTP LTC Temporary Rate Duration Low Register (PTP_LTC_TEMP_RATE_DU-RATION_LO)
	275	113h	PTP LTC Step Adjustment High Register (PTP_LTC_STEP_ADJ_HI)
	276	114h	PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO)
	277	115h	PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_AD-J_CFG)
	278	116h	PTP LTC Target x Seconds High Register (PTP_LTC_TARGET_SEC_HI_x) x=A
	279	117h	PTP LTC Target x Seconds Low Register (PTP_LTC_TARGET_SEC_LO_x) x=A
	280	118h	PTP LTC Target x Nanoseconds High Register (PTP_LTC_TARGET_NS_HI_x) x=A
	281	119h	PTP LTC Target x Nanoseconds Low Register (PTP_LTC_TARGET_NS_LO_x) x=A
	282	11Ah	PTP LTC Target x Reload / Add Seconds High Register (PTP_LTC_TAR-GET_RELOAD_SEC_HI_x) x=A
	283	11Bh	PTP LTC Target x Reload / Add Seconds Low Register (PTP_LTC_TAR-GET_RELOAD_SEC_LO_x) x=A
	284	11Ch	PTP LTC Target x Reload / Add Nanoseconds High Register (PTP_LTC_TAR-GET_RELOAD_NS_HI_x) x=A
	285	11Dh	PTP LTC Target x Reload / Add Nanoseconds Low Register (PTP_LTC_TAR-GET_RELOAD_NS_LO_x) x=A
	286	11Eh	PTP LTC Target x Actual Nanoseconds High Register (PTP_LTC_TAR-GET_ACT_NS_HI_x) x=A
	287	11Fh	PTP LTC Target x Actual Nanoseconds Low Register (PTP_LTC_TAR-GET_ACT_NS_LO_x) x=A

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	288	120h	PTP LTC Target x Seconds High Register (PTP_LTC_TARGET_SEC_HI_x) x=B
	289	121h	PTP LTC Target x Seconds Low Register (PTP_LTC_TARGET_SEC_LO_x) x=B
	290	122h	PTP LTC Target x Nanoseconds High Register (PTP_LTC_TARGET_NS_HI_x) x=B
	291	123h	PTP LTC Target x Nanoseconds Low Register (PTP_LTC_TARGET_NS_LO_x) x=B
	292	124h	PTP LTC Target x Reload / Add Seconds High Register (PTP_LTC_TARGET_RELOAD_SEC_HI_x) x=B
	293	125h	PTP LTC Target x Reload / Add Seconds Low Register (PTP_LTC_TARGET_RELOAD_SEC_LO_x) x=B
	294	126h	PTP LTC Target x Reload / Add Nanoseconds High Register (PTP_LTC_TARGET_RELOAD_NS_HI_x) x=B
	295	127h	PTP LTC Target x Reload / Add Nanoseconds Low Register (PTP_LTC_TARGET_RELOAD_NS_LO_x) x=B
	296	128h	PTP LTC Target x Actual Nanoseconds High Register (PTP_LTC_TARGET_ACT_NS_HI_x) x=B
	297	129h	PTP LTC Target x Actual Nanoseconds Low Register (PTP_LTC_TARGET_ACT_NS_LO_x) x=B
	298	12Ah	PTP RX User MAC Address High Register (PTP_RX_USER_MAC_HI)
	299	12Bh	PTP RX User MAC Address Mid Register (PTP_RX_USER_MAC_MID)
	300	12Ch	PTP RX User MAC Address Low Register (PTP_RX_USER_MAC_LO)
	301	12Dh	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=0
	302	12Eh	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=1
	303	12Fh	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=2
	304	130h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=3
	305	131h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=4
	306	132h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=5
	307	133h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=6
	308	134h	PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) x=7
	309	135h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=0
	310	136h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=1
	311	137h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=2
	312	138h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=3
	313	139h	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=4
	314	13Ah	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=5
	315	13Bh	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=6
	316	13Ch	PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx) x=7
	317	13Dh	VLAN Ethernet Type ID Register (VLAN_TYPE_ID)
	318	13Eh	VLAN 1 Type / ID Register (VLAN1_TYPE_ID)
	319	13Fh	VLAN 1 ID Mask Register (VLAN1_ID_MASK)
	320	140h	VLAN 1 VID Range Upper Register (VLAN1_VID_RANGE_UP)
	321	141h	VLAN 1 VID Range Lower Register (VLAN1_VID_RANGE_LO)
	322	142h	VLAN 2 Type / ID Register (VLAN2_TYPE_ID)
	323	143h	VLAN 2 ID Mask Register (VLAN2_ID_MASK)
	324	144h	VLAN 2 VID Range Upper Register (VLAN2_VID_RANGE_UP)

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	325	145h	VLAN 2 VID Range Lower Register (VLAN2_VID_RANGE_LO)
	326	146h	LLC Ethernet Type ID Register (LLC_TYPE_ID)
	327	147h	PTP GPIO Select Register (PTP_GPIO_SEL)
	328	148h	PTP RX Latency 10Mbps Register (PTP_RX_LATENCY_10)
	329	149h	PTP TX Latency 10Mbps Register (PTP_TX_LATENCY_10)
	330	14Ah	PTP RX Latency 100Mbps Register (PTP_RX_LATENCY_100)
	331	14Bh	PTP TX Latency 100Mbps Register (PTP_TX_LATENCY_100)
	332	14Ch	PTP RX Latency 1000Mbps Register (PTP_RX_LATENCY_1000)
	333	14Dh	PTP TX Latency 1000Mbps Register (PTP_TX_LATENCY_1000)
	334	14Eh	PTP Asymmetry Delay High Register (PTP_ASYM_DLY_HI)
	335	14Fh	PTP Asymmetry Delay Low Register (PTP_ASYM_DLY_LO)
	336	150h	PTP Peer Delay High Register (PTP_PEERDLY_HI)
	337	151h	PTP Peer Delay Low Register (PTP_PEERDLY_LO)
	338	152h	PTP Capture Information Register (PTP_CAP_INFO)
	339	153h	PTP TX User MAC Address High Register (PTP_TX_USER_MAC_HI)
	340	154h	PTP TX User MAC Address Mid Register (PTP_TX_USER_MAC_MID)
	341	155h	PTP TX User MAC Address Low Register (PTP_TX_USER_MAC_LO)
	342	156h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=0
	343	157h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=1
	344	158h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=2
	345	159h	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=3
	346	15Ah	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=4
	347	15Bh	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=5
	348	15Ch	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=6
	349	15Dh	PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) x=7
	350	15Eh	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=0
	351	15Fh	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=1
	352	160h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=2
	353	161h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=3
	354	162h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=4
	355	163h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=5
	356	164h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=6
	357	165h	PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx) x=7
	358	166h	PTP LTC Read Seconds High Register (PTP_LTC_RD_SEC_HI)
	359	167h	PTP LTC Read Seconds Mid Register (PTP_LTC_RD_SEC_MID)
	360	168h	PTP LTC Read Seconds Low Register (PTP_LTC_RD_SEC_LO)
	361	169h	PTP LTC Read Nanoseconds High Register (PTP_LTC_RD_NS_HI)
	362	16Ah	PTP LTC Read Nanoseconds Low Register (PTP_LTC_RD_NS_LO)
	363	16Bh	PTP LTC Read Sub-Nanoseconds High Register (PTP_LTC_RD_SUBNS_HI)
	364	16Ch	PTP LTC Read Sub-Nanoseconds Low Register (PTP_LTC_RD_SUBNS_LO)
	365	16Dh	PTP Revision Register (PTP_REV)

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	366	16Eh	PTP Spare Register (PTP_SPARE)
	367	16Fh	RESERVED
	368	170h	PTP RX Parsing Configuration Register (PTP_RX_PARSE_CONFIG)
	369	171h	PTP RX Parsing VLAN Configuration Register (PTP_RX_PARSE_VLAN_CONFIG)
	370	172h	PTP RX Parsing Layer2 Format Address Enable Register (PTP_RX_PARSE_L2_ADDR_EN)
	371	173h	PTP RX Parsing IP Format Address Enable Register (PTP_RX_PARSE_IP_ADDR_EN)
	372	174h	PTP RX Parsing UDP Source Port Register (PTP_RX_PARSE_UDP_SRC_PORT)
	373	175h	PTP RX Parsing UDP Destination Port Register (PTP_RX_PARSE_UDP_DEST_PORT)
	374	176h	PTP RX Version Register (PTP_RX_VERSION)
	375	177h	PTP RX Domain / Domain Range Lower Register (PTP_RX_DOMAIN_DOMAIN_LO)
	376	178h	PTP RX Domain Mask / Domain Range Upper Register (PTP_RX_DOMAIN_MASK_DOMAIN_UP)
	377	179h	PTP RX SdoId / SdoId Range Lower Register (PTP_RX_SDOID_SDOID_LO)
	378	17Ah	PTP RX SdoId Mask / SdoId Range Upper Register (PTP_RX_SDOID_MASK_SDOID_UP)
	379	17Bh	PTP RX Timestamp Enable Register (PTP_RX_TIMESTAMP_EN)
	380	17Ch	PTP RX Timestamp Configuration Register (PTP_RX_TIMESTAMP_CONFIG)
	381	17Dh	PTP RX Modification Register (PTP_RX_MOD)
	382	17Eh	PTP RX Reserved Bytes Configuration Register (PTP_RX_RSVD_BYTE_CFG)
	383	17Fh	PTP RX Tail Tag Register (PTP_RX_TAIL_TAG)
	384	180h	PTP RX Correction Field Modification Enable Register (PTP_RX_CF_MOD_EN)
	385	181h	PTP RX Correction Field Configuration Register (PTP_RX_CF_CFG)
	386	182h	PTP RX Ingress Time Nanoseconds High Register (PTP_RX_INGRESS_NS_HI)
	387	183h	PTP RX Ingress Time Nanoseconds Low Register (PTP_RX_INGRESS_NS_LO)
	388	184h	PTP RX Ingress Time Seconds High Register (PTP_RX_INGRESS_SEC_HI)
	389	185h	PTP RX Ingress Time Seconds Low Register (PTP_RX_INGRESS_SEC_LO)
	390	186h	PTP RX Message Header 1 Register (PTP_RX_MSG_HEADER1)
	391	187h	PTP RX Message Header 2 Register (PTP_RX_MSG_HEADER2)
	392	188h	PTP RX Pdelay_Req Ingress Time Seconds High Register (PTP_RX_PDREQ_SEC_HI)
	393	189h	PTP RX Pdelay_Req Ingress Time Seconds Mid Register (PTP_RX_PDREQ_SEC_MID)
	394	18Ah	PTP RX Pdelay_Req Ingress Time Seconds low Register (PTP_RX_PDREQ_SEC_LOW)
	395	18Bh	PTP RX Pdelay_Req Ingress Time Nanoseconds High Register (PTP_RX_PDREQ_NS_HI)
	396	18Ch	PTP RX Pdelay_Req Ingress Time Nanoseconds Low Register (PTP_RX_PDREQ_NS_LO)

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	397	18Dh	PTP RX Raw Ingress Time Seconds Register (PTP_RX_RAW_TS_SEC)
	398	18Eh	PTP RX Raw Ingress Time Nanoseconds High Register (PTP_RX-_RAW_TS_NS_HI)
	399	18Fh	PTP RX Raw Ingress Time Nanoseconds Low Register (PTP_RX-_RAW_TS_NS_LO)
	400	190h	PTP RX Checksum Dropped Count High Register (PTP_RX_CHKSUM_-DROPPED_CNT_HI)
	401	191h	PTP RX Checksum Dropped Count Low Register (PTP_RX_CHKSUM_-DROPPED_CNT_LO)
	402	192h	PTP RX Frames Modified Count High Register (PTP_RX_FRMS_-MOD_CNT_HI)
	403	193h	PTP RX Frames Modified Count Low Register (PTP_RX_FRMS_-MOD_CNT_LO)
	404-431	194h-1AFh	RESERVED
	432	1B0h	PTP TX Parsing Configuration Register (PTP_TX_PARSE_CONFIG)
	433	1B1h	PTP TX Parsing VLAN Configuration Register (PTP_TX_PARSE_VLAN_CON-FIG)
	434	1B2h	PTP TX Parsing Layer2 Format Address Enable Register (PTP_TX-_PARSE_L2_ADDR_EN)
	435	1B3h	PTP TX Parsing IP Format Address Enable Register (PTP_TX_PARSE_IP_AD-DR_EN)
	436	1B4h	PTP TX Parsing UDP Source Port Register (PTP_TX_PARSE_UDP_S-RC_PORT)
	437	1B5h	PTP TX Parsing UDP Destination Port Register (PTP_TX_PARSE_UD-P_DEST_PORT)
	438	1B6h	PTP TX Version Register (PTP_TX_VERSION)
	439	1B7h	PTP TX Domain / Domain Range Lower Register (PTP_TX_DOMAIN_DO-MAIN_LO)
	440	1B8h	PTP TX Domain Mask / Domain Range Upper Register (PTP_TX_DO-MAIN_MASK_DOMAIN_UP)
	441	1B9h	PTP TX Sdold / Sdold Range Lower Register (PTP_TX_SDOID_SDOID_LO)
	442	1BAh	PTP TX Sdold Mask / Sdold Range Upper Register (PTP_TX_SDOID_MASK_S-DOID_UP)
	443	1BBh	PTP TX Timestamp Enable Register (PTP_TX_TIMESTAMP_EN)
	444	1BCh	PTP TX Timestamp Configuration Register (PTP_TX_TIMESTAMP_CONFIG)
	445	1BDh	PTP TX Modification Register (PTP_TX_MOD)
	446	1BEh	PTP TX Reserved Bytes Configuration Register (PTP_TX_RSVD_BYTE_CFG)
	447	1BFh	PTP TX Tail Tag Register (PTP_TX_TAIL_TAG)
	448	1C0h	PTP TX Correction Field Modification Enable Register (PTP_TX_CF_MOD_EN)
	449	1C1h	PTP TX Correction Field Configuration Register (PTP_TX_CF_CFG)
	450	1C2h	PTP TX Egress Time Nanoseconds High Register (PTP_TX_EGRESS_NS_HI)
	451	1C3h	PTP TX Egress Time Nanoseconds Low Register (PTP_TX_EGRESS_NS_LO)
	452	1C4h	PTP TX Egress Time Seconds High Register (PTP_TX_EGRESS_SEC_HI)
	453	1C5h	PTP TX Egress Time Seconds Low Register (PTP_TX_EGRESS_SEC_LO)

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	454	1C6h	PTP TX Message Header 1 Register (PTP_TX_MSG_HEADER1)
	455	1C7h	PTP TX Message Header 2 Register (PTP_TX_MSG_HEADER2)
	456	1C8h	PTP TX Sync Egress Time Seconds High Register (PTP_TX_SYNC_SEC_HI)
	457	1C9h	PTP TX Sync Egress Time Seconds Mid Register (PTP_TX_SYNC_SEC_MID)
	458	1CAh	PTP TX Sync Egress Time Seconds Low Register (PTP_TX_SYNC_SEC_LOW)
	459	1CBh	PTP TX Sync Egress Time Nanoseconds High Register (PTP_TX_SYNC_NS_HI)
	460	1CCh	PTP TX Sync Egress Time Nanoseconds Low Register (PTP_TX_SYNC_NS_LO)
	461	1CDh	PTP TX Pdelay_Resp Egress Time Seconds High Register (PTP_TX_PDRESP_SEC_HI)
	462	1CEh	PTP TX Pdelay_Resp Egress Time Seconds Mid Register (PTP_TX_PDRESP_SEC_MID)
	463	1CFh	PTP TX Pdelay_Resp Egress Time Seconds low Register (PTP_TX_PDRESP_SEC_LOW)
	464	1D0h	PTP TX Pdelay_Resp Egress Time Nanoseconds High Register (PTP_TX_PDRESP_NS_HI)
	465	1D1h	PTP TX Pdelay_Resp Egress Time Nanoseconds Low Register (PTP_TX_PDRESP_NS_LO)
	466	1D2h	PTP TX Raw Egress Time Seconds Register (PTP_TX_RAW_TS_SEC)
	467	1D3h	PTP TX Raw Egress Time Nanoseconds High Register (PTP_TX_RAW_TS_NS_HI)
	468	1D4h	PTP TX Raw Egress Time Nanoseconds Low Register (PTP_TX_RAW_TS_NS_LO)
	469	1D5h	PTP TX Checksum Dropped Count High Register (PTP_TX_CHKSUM_DROPPED_CNT_HI)
	470	1D6h	PTP TX Checksum Dropped Count Low Register (PTP_TX_CHKSUM_DROPPED_CNT_LO)
	471	1D7h	PTP TX Frames Modified Count High Register (PTP_TX_FRMS_MOD_CNT_HI)
	472	1D8h	PTP TX Frames Modified Count Low Register (PTP_TX_FRMS_MOD_CNT_LO)
	473-495	1D9h-1EFh	RESERVED
	496	1F0h	PTP GPIO Capture Enable Register (PTP_GPIO_CAP_EN)
	497	1F1h	PTP GPIO Capture Lock Register (PTP_GPIO_CAP_LOCK)
	498	1F2h	PTP GPIO x Rising Edge LTC Seconds High Capture Register (PTP_GPIO_RE_LTC_SEC_HI_CAP_x)
	499	1F3h	PTP GPIO x Rising Edge LTC Seconds Low Capture Register (PTP_GPIO_RE_LTC_SEC_LO_CAP_x)
	500	1F4h	PTP GPIO x Rising Edge LTC Nanoseconds High Capture Register (PTP_GPIO_RE_LTC_NS_HI_CAP_x)
	501	1F5h	PTP GPIO x Rising Edge LTC Nanoseconds Low Capture Register (PTP_GPIO_RE_LTC_NS_LO_CAP_x)

TABLE 3: MMD CONTROL AND STATUS REGISTERS MAP (CONTINUED)

MMD Device Address (in decimal)	Index (in decimal)	Index (in hex)	Register Name
2 (cont.)	502	1F6h	PTP GPIO x Falling Edge LTC Seconds High Capture Register (PTP_GPIO_FE_LTC_SEC_HI_CAP_x)
	503	1F7h	PTP GPIO x Falling Edge LTC Seconds Low Capture Register (PTP_GPIO_FE_LTC_SEC_LO_CAP_x)
	504	1F8h	PTP GPIO x Falling Edge LTC Nanoseconds High Capture Register (PTP_GPIO_FE_LTC_NS_HI_CAP_x)
	505	1F9h	PTP GPIO x Falling Edge LTC Nanoseconds Low Capture Register (PTP_GPIO_FE_LTC_NS_LO_CAP_x)
	506	1FAh	PTP GPIO Capture Status Register (PTP_GPIO_CAP_STS)
	507	1FBh	PTP GPIO Interrupt Clear Configuration Register (PTP_GPIO_INT_CLR_CFG)
	508-509	1FCh-1FDh	RESERVED
	510	1FEh	PTP Debug BUS Signal Group Select (PTP_DEBUG_SEL)
3	0	0h	PCS Control 1 Register
	1	1h	PCS Status 1 Register
	2-7	2h-7h	RESERVED
	8	8h	EEE Quiet Timer Register
	9	9h	EEE Update Timer Register
	10	Ah	EEE Link-Fail Timer Register
	11	Bh	EEE Post-Update Timer Register
	12	Ch	EEE WaitWQ Timer Register
	13	Dh	EEE Wake Timer Register
	14	Eh	EEE WakeTX Timer Register
	15	Fh	EEE WakeMz Timer Register
	16-19	10h-13h	RESERVED
	20	14h	EEE Control and Capability Register
	21	15h	RESERVED
	22	16h	EEE Wake Error Counter Register
	23	17h	RESERVED
	24	18h	EEE 100 Timer-0 Register
	25	19h	EEE 100 Timer-1 Register
	26	1Ah	EEE 100 Timer-2 Register
	27	1Bh	EEE 100 Timer-3 Register
7	60	3Ch	EEE Advertisement Register
	61	3Dh	EEE Link Partner Ability Register
	62	3Eh	EEE Link Partner Ability Override Register
	63	3Fh	EEE Message Code Register
28 (1Ch)	1	1h	XTAL Control Register
	2-8	2h-8h	RESERVED
	9	9h	AFED Control Register
	10-13	Ah-Dh	RESERVED
	14	Eh	LDO Control Register
	15-35	Fh-23h	RESERVED
	36	24h	EDPD Control Register
	37	25h	EMITX Control Register
	38-52	26h-34h	EMITX Coefficient Registers

5.0 REGISTER DEFINITIONS

Register Definitions are divided into the following sections:

- Section 5.1, "Standard Registers"
- Section 5.2, "MDIO Manageable Device (MMD) Registers"

5.1 Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0 to 15 (Fh)) are defined according to the IEEE specification, while the remaining 16 registers (Registers 16 (10h) to 31 (1Fh)) are defined specific to the PHY vendor.

5.1.1 BASIC CONTROL REGISTER

Index (In Decimal): 0 Size: 16 bits

This read/write register is used to configure the PHY.

Bits	Description	Type	Default
15	**PHY Soft Reset (RESET)** When set, this bit resets all the PHY and all its registers to their default state. This bit is self clearing. 1 = PHY software reset.	R/W1S/ SC	0b
14	**Loopback (PHY_LOOPBACK)** This bit enables/disables the loopback mode. When enabled, transmissions are not sent to network. Instead, they are looped back into the PHY. 0 = Loopback mode disabled (normal operation) 1 = Loopback mode enabled	R/W	0b
13	**Speed Select[0]** Together with Speed Select[1], sets speed per the following table: [Speed Select1][Speed Select0] 00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	0b
12	**Auto-Negotiation Enable** This bit enables/disables Auto-Negotiation. 0 = disable auto-negotiate process 1 = enable auto-negotiate process (overrides the Speed Select[0], Speed Select[1] and Duplex Mode bits of this register)	R/W	1b
11	**Power Down** This bit controls the power down mode of the PHY. 0 = Normal operation 1 = General power down mode	R/W	0b

Bits	Description	Type	Default
10	**Isolate (PHY_ISO)** This bit controls the isolation of the PHY from the MII interface. 0 = Non-Isolated (Normal operation) 1 = Isolated	R/W	0b
9	**Restart Auto-Negotiation (PHY_RST_AN)** When set, this bit restarts the Auto-Negotiation process. This bit is self clearing. 1 = Auto-Negotiation restarted	R/W1S/ SC	0b
8	**Duplex Mode** This bit is used to set the duplex. 0 = Half Duplex 1 = Full Duplex **Note:** Ignored if the Auto-Negotiation Enable bit of this register is 1.	R/W	1b
7	**Collision Test Mode (PHY_COL_TEST)** This bit enables/disables the collision test mode of the PHY. When set, the collision signal is active during transmission. It is recommended that this feature be used only in loopback mode. 0 = Collision test mode disabled 1 = Collision test mode enabled	R/W	0b
6	**Speed Select[1]** See description for Speed Select[0] for details.	R/W	1b
5:0	**RESERVED**	R/W	—

5.1.2 BASIC STATUS REGISTER

Index (In Decimal): 1 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**100BASE-T4** This bit displays the status of 100BASE-T4 compatibility. 0 = PHY not able to perform 100BASE-T4 1 = PHY able to perform 100BASE-T4	RO	0b
14	**100BASE-X Full Duplex** This bit displays the status of 100BASE-X full duplex compatibility. 0 = PHY not able to perform 100BASE-X full duplex 1 = PHY able to perform 100BASE-X full duplex	RO	1b
13	**100BASE-X Half Duplex** This bit displays the status of 100BASE-X half duplex compatibility. 0 = PHY not able to perform 100BASE-X half duplex 1 = PHY able to perform 100BASE-X half duplex	RO	1b
12	**10BASE-T Full Duplex** This bit displays the status of 10BASE-T full duplex compatibility. 0 = PHY not able to perform 10BASE-T full duplex 1 = PHY able to perform 10BASE-T full duplex	RO	1b
11	**10BASE-T Half Duplex** This bit displays the status of 10BASE-T half duplex compatibility. 0 = PHY not able to perform 10BASE-T half duplex 1 = PHY able to perform 10BASE-T half duplex	RO	1b
10	**100BASE-T2 Full Duplex** This bit displays the status of 100BASE-T2 full duplex compatibility. 0 = PHY not able to perform 100BASE-T2 full duplex 1 = PHY able to perform 100BASE-T2 full duplex	RO	0b
9	**100BASE-T2 Half Duplex** This bit displays the status of 100BASE-T2 half duplex compatibility. 0 = PHY not able to perform 100BASE-T2 half duplex 1 = PHY able to perform 100BASE-T2 half duplex	RO	0b
8	**Extended Status** This bit displays whether extended status information is in register 15 (per IEEE 802.3 clause 22.2.4). 0 = No extended status information in Register 15 1 = Extended status information in Register 15	RO	1b

Bits	Description	Type	Default
7	**Unidirectional Ability** This bit indicates whether the PHY is able to transmit regardless of whether the PHY has determined that a valid link has been established. 0 = Can only transmit when a valid link has been established 1 = Can transmit regardless	RO	0b
6	**MF Preamble Suppression** This bit indicates whether the PHY accepts management frames with the preamble suppressed. 0 = Management frames with preamble suppressed not accepted 1 = Management frames with preamble suppressed accepted	RO	1b
5	**Auto-Negotiation Complete** This bit indicates the status of the Auto-Negotiation process. 0 = Auto-Negotiation process not completed 1 = Auto-Negotiation process completed	RO	0b
4	**Remote Fault** This bit indicates if a remote fault condition has been detected. 0 = No remote fault condition detected 1 = Remote fault condition detected	RO/LH	0b
3	**Auto-Negotiation Ability** This bit indicates the PHY's Auto-Negotiation ability. 0 = PHY is unable to perform Auto-Negotiation 1 = PHY is able to perform Auto-Negotiation	RO	1b
2	**Link Status** This bit indicates the status of the link. 0 = Link is down 1 = Link is up	RO/LL	0b
1	**Jabber Detect** This bit indicates the status of the jabber condition. 0 = No jabber condition detected 1 = Jabber condition detected	RO/LH	0b
0	**Extended Capability** This bit indicates whether extended register capability is supported. 0 = Basic register set capabilities only 1 = Extended register set capabilities	RO	1b

5.1.3 DEVICE IDENTIFIER 1 REGISTER

Index (In Decimal): 2 Size: 16 bits

This register contains the MSB of the Organizationally Unique Identifier (OUI) for the PHY. The LSB of the PHY OUI is contained in the Device Identifier 2 Register.

Bits	Description	Type	Default
15:0	**PHY ID Number** Assigned to the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0022h

5.1.4 DEVICE IDENTIFIER 2 REGISTER

Index (In Decimal): 3 Size: 16 bits

This register contains the LSB of the Organizationally Unique Identifier (OUI) for the PHY. The MSB of the PHY OUI is contained in the Device Identifier 1 Register.

Bits	Description	Type	Default
15:10	**PHY ID Number** Assigned to the 19th through 24th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	000101b
9:4	**Model Number** Six-bit manufacturer's model number.	RO	100101b
3:0	**Revision Number** Four-bit manufacturer's revision number.	RO	Note 5-1

Note 5-1 The default value of the Revision Number field varies dependent on the silicon revision number.

Note:	The hexadecimal equivalent of this register is 165xh.

5.1.5 AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Index (In Decimal): 4 Size: 16 bits

This read/write register contains the advertised ability of the PHY and is used in the Auto-Negotiation process with the link partner.

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	—
13	**Remote Fault** This bit determines if remote fault indication will be advertised to the link partner. 0 = Remote fault indication not advertised 1 = Remote fault indication advertised	R/W	0b
12	**Extended Next Page** **Note:** This bit should be written as 0.	RO	0b
11	**Asymmetric Pause** This bit determines the advertised asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner advertised 1 = Asymmetric PAUSE toward link partner advertised	R/W	1b
10	**Symmetric Pause** This bit determines the advertised symmetric pause capability. 0 = No Symmetric PAUSE toward link partner advertised 1 = Symmetric PAUSE toward link partner advertised	R/W	1b
9	**100BASE-T4** 0 = no T4 ability 1 = T4 able **Note:** The device does not support this mode and this bit should always be written as a 0.	RO	0
8	**100BASE-X Full Duplex** This bit determines the advertised 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not advertised 1 = 100BASE-X full duplex ability advertised	R/W	Note 5-2
7	**100BASE-X Half Duplex** This bit determines the advertised 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not advertised 1 = 100BASE-X half duplex ability advertised	R/W	Note 5-2

Bits	Description	Type	Default
6	**10BASE-T Full Duplex** This bit determines the advertised 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not advertised 1 = 10BASE-T full duplex ability advertised	R/W	Note 5-2
5	**10BASE-T Half Duplex** This bit determines the advertised 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not advertised 1 = 10BASE-T half duplex ability advertised	R/W	Note 5-2
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	R/W	00001b

Note 5-2 Set by the MODE[3:0] strapping pins.

5.1.6 AUTO-NEGOTIATION LINK PARTNER BASE PAGE ABILITY REGISTER

Index (In Decimal): 5 Size: 16 bits

This read-only register contains the advertised ability of the link partner's PHY and is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15	**Next Page** This bit indicates the link partner PHY page capability. 0 = Link partner PHY does not advertise next page capability 1 = Link partner PHY advertises next page capability	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0b
13	**Remote Fault** This bit indicates whether a remote fault has been detected. 0 = No remote fault 1 = Remote fault detected	RO	0b
12	**Extended Next Page** 0 = Link partner PHY does not advertise extended next page capability 1 = Link partner PHY advertises extended next page capability	RO	0b
11	**Asymmetric Pause** This bit indicates the link partner PHY asymmetric pause capability. 0 = No Asymmetric PAUSE toward link partner 1 = Asymmetric PAUSE toward link partner	RO	0b

Bits	Description	Type	Default
10	**Pause** This bit indicates the link partner PHY symmetric pause capability. 0 = No Symmetric PAUSE toward link partner 1 = Symmetric PAUSE toward link partner	RO	0b
9	**100BASE-T4** This bit indicates the link partner PHY 100BASE-T4 capability. 0 = 100BASE-T4 ability not supported 1 = 100BASE-T4 ability supported	RO	0b
8	**100BASE-X Full Duplex** This bit indicates the link partner PHY 100BASE-X full duplex capability. 0 = 100BASE-X full duplex ability not supported 1 = 100BASE-X full duplex ability supported	RO	0b
7	**100BASE-X Half Duplex** This bit indicates the link partner PHY 100BASE-X half duplex capability. 0 = 100BASE-X half duplex ability not supported 1 = 100BASE-X half duplex ability supported	RO	0b
6	**10BASE-T Full Duplex** This bit indicates the link partner PHY 10BASE-T full duplex capability. 0 = 10BASE-T full duplex ability not supported 1 = 10BASE-T full duplex ability supported	RO	0b
5	**10BASE-T Half Duplex** This bit indicates the link partner PHY 10BASE-T half duplex capability. 0 = 10BASE-T half duplex ability not supported 1 = 10BASE-T half duplex ability supported	RO	0b
4:0	**Selector Field** This field identifies the type of message being sent by Auto-Negotiation. 00001 = IEEE 802.3	RO	00000b

5.1.7 AUTO-NEGOTIATION EXPANSION REGISTER

Index (In Decimal): 6 Size: 16 bits

This read/write register is used in the Auto-Negotiation process between the link partner and the PHY.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**Receive Next Page Location Able** 0 = Received next page storage location is not specified by bit 6.5 1 = Received next page storage location is specified by bit 6.5	RO	1b
5	**Received Next Page Storage Location** 0 = Link partner next pages are stored in the Auto-Negotiation Link Partner Base Page Ability Register (PHY register 5) 1 = Link partner next pages are stored in the Auto-Negotiation Next Page RX Register (PHY register 8)	RO	1b
4	**Parallel Detection Fault** This bit indicates whether a Parallel Detection Fault has been detected. 0 = A fault hasn't been detected via the Parallel Detection function 1 = A fault has been detected via the Parallel Detection function	RO/LH	0b
3	**Link Partner Next Page Able** This bit indicates whether the link partner has next page ability. 0 = Link partner does not contain next page capability 1 = Link partner contains next page capability	RO	0b
2	**Next Page Able** This bit indicates whether the local device has next page ability. 0 = Local device does not contain next page capability 1 = Local device contains next page capability	RO	1b
1	**Page Received** This bit indicates the reception of a new page. 0 = A new page has not been received 1 = A new page has been received	RO/LH	0b
0	**Link Partner Auto-Negotiation Able** This bit indicates the Auto-Negotiation ability of the link partner. 0 = Link partner is not Auto-Negotiation able 1 = Link partner is Auto-Negotiation able	RO	0b

5.1.8 AUTO-NEGOTIATION NEXT PAGE TX REGISTER

Index (In Decimal): 7 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	R/W	0b
14	**RESERVED**	RO	—
13	**Message Page** 0 = Unformatted page 1 = Message page	R/W	1b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	R/W	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	R/W	000 0000 0001b

5.1.9 AUTO-NEGOTIATION NEXT PAGE RX REGISTER

Index (In Decimal): 8 Size: 16 bits

Bits	Description	Type	Default
15	**Next Page** 0 = No next page ability 1 = Next page capable	RO	0b
14	**Acknowledge** This bit indicates whether the link code word has been received from the partner. 0 = Link code word not yet received from partner 1 = Link code word received from partner	RO	0
13	**Message Page** 0 = Unformatted page 1 = Message page	RO	0b
12	**Acknowledge 2** 0 = Device cannot comply with message. 1 = Device will comply with message.	RO	0b
11	**Toggle** 0 = Previous value was HIGH. 1 = Previous value was LOW.	RO	0b
10:0	**Message Code** Message/Unformatted Code Field	RO	000 0000 0000b

5.1.10 AUTO-NEGOTIATION MASTER SLAVE CONTROL REGISTER

Index (In Decimal): 9 Size: 16 bits

Bits	Description	Type	Default
15:13	**Test Mode** IEEE 802.3 clause 40.6.1.1.2 transmitter test mode. 000 = Normal mode 001 = Test Mode 1 - Transmit waveform test 010 = Test Mode 2 - Transmit jitter test in Master mode 011 = Test Mode 3 - Transmit jitter test in Slave mode 100 = Test Mode 4 - Transmitter distortion test 101 = Reserved 110 = Reserved 111 = Reserved	R/W	000b
12	**Master/Slave Manual Configuration Enable** 0 = disable MASTER-SLAVE manual configuration value 1 = enable MASTER-SLAVE manual configuration value	R/W	0b
11	**Master/Slave Manual Configuration Value** Active only when the Master/Slave Manual Configuration Enable bit of this register is 1. 0 = Configure PHY as slave 1 = Configure PHY as master	R/W	0b
10	**Port Type** 0 = single-port device 1 = multi-port device	R/W	0b
9	**1000BASE-T Full Duplex** 0 = advertise PHY is not 1000BASE-T full duplex capable 1 = advertise PHY is 1000BASE-T full duplex capable	R/W	1b
8	**1000BASE-T Half Duplex** 0 = advertise PHY is not 1000BASE-T half duplex capable 1 = advertise PHY is 1000BASE-T half duplex capable **Note:** The device does not support this mode and this bit should always be written as a 0.	R/W	0b
7:0	**RESERVED**	RO	—

5.1.11 AUTO-NEGOTIATION MASTER SLAVE STATUS REGISTER

Index (In Decimal): 10 Size: 16 bits

Bits	Description	Type	Default
15	**Master/Slave Configuration Fault** 0 = No MASTER-SLAVE configuration fault detected 1 = MASTER-SLAVE configuration fault detected	RO/LH	0b
14	**Master/Slave Configuration Resolution** 0 = Local PHY configuration resolved to SLAVE 1 = Local PHY configuration resolved to MASTER	RO	0b
13	**Local 1000BASE-T Receiver Status** 0 = Local Receiver not OK 1 = Local Receiver OK	RO	0b
12	**Remote (Link Partner) Receiver Status** 0 = Remote Receiver not OK 1 = Remote Receiver OK	RO	0b
11	**Link Partner Advertised 1000BASE-T Full Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T full duplex 1 = Link Partner is capable of 1000BASE-T full duplex	RO	0b
10	**Link Partner Advertised 1000BASE-T Half Duplex Capability** 0 = Link Partner is not capable of 1000BASE-T half duplex 1 = Link Partner is capable of 1000BASE-T half duplex	RO	0b
9:8	**RESERVED**	RO	—
7:0	**1000BASE-T Idle Error Count** Cumulative count of the errors detected when the receiver is receiving idles. **Note:** This counter halts at a value of 0xFF.	RO/RC	00h

5.1.12 MMD ACCESS CONTROL REGISTER

Index (In Decimal): 13 Size: 16 bits

Bits	Description	Type	Default
15:14	**MMD Function** This field is used to select the desired MMD function: 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only	R/W	00b
13:5	**RESERVED**	RO	—
4:0	**MMD Device Address (DEVAD)** This field is used to select the desired MMD device address.	R/W	00000b

5.1.13 MMD ACCESS ADDRESS/DATA REGISTER

Index (In Decimal): 14 Size: 16 bits

Bits	Description	Type	Default
15:0	**MMD Register Address/Data** If the MMD Function field of the MMD Access Control Register is “00”, this field is used to indicate the MMD register address to read/write of the device specified in the MMD Device Address (DEVAD) field. Otherwise, this register is used to read/write data from/to the previously specified MMD address.	R/W	0000h

5.1.14 EXTENDED STATUS REGISTER

Index (In Decimal): 15 Size: 16 bits

This register is used to monitor the status of the PHY.

Bits	Description	Type	Default
15	**1000BASE-X Full Duplex** This bit displays the status of 1000BASE-X full duplex compatibility. 0 = PHY not able to perform 1000BASE-X full duplex 1 = PHY able to perform 1000BASE-X full duplex	RO	0b
14	**1000BASE-X Half Duplex** This bit displays the status of 1000BASE-X half duplex compatibility. 0 = PHY not able to perform 1000BASE-X half duplex 1 = PHY able to perform 1000BASE-X half duplex	RO	0b
13	**1000BASE-T Full Duplex** This bit displays the status of 1000BASE-T full duplex compatibility. 0 = PHY not able to perform 1000BASE-T full duplex 1 = PHY able to perform 1000BASE-T full duplex	RO	1b
12	**1000BASE-T Half Duplex** This bit displays the status of 1000BASE-T half duplex compatibility. 0 = PHY not able to perform 1000BASE-T half duplex 1 = PHY able to perform 1000BASE-T half duplex	RO	0b
11:0	**RESERVED**	RO	—

5.1.15 PCS LOOPBACK SWAP/POLARITY CONTROL REGISTER

Index (In Decimal): 17 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**Remote Loopback** 1 = Enable remote loopback 0 = Disable remote loopback	R/W	0b
7:6	**mr_led_sel** See Table 5-12 in the *LAN8840 Data Sheet*.	R/W	11b
5:3	**RESERVED**	RO	—
2	**10BASE-T Preamble Enable** 1 = Enable 10BASE-T Preamble for Loopback 0 = Disable 10BASE-T Preamble for Loopback	R/W	0b

Bits	Description	Type	Default
1:0	**RESERVED**	RO	—

5.1.16 LINKMD CABLE DIAGNOSTIC REGISTER

Index (In Decimal): 18 Size: 16 bits

Bits	Description	Type	Default
15	**Cable Diagnostics Test Enable (VCT_EN)** Writing a 1 enables the test. This bit is self-cleared when the test is complete. Writing a 0 will disable the test. Reading a 0 indicates the cable diagnostic test is completed and the status information is valid. Reading a 1 indicates the cable diagnostic test is in progress and the status information is NOT valid.	R/W/SC	0b
14	**Cable Diagnostic Disable Transmitter (VCT_DIS_TX)** [0] = The transmitter is enabled to start cable diagnostic. [1] = The transmitter is disabled and cable diagnostic is on hold to break down the link.	R/W	0b
13:12	**Cable Diagnostics Test Pair (VCT_PAIR[1:0])** This field defines which channel to be tested. 00 = Pair A 01 = Pair B 10 = Pair C 11 = Pair D	R/W	00b
11:10	**RESERVED**	R/W	00b
9:8	**Cable Diagnostics Status (VCT_ST[1:0])** Valid only when VCT_EN = 0. 00 = Normal, no fault has been detected 01 = Open Fault has been detected 10 = Short Fault has been detected 11 = Cable diagnostic test failed	RO	00b

Bits	Description	Type	Default
7:0	**Cable Diagnostics Data or Threshold (VCT_DATA[7:0])** This is the data of cable diagnostics. Valid only when VCT_EN = 0. (1) If cable is normal, i.e., VCT_ST = 00, VCT_DATA don't care. (2) If cable is open or short, i.e., VCT_ST = 01 or 10, the distance to fault is approximately 0.8 * (VCT_DATA - 22) (Meters) (3) If cable diagnostics failed, i.e., VCT_ST = 11, Bit[7] = 1 means invalid reflected pulse width, i.e. equal or greater than 152ns, equal or less than 48ns. Bit[6] = 1 means cable has signal for too long time during WAIT state. It's unusual and for debug only. Bit[5] = 1 means mask100 detected and no silent time window can be found for diagnostics. It means high frequency signal is found on the line. The link partner probably is in forced 100BT or 1000BT mode. Bit[4] = 1 means signals faster than NLP and FLP exists and no silent time window can be found for diagnostics. It's unusual and for debug only. Bit[3:2] = number of low pulses detected. If more than 3, stay at 3. Bit[1:0] = number of high pulses detected. If more than 3, stay at 3.	RO	00h

5.1.17 DIGITAL PMA/PCS STATUS REGISTER

Index (In Decimal): 19 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	**1000BT link status** 1000 BT link status 1 = link status OK 0 = link status not OK	RO	0b
0	**100BT link status** 100 BT link status 1 = link status OK 0 = link status not OK	RO	0b

5.1.18 RXER COUNTER REGISTER

Index (In Decimal): 21 Size: 16 bits

Bits	Description	Type	Default
15:0	**RXER Counter** RX Error counter for the RX_ER signal **Note:** This counter halts at a value of 0xFFFF.	RC	0000h

5.1.19 LED MODE SELECT REGISTER

Index (In Decimal): 22 Size: 16 bits

This register selects the operating mode of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is clear.

Bits	Description	Type	Default
15:12	**LED4 Configuration** This field configures the LED4 pin function. Refer to Table 4 for definitions.	R/W	1000b
11:8	**LED3 Configuration** This field configures the LED3 pin function. Refer to Table 4 for definitions.	R/W	0000b
7:4	**LED2 Configuration** This field configures the LED2 pin function. Refer to Table 4 for definitions.	R/W	0010b
3:0	**LED1 Configuration** This field configures the LED1 pin function. Refer to Table 4 for definitions.	R/W	0001b

TABLE 4: LED MODE AND FUNCTION SUMMARY

Mode	Name	Description
0	Link/Activity	1 (led off) = No link in any speed on any media interface. 0 (led on) = Valid link at any speed on any media interface. Blink or pulse stretch (led turns off) = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 (led off) = No link at 1000BASE-T. 0 (led on) = Valid link at 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 1000BASE-T with activity present.
2	Link100/Activity	1 (led off) = No link at 100BASE-TX. 0 (led on) = Valid link at 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX with activity present.
3	Link10/Activity	1 (led off) = No link at 10BASE-T. 0 (led on) = Valid link at 10BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T with activity present.
4	Link100/1000/Activity	1 (led off) = No link at 100BASE-TX or 1000BASE-T. 0 (led on) = Valid link at 100BASE-TX or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 100BASE-TX or 1000BASE-T, with activity present.
5	Link10/1000/Activity	1 (led off) = No link at 10BASE-T or 1000BASE-T. 0 (led on) = Valid link at 10BASE-T or 1000BASE-T. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 1000BASE-T, with activity present.

TABLE 4: LED MODE AND FUNCTION SUMMARY (CONTINUED)

Mode	Name	Description
6	Link10/100/Activity	1 (led off) = No link at 10BASE-T or 100BASE-TX. 0 (led on) = Valid link at 10BASE-T or 100BASE-TX. Blink or pulse stretch (led turns off) = Valid link at 10BASE-T or 100BASE-TX, with activity present.
7	RESERVED	RESERVED
8	Duplex/Collision	1 (led off) = Link established in half-duplex mode, or no link established. 0 (led on) = Link established in full-duplex mode. Blink or pulse stretch (led turns on) = Link established in half-duplex mode but collisions are present.
9	Collision	1 (led off) = No collisions detected. Blink or pulse stretch (led turns on) = Collision detected.
10	Activity	1 (led off) = No activity present. Blink or pulse stretch (led turns on) = Activity present. (becomes TX activity present if the LED Activity Output Select bit in the LED Behavior Register is set to 1.)
11	RESERVED	RESERVED
12	Auto-Negotiation Fault	1 (led off) = No Auto-Negotiation fault present. 0 (led on) = Auto-Negotiation fault occurred.
13	RESERVED	RESERVED
14	Force LED Off	1 (led off) = De-asserts the LED.
15	Force LED On	0 (led on) = Asserts the LED.

5.1.20 LED BEHAVIOR REGISTER

Index (In Decimal): 23 Size: 16 bits

This register selects the operating parameters of the PHY LEDs when in extended mode. This register is only used when the KSZ9031 LED Mode bit in the KSZ9031 LED Mode Register is clear.

Bits	Description	Type	Default
15	**RESERVED**	R/W	—
14	**LED Activity Output Select**	R/W	0b
13	**RESERVED**	R/W	—
12	**LED Pulsing Enable**	R/W	1b
11:10	**LED Blink / Pulse-Stretch Rate** 00 = 2.5 Hz Blink Rate / 400 ms pulse-stretch 01 = 5 Hz Blink Rate / 200 ms pulse-stretch 10 = 10 Hz Blink Rate / 100 ms pulse-stretch 11 = 20 Hz Blink Rate / 50 ms pulse-stretch	R/W	00b
9	**RESERVED**	R/W	—
8:5	**LED Pulse Stretch Enables** Configures LED4 (bit 8), LED3 (bit 7), LED2 (bit 6) and LED1 (bit 5) to either pulse-stretch when 1, or blink when 0.	R/W	0000b

Bits	Description	Type	Default
4	**RESERVED**	R/W	—
1:0	**LED Combination Disables** Configures LED4 (bit 3), LED3 (bit 2), LED2 (bit 1) and LED1 (bit 0) to either combine link/activity and duplex/collision when 0, or disable combination, providing link-only and duplex-only when 1.	R/W	0000b

5.1.21 OUTPUT CONTROL REGISTER

Index (In Decimal): 25 Size: 16 bits

This register selects the output buffer type and polarity of the INT_N, MDIO and LED pins.

Bits	Description	Type	Default
15	**MDIO Buffer Type** When set to a 0, the MDIO output is open-drain When set to a 1, the MDIO output is push-pull	R/W	0b
14	**INT Buffer Type** When set to a 0, the INT_N output is open-drain When set to a 1, the INT_N output is push-pull **Note:** If the buffer type is set to open-drain, INT_N is always active low.	R/W	0b
13:8	**LED Buffer Type** When set to a 0, the LED pins are open-drain or open-source When set to a 1, the LED pins are push-pull **Bit 8 is for LED1, bit 9 for LED2, etc.**	R/W	000000b
7	**PME Polarity** When set to a 0, the PME_N pin is active low When set to a 1, the PME_N pin is active high	R/W	0b
6	**RESERVED**	R/W	—
5:0	**LED Polarity** When set to a 0, the LED pins are active low When set to a 1, the LED pins are active high Bit 0 is for LED1, bit 1 is for LED2, etc.	RO	Note 1

Note 1: Set by the inverse of the LEDPOL configuration straps.

5.1.22 KSZ9031 LED MODE REGISTER

Index (In Decimal): 26 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	R/W	—
14	**KSZ9031 LED Mode** 1 = KSZ9031 LED mode 0 = Extended LED mode **Note:** For normal LED operation, this bit should always be written as a 1.	R/W	1b
13:0	**RESERVED**	R/W	—

5.1.23 INTERRUPT STATUS REGISTER

Index (In Decimal): 27 Size: 16 bits

Reading this register clears the RC interrupt sources. RO sources must be cleared at their lower level register.

Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

Bits	Description	Type	Default
15:12	**RESERVED**	R/W	—
11	**Energy Not Detected Interrupt** 1 = “Energy not detected” interrupt 0 = No “energy not detected” interrupt This bit is set when the EDPD Low Power bit in the EDPD Control Register changes from 1 to 0.	RC	0b
10	**Energy Detected Interrupt** 1 = “Energy detected” interrupt 0 = No “energy detected” interrupt This bit is set when the EDPD Low Power bit in the EDPD Control Register changes from 0 to 1.	RC	0b
9	**1588 Interrupt** Indicates an interrupt generated from the 1588 controller. This bit is set whenever any enabled bits in the PTP Interrupt Status Register (PTP_INT_STS) are set. **Note:** The sources for these interrupts are level. The interrupt persists until the bits int he 1588 controller are cleared or disabled. 1 = 1588 interrupt 0 = No 1588 interrupt	RO	0b

Bits	Description	Type	Default
8	**GPIO Interrupt** Indicates an interrupt generated from the GPIOs. This bit is set whenever any enabled bits in the General Purpose I/O Interrupt Status Register (GPIO_INT_STS) are set. **Note:** The sources for these interrupts are level. The interrupt persists until the bits in the GPIO controller are cleared or disabled. 1 = GPIO interrupt 0 = No GPIO interrupt	RO	0b
7	**Jabber Interrupt** 1 = Jabber interrupt 0 = No jabber interrupt	RC	0b
6	**Receive Error Interrupt** 1 = Receive error interrupt 0 = No receive error interrupt	RC	0b
5	**Page Receive Interrupt** 1 = Page receive interrupt 0 = No page receive interrupt	RC	0b
4	**Parallel Detect Fault Interrupt** 1 = Parallel detection fault interrupt 0 = No parallel detection fault interrupt	RC	0b
3	**Link Partner Acknowledge Interrupt** 1 = Link partner acknowledge interrupt 0 = No link partner acknowledge interrupt	RC	0b
2	**Link Down Interrupt** 1 = Link down interrupt 0 = No link down interrupt	RC	0b
1	**ADC FIFO Error Interrupt** 1 = ADC FIFO Error interrupt 0 = No ADC FIFO Error interrupt	RC	0b
0	**Link Up Interrupt** 1 = Link up interrupt 0 = No link up interrupt	RC	0b

5.1.24 AUTO-MDI/MDI-X REGISTER

Index (In Decimal): 28 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7	**MDI Set** When the Swap-Off bit of this register is asserted (1), 1 = PHY is set to operate in MDI mode 0 = PHY is set to operate in MDI-X mode	R/W	0b

Bits	Description	Type	Default
6	**Swap-Off** 1 = Disable Auto-MDI/MDI-X function 0 = Enable Auto-MDI/MDI-X function	R/W	0b
5:0	**RESERVED**	RO	—

5.1.25 SOFTWARE POWER DOWN CONTROL REGISTER

Index (In Decimal): 29 Size: 16 bits

Bits	Description	Type	Default
15:12	**RESERVED**	R/W	—
11	**spd_clock_gate_override** 0 = internal clocks are gated during the Software Power Down (SPD) mode. 1 = internal clock gating is overridden during the SPD mode.	R/W	0b
10	**spd_pll_disable** 0 = PLL is enabled during the Software Power Down (SPD) mode. 1 = PLL is disabled during the SPD mode.	R/W	0b
9:8	**RESERVED**	R/W	—
7	**IO_DC_test_en** 1 = enable IO test	R/W	0b
6	**VOH** 1 = “VDD” to output IO 0 = “GND” to IO	R/W	0b

5.1.26 EXTERNAL LOOPBACK REGISTER

Index (In Decimal): 30 Size: 16 bits

Bits	Description	Type	Default
15:4	**RESERVED**	R/W	—
3	**Ext_lpbk** External loopback enable	R/W	0b
2:0	**RESERVED**	R/W	—

5.1.27 CONTROL REGISTER

Index (In Decimal): 31 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Interrupt Polarity Invert** 1 = invert 0 = normal	R/W	0b
13:10	**RESERVED**	RO	—
9	**Enable Jabber** 1 = Enable jabber counter 0 = Disable	R/W	1b
8	**Enable SQE Test** 1 = Enable SQE test 0 = Disable	R/W	1b
7	**RESERVED**	RO	—
6	**Speed status 1000T** Indicates speed is 1000T	RO	0b
5	**Speed status 100TX** Indicates speed is 100TX	RO	0b
4	**Speed status 10BT** Indicates speed is 10BT	RO	0b
3	**Duplex status** Indicates duplex status	RO	0b
2	**1000BASE-T Mater/Slave status** 1 = Indicates 1000BASE-T Master mode 0 = Indicates 1000BASE-T Slave mode	RO	0b
1	**Software Reset** 1 = Reset PHY except all registers 0 = Disable reset	W1S/RC	0b
0	**Link Status Check Fail** 1 = Fail 0 = Not Failing	RC	0b

5.2 MDIO Manageable Device (MMD) Registers

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. This device, however, uses only a small fraction of the available registers. See Table 3 for a list of supported MMD device addresses and their associated register addresses. These registers are accessed through the SMI (MDIO/MDC) interface.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- MMD Access Control Register
- MMD Access Address/Data Register

Example: MMD Register Write

Write MMD - Device Address 2h, Register 10h = 0001h to enable link-up detection to trigger PME for WOL.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0010h // Set address register = 10h.
3. Write the MMD Access Control Register with 4002h // Select data register for MMD – Device Address 2h.
4. Write the MMD Access Address/Data Register with 0001h // Write value 0001h to MMD – Device Address 2h, Register 10h.

Example: MMD Register Read

Read MMD - Device Address 3h, Register 14h EEE Control and Capability.

1. Write the MMD Access Control Register with 0003h // Select address register for MMD – Device Address 3h.
2. Write the MMD Access Address/Data Register with 0014h // Set address register = 14h.
3. Write the MMD Access Control Register with 4003h // Select data register for MMD – Device Address 3h.
4. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 3h, Register 14h.

It is also possible to automatically increment the register address for reads and/or writes

Example: MMD Register Writes with Post Increment

Write MMD - Device Address 2h, Register 11h – 13h = 0123_4567_89ABh for the magic packet's MAC address.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0011h // Set address register = 11h.
3. Write the MMD Access Control Register with 8002h or C002h // Select data register with post increment for MMD – Device Address 2h.
4. Write the MMD Access Address/Data Register with 0123h // Write value 0123h to MMD – Device Address 2h, Register 11h.
5. Write the MMD Access Address/Data Register with 4567h // Write value 4567h to MMD – Device Address 2h, Register 12h.
6. Write the MMD Access Address/Data Register with 89ABh // Write value 89ABh to MMD – Device Address 2h, Register 13h.

Example: MMD Register Reads with Post Increment

Read MMD - Device Address 2h, Register 11h – 13h for the magic packet's MAC address.

1. Write the MMD Access Control Register with 0002h // Select address register for MMD – Device Address 2h.
2. Write the MMD Access Address/Data Register with 0011h // Set address register = 11h.
3. Write the MMD Access Control Register with 8002h // Select data register with post increment for MMD – Device Address 2h.
4. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 11h.
5. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 12h.
6. Read the MMD Access Address/Data Register // Read data in MMD – Device Address 2h, Register 13h.

5.2.1 MEAN SLICER ERROR REGISTER

Index (In Decimal): 1.225 Size: 16 bits

Bits	Description	Type	Default
15:0	**Mean Slicer Error** This field provides the current mean error value. Either absolute or square mode values can be provided. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0000h

5.2.2 DCQ MEAN SQUARE ERROR REGISTER

Index (In Decimal): 1.226 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9	**MSE Value Valid** This field provides the mean square error valid indication. 1 = invalid 0 = valid **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0b
8:0	**MSE Value** This field provides the current mean square error value. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000h

5.2.3 DCQ MEAN SQUARE ERROR WORST CASE REGISTER

Index (In Decimal): 1.227 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9	**MSE Worst Case Value Valid** This field provides the worst case mean square error valid indication. 1 = invalid 0 = valid **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	0b
8:0	**MSE Worst Case Value** This field provides the worst case mean square error value since the last time the channel was captured for reading. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000h

5.2.4 DCQ SQI REGISTER

Index (In Decimal): 1.228 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:5	**SQI Worst Case** This field indicates the worst case SQI value since the last time the channel was captured for reading. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000b
4	**RESERVED**	RO	—

Bits	Description	Type	Default
3:1	**SQI** This field indicates the current SQI value. **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	000b
0	**RESERVED**	RO	—

5.2.5 DCQ PEAK MSE REGISTER

Index (In Decimal): 1.229 Size: 16 bits

Bits	Description	Type	Default
15:8	**Peak MSE Worst Case** This field indicates the worst case peak MSE value since the last time the channel was captured for reading. 0-63 = Peak MSE 64-254 = Invalid 255 = measurement not ready **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	00h
7:0	**Peak MSE Value** This field provides the current peak MSE value. 0-63 = Peak MSE 64-254 = Invalid 255 = measurement not ready **Note:** This field is updated when the DCQ Read Capture bit in the DCQ Control Register is written as a 1. **Note:** The DCQ Channel Number field specifies which channel is captured.	RO	00h

5.2.6 DCQ CONTROL REGISTER

Index (In Decimal): 1.230 Size: 16 bits

Bits	Description	Type	Default
15	**DCQ Read Capture** When this bit is set the DCQ values are captured.	R/W/SC	0b
14:2	**RESERVED**	R/W	—
1:0	**DCQ Channel Number** This field specifies which channel's (wire pair) values are captured into the DCQ registers. 00 = Channel A 01 = Channel B 10 = Channel C 11 = Channel D **Note:** Channel A is used for both 100BASE-TX and 1000BASE-T. Channels B-D are only used for 1000BASE-T.	R/W	00b

5.2.7 DCQ CONFIGURATION REGISTER

Index (In Decimal): 1.231 Size: 16 bits

Bits	Description	Type	Default
15:14	**scale613** Scaling factor for SQI method 5 (TC1 peak MSE).	R/W	00b
13:10	**sqi_kp3** LPF bandwidth control.for SQI method 5 (TC1 peak MSE).	R/W	101b
9:8	**scale611** Scaling factor for SQI methods 3 (TC1 MSE) and 4 (TC1 SQI).	R/W	00b
7	**sqi_reset** When set the SQI logic is reset. **Note:** This bit does not self-clear.	R/W	0b
6	**sqi_squ_mode_en** 0 = Absolute mode 1 = Square mode	R/W	1b
5	**sqi_enable** When set SQI measurements are enabled.	R/W	1b
4:0	**sqi_kp** LPF bandwidth control.for SQI methods 2 (non TC1 LPF mean), 3 (TC1 MSE) and 4 (TC1 SQI).	R/W	0Dh

5.2.8 DCQ SQI TABLE REGISTERS

Index (In Decimal): 1.232-238 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8:0	**SQI_VALUE** Lookup table utilized for implement of SQI method 4 (TC1 SQI). These registers set the thresholds to map the error value to a SQI level.	R/W	Table 5

TABLE 5: SQI VALUE DEFAULTS

Register	Default (Hexadecimal)
SQI_TBL1.SQI_VALUE	A3h
SQI_TBL2.SQI_VALUE	82h
SQI_TBL3.SQI_VALUE	67h
SQI_TBL4.SQI_VALUE	52h
SQI_TBL5.SQI_VALUE	41h
SQI_TBL6.SQI_VALUE	34h
SQI_TBL7.SQI_VALUE	29h

5.2.9 COMMON CONTROL REGISTER

Index (In Decimal): 2.0 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**Single LED** 1 = Individual-LED mode 0 = Tri-color-LED mode By default, this bit reflects the value of the LED_MODE strapping pin. If written as a 1, the value of the LED_MODE strapping pin is overridden and Single-LED mode is selected.	R/W	Note 5-3
3:2	**RESERVED**	R/W	—
1	**clk125 Enable** A 1 enables the 125 MHz clock output onto the CLK125_NDO pin.	R/W	Note 5-4
0	**All-PHYAD Enable** When this bit is set, the PHY will respond to PHY address 0 as well as it's assigned PHY address.	R/W	Note 5-5

Note 5-3 Set by the LED_MODE strapping pin.

Note 5-4 Set by the CLK125_EN strapping pin.

Note 5-5 Set by the inverse of the ALLPHYAD strapping pin.

5.2.10 STRAP STATUS REGISTER

Index (In Decimal): 2.1 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:8	**LEDPOLx Strap-In Status** Strap status of LED polarities 0 = Active low 1 = Active high	RO	Note 5-6
7	**LED_MODE Strap-In Status** 1 = Individual LED mode 0 = Tri-color LED mode	RO	Note 5-7
6	**RESERVED**	RO	—
5	**CLK125_EN Strap-In Status** 1 = CLK125_EN strap-in is enabled 0 = CLK125_EN strap-in is disabled	RO	Note 5-8
4:0	**PHYAD[2:0] Strap-In Status** Strap-in value for PHY address **Note:** Bits [4:3] of PHY address are always set to '00'.	RO	Note 5-9

Note 5-6 Set by the inverse of the LEDPOL6 through LEDPOL1 strapping pins.

Note 5-7 Set by the LED_MODE strapping pin.

Note 5-8 Set by the CLK125_EN strapping pin.

Note 5-9 Set by the PHYAD[2:0] strapping pins.

5.2.11 OPERATION MODE STRAP OVERRIDE REGISTER

Index (In Decimal): 2.2 Size: 16 bits

This register may be used to override the value of the MODE[4:0], RGMII_EN, and MAGJACK configuration straps.

Following an update to this register, a PHY Soft Reset (RESET) should be issued into the Basic Control Register in order for the new value to take effect.

APPLICATION NOTE: When setting a new value, it is the user's responsibility to ensure that conflicting assignments are not made.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**MagJack_mode** Forced MagJack mode 1 = Forced MagJack mode	R/W NASR	Note 5-10
13	**1000_FD_slave_mode** Forced 1000BASE-T full duplex slave mode 1 = Forced 1000BT FD slave mode	R/W NASR	Note 5-12
12	**100_HD_mode** Forced 100BASE-TX half duplex mode 1 = Forced 100BT HD mode	R/W NASR	Note 5-12
11	**100_FD_mode** Forced 100BASE-TX full duplex mode 1 = Forced 100BT FD mode	R/W NASR	Note 5-12
10	**1000_FD_master_mode** Forced 1000BASE-T full duplex master mode 1 = Forced 1000BT FD master mode	R/W NASR	Note 5-12
9	**spd_pll_dis_mode** Software Power Down with PLL disabled mode 1 = SPD w/pll disabled mode	R/W NASR	Note 5-12
8	**spd_pll_en_mode** Software Power Down with PLL enabled mode 1 = SPD w/pll enable mode	R/W NASR	Note 5-12
7	**iddq_scan_mode** IDDQ scan mode 1 = IDDQ scan mode	RO NASR	Note 5-12
6:5	**RESERVED**	RO	—
4	**ntree_mode** NAND Tree mode 1 = NAND Tree mode	R/W NASR	Note 5-12
3:0	**RESERVED**	RO	—

Note 5-10 Set by the MAGJACK strapping pin as indicated by the corresponding but in the Operation Mode Strap Register.

Note 5-11 Writable to a 1 if scan_mode is set and Strap_iddq_scan_mode is clear in the Operation Mode Strap Register.

Note 5-12 Set by the MODE[4:0] strapping pins.

5.2.12 OPERATION MODE STRAP REGISTER

Index (In Decimal): 2.3 Size: 16 bits

This register indicates the value of the MODE[4:0], RGMII_EN, and MAGJACK configuration straps that were latched into the device at reset.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Strap_magjack_mode** MagJack Strap-In Status 1 = MagJack mode	RO	Note 5-13
13	**Strap_1000_FD_slave_mode** Forced 1000BASE-T full duplex slave Strap-In Status 1 = Forced 1000BT FD slave mode (MODE[4:0]='01101')	RO	Note 5-14
12	**Strap_100_HD_mode** Forced 100BASE-TX half duplex Strap-In Status 1 = Forced 100BT HD mode (MODE[4:0]='01100')	RO	Note 5-14
11	**Strap_100_FD_mode** Forced 100BASE-TX full duplex Strap-In Status 1 = Forced 100BT FD mode (MODE[4:0]='01011')	RO	Note 5-14
10	**Strap_1000_FD_master_mode** Forced 1000BASE-T full duplex master Strap-In Status 1 = Forced 1000BT FD master mode (MODE[4:0]='01010')	RO	Note 5-14
9	**Strap_spd_pll_dis_mode** Software Power Down with PLL disabled Strap-In Status 1 = SPD w/pll disabled mode (MODE[4:0]='01001')	RO	Note 5-14
8	**Strap_spd_pll_en_mode** Software Power Down with PLL enabled Strap-In Status 1 = SPD w/pll enable mode (MODE[4:0]='01000')	RO	Note 5-14
7	**Strap_iddq_scan_mode** IDDQ Scan Strap-In Status 1 = IDDQ scan mode (MODE[4:0]='00111')	RO	Note 5-14
6:5	**RESERVED**	RO	—
4	**Strap_ntree_mode** NAND Tree Strap-In Status 1 = NAND Tree mode (MODE[4:0]='00100')	RO	Note 5-14
3:0	**RESERVED**	RO	—

Note 5-13 Set by the MAGJACK strapping pin as indicated by the corresponding but in the Operation Mode Strap Register.

Note 5-14 Set by the MODE[3:0] strapping pins.

5.2.13 CLOCK INVERT AND CONTROL SIGNAL PAD SKEW REGISTER

Index (In Decimal): 2.4 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	R/W	0h
8	**Inverse RGMII TXC Input** 0 = no change 1 = inverse on TXC for RGMII	R/W	0b
7:4	**RX_CTL Skew** RX_CTL output skew Control (0.1 ns/step)	R/W	7h
3:0	**TX_CTL Skew** TX_CTL input skew Control (0.1 ns/step)	R/W	7h

5.2.14 RGMII RX DATA PAD SKEW REGISTER

Index (In Decimal): 2.5 Size: 16 bits

Bits	Description	Type	Default
15:12	**RXD3 Pad Skew** RGMII RXD3 output pad skew control (0.1 ns/step)	R/W	7h
11:8	**RXD2 Pad Skew** RGMII RXD2 output pad skew control (0.1 ns/step)	R/W	7h
7:4	**RXD1 Pad Skew** RGMII RXD1 output pad skew control (0.1 ns/step)	R/W	7h
3:0	**RXD0 Pad Skew** RGMII RXD0 output pad skew control (0.1 ns/step)	R/W	7h

5.2.15 RGMII TX DATA PAD SKEW REGISTER

Index (In Decimal): 2.6 Size: 16 bits

Bits	Description	Type	Default
15:12	**TXD3 Pad Skew** RGMII TXD3 output pad skew control (0.1 ns/step)	R/W	7h
11:8	**TXD2 Pad Skew** RGMII TXD2 output pad skew control (0.1 ns/step)	R/W	7h
7:4	**TXD1 Pad Skew** RGMII TXD1 output pad skew control (0.1 ns/step)	R/W	7h
3:0	**TXD0 Pad Skew** RGMII TXD0 output pad skew control (0.1 ns/step)	R/W	7h

5.2.16 CLOCK PAD SKEW REGISTER

Index (In Decimal): 2.8 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9:5	**TXC Pad Input Skew** TXC input Skew Control (~24 min to ~58 max ps/step)	R/W	07h
4:0	**RXC Pad Output Skew** RXC output Skew Control (~24 min to ~58 max ps/step)	R/W	07h

5.2.17 SELF-TEST PACKET COUNT LO REGISTER

Index (In Decimal): 2.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[15:0]**	R/W	0000h

5.2.18 SELF-TEST PACKET COUNT HI REGISTER

Index (In Decimal): 2.10 Size: 16 bits

Bits	Description	Type	Default
15:0	**Self_test_frame_cnt[31:16]**	R/W	0001h

5.2.19 SELF-TEST STATUS REGISTER

Index (In Decimal): 2.11 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_done** 0 = Self test running 1 = Self test finished	RO	0b

5.2.20 SELF-TEST FRAME COUNT ENABLE REGISTER

Index (In Decimal): 2.12 Size: 16 bits

Bits	Description	Type	Default
15:1	**RESERVED**	RO	—
0	**Self_test_frame_cnt_en** 0 = disabled 1 = enabled	R/W	0b

5.2.21 SELF-TEST PGEN ENABLE REGISTER

Index (In Decimal): 2.13 Size: 16 bits

Bits	Description	Type	Default
15:5	**RESERVED**	RO	—
4	**Force_self_test_pgen_en** 0 = packet generator needs to wait for link up to start sending data 1 = packet generator sends data regardless of link status	R/W	0b
3:1	**RESERVED**	RO	—
0	**Self_test_pgen_en** 0 = disabled 1 = enabled	R/W	0b

5.2.22 SELF-TEST ENABLE REGISTER

Index (In Decimal): 2.14 Size: 16 bits

Bits	Description	Type	Default
15	**Self_test_external_clk_sel** **Note:** This bit is not used.	R/W	0b
14:13	**Self_test_packet_type[1:0]** 00 = random data bit 01 = all data bits and SA/DA are 0 10 = all data bits and SA/DA are 1 11 = random	R/W	00b
12:10	**RESERVED**	RO	—
9	**Self_test_clear_counters_on_link_down** 1 = clear counters on link drop 0 = don't clear counters on link drop	R/W	0b
8	**Self_test_CRC_checker_enable** 1 = Enable 0 = Disable	R/W	0b
7:5	**RESERVED**	RO	—
4	**GMII_TX_CRC_check_en** Enables CRC_checker in Tx path (toward line) 0 = disabled 1 = enabled	R/W	0b
3:1	**RESERVED**	RO	—

Bits	Description	Type	Default
0	**Self_test_en** 0 = disabled 1 = enabled	R/W	0b

5.2.23 WAKE-ON-LAN CONTROL REGISTER

Index (In Decimal): 2.16 Size: 16 bits

Bits	Description	Type	Default
15:14	**PME Output Select** Controls definition of PME_N signal. 00 = PME 01 = Interrupt 10 = Interrupt ORed with PME 11 = always 0 **Note:** This field controls the PME_N function regardless of the pin to which PME_N is mapped.	R/W	00b
13	**RESERVED**	R/W	—
12	**Enable Energy Not Detected Wake Event** Enables energy not detected as a wake event	R/W	0b
11	**Enable Energy Detected Wake Event** Enables energy detected as a wake event	R/W	0b
7	**Wake-on-LAN Reset (Wol_reset)** Write a 1 then a 0 to reset the WoL module.	R/W	0b
6	**Enable Magic Packet Detection Wake Event** Enables magic packet detection as a wake event	R/W	0b
5:2	**Enable Customized Frame Filter Wake Event** Enables customized frame filters as wake events	R/W	0h
1	**Enable Link Down Wake Event** Enables link down as a wake event	R/W	0b
0	**Enable Link Up Wake Event** Enables link up as a wake event	R/W	0b

5.2.24 WAKE-ON-LAN-MAC-LO REGISTER

Index (In Decimal): 2.17 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-lo** MAC-Address[15:0] of magic packet	R/W	0000h

5.2.25 WAKE-ON-LAN-MAC-MI REGISTER

Index (In Decimal): 2.18 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-mi** MAC-Address[31:16] of magic packet	R/W	0000h

5.2.26 WAKE-ON-LAN-MAC-HI REGISTER

Index (In Decimal): 2.19 Size: 16 bits

Bits	Description	Type	Default
15:0	**m-pkt-mac-hi** MAC-Address[47:32] of magic packet	R/W	0000h

5.2.27 CUSTOMIZED-PKT-0-CRC-LO REGISTER

Index (In Decimal): 2.20 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-crc-lo** Customized frame filter 0 CRC[15:0]	R/W	0000h

5.2.28 CUSTOMIZED-PKT-0-CRC-HI REGISTER

Index (In Decimal): 2.21 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-crc-hi** Customized frame filter 0 CRC[31:16]	R/W	0000h

5.2.29 CUSTOMIZED-PKT-1-CRC-LO REGISTER

Index (In Decimal): 2.22 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-crc-lo** Customized frame filter 1 CRC[15:0]	R/W	0000h

5.2.30 CUSTOMIZED-PKT-1-CRC-HI REGISTER

Index (In Decimal): 2.23 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-crc-hi** Customized frame filter 1 CRC[31:16]	R/W	0000h

5.2.31 CUSTOMIZED-PKT-2-CRC-LO REGISTER

Index (In Decimal): 2.24 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-crc-lo** Customized frame filter 2 CRC[15:0]	R/W	0000h

5.2.32 CUSTOMIZED-PKT-2-CRC-HI REGISTER

Index (In Decimal): 2.25 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-crc-hi** Customized frame filter 2 CRC[31:16]	R/W	0000h

5.2.33 CUSTOMIZED-PKT-3-CRC-LO REGISTER

Index (In Decimal): 2.26 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-crc-lo** Customized frame filter 3 CRC[15:0]	R/W	0000h

5.2.34 CUSTOMIZED-PKT-3-CRC-HI REGISTER

Index (In Decimal): 2.27 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-crc-hi** Customized frame filter 3 CRC[31:16]	R/W	0000h

5.2.35 CUSTOMIZED-PKT-0-MASK_LL REGISTER

Index (In Decimal): 2.28 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-ll** Customized frame filter 0 mask[15:0]	R/W	0000h

5.2.36 CUSTOMIZED-PKT-0-MASK_LH REGISTER

Index (In Decimal): 2.29 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-lh** Customized frame filter 0 mask[31:16]	R/W	0000h

5.2.37 CUSTOMIZED-PKT-0-MASK_HL REGISTER

Index (In Decimal): 2.30 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-hl** Customized frame filter 0 mask[47:32]	R/W	0000h

5.2.38 CUSTOMIZED-PKT-0-MASK_HH REGISTER

Index (In Decimal): 2.31 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-0-mask-hh** Customized frame filter 0 mask[63:48]	R/W	0000h

5.2.39 CUSTOMIZED-PKT-1-MASK_LL REGISTER

Index (In Decimal): 2.32 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-ll** Customized frame filter 1 mask[15:0]	R/W	0000h

5.2.40 CUSTOMIZED-PKT-1-MASK_LH REGISTER

Index (In Decimal): 2.33 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-lh** Customized frame filter 1 mask[31:16]	R/W	0000h

5.2.41 CUSTOMIZED-PKT-1-MASK_HL REGISTER

Index (In Decimal): 2.34 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-hl** Customized frame filter 1 mask[47:32]	R/W	0000h

5.2.42 CUSTOMIZED-PKT-1-MASK_HH REGISTER

Index (In Decimal): 2.35 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-1-mask-hh** Customized frame filter 1 mask[63:48]	R/W	0000h

5.2.43 CUSTOMIZED-PKT-2-MASK_LL REGISTER

Index (In Decimal): 2.36 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-ll** Customized frame filter 2 mask[15:0]	R/W	0000h

5.2.44 CUSTOMIZED-PKT-2-MASK_LH REGISTER

Index (In Decimal): 2.37 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-lh** Customized frame filter 2 mask[31:16]	R/W	0000h

5.2.45 CUSTOMIZED-PKT-2-MASK_HL REGISTER

Index (In Decimal): 2.38 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-hl** Customized frame filter 2 mask[47:32]	R/W	0000h

5.2.46 CUSTOMIZED-PKT-2-MASK_HH REGISTER

Index (In Decimal): 2.39 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-2-mask-hh** Customized frame filter 2 mask[63:48]	R/W	0000h

5.2.47 CUSTOMIZED-PKT-3-MASK_LL REGISTER

Index (In Decimal): 2.40 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-ll** Customized frame filter 3 mask[15:0]	R/W	0000h

5.2.48 CUSTOMIZED-PKT-3-MASK_LH REGISTER

Index (In Decimal): 2.41 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-lh** Customized frame filter 3 mask[31:16]	R/W	0000h

5.2.49 CUSTOMIZED-PKT-3-MASK_HL REGISTER

Index (In Decimal): 2.42 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-hl** Customized frame filter 3 mask[47:32]	R/W	0000h

5.2.50 CUSTOMIZED-PKT-3-MASK_HH REGISTER

Index (In Decimal): 2.43 Size: 16 bits

Bits	Description	Type	Default
15:0	**c-pkt-3-mask-hh** Customized frame filter 3 mask[63:48]	R/W	0000h

5.2.51 WAKE-ON-LAN CONTROL STATUS REGISTER

Index (In Decimal): 2.44 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_ctrl_status** Wake-on-LAN Control module status	RO	0000h

5.2.52 WAKE-ON-LAN CUSTOM PACKET RECEIVE STATUS REGISTER

Index (In Decimal): 2.45 Size: 16 bits

Bits	Description	Type	Default
15	**cpkt_pmen** custom packet 0 enabled and custom packet 0 found	RO	0b
14:12	**mismatch code**	RO	000b
11	**good_pkt_crc**	RO	0b
10:7	**crc_match** crc matched bit 10 = custom packet 3 bit 9 = custom packet 2 bit 8 = custom packet 1 bit 7 = custom packet 0	RO	0000b
6:3	**cpkt_found** custom packet found bit 6 = custom packet 3 bit 5 = custom packet 2 bit 4 = custom packet 1 bit 3 = custom packet 0	RO	0000b
2:0	**cpkt_state** custom packet detection state	RO	000b

5.2.53 WAKE-ON-LAN MAGIC PACKET RECEIVE STATUS REGISTER

Index (In Decimal): 2.46 Size: 16 bits

Bits	Description	Type	Default
15	**mpkt_pmen** magic packet enabled and magic packet found	RO	0b
14:12	**byte count**	RO	000b
11:9	**mismatch code**	RO	000b
8:5	**macda_match_count**	RO	0h
4	**good_pkt_crc**	RO	0b
3	**mpkt_found** magic packet found	RO	0b
2:0	**mpkt_state** magic packet detection state	RO	000b

5.2.54 WAKE-ON-LAN DATA MODULE STATUS REGISTER

Index (In Decimal): 2.47 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_data_status** Wake-on-LAN Data module status	RO	0000h

5.2.55 CUSTOMIZED PKT-0 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.48 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_0 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 0	RO	0000h

5.2.56 CUSTOMIZED PKT-0 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.49 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_0 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 0	RO	0000h

5.2.57 CUSTOMIZED PKT-1 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.50 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_1 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 1	RO	0000h

5.2.58 CUSTOMIZED PKT-1 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.51 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_1 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 1	RO	0000h

5.2.59 CUSTOMIZED PKT-2 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.52 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_2 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 2	RO	0000h

5.2.60 CUSTOMIZED PKT-2 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.53 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_2 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 2	RO	0000h

5.2.61 CUSTOMIZED PKT-3 RECEIVED CRC-L REGISTER

Index (In Decimal): 2.54 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_3 [15:0]** Wake-on-LAN CRC [15:0] calculated on Customized frame filter 3	RO	0000h

5.2.62 CUSTOMIZED PKT-3 RECEIVED CRC-H REGISTER

Index (In Decimal): 2.55 Size: 16 bits

Bits	Description	Type	Default
15:0	**Wol_crc_rcv_3 [31:16]** Wake-on-LAN CRC [31:16] calculated on Customized frame filter 3	RO	0000h

5.2.63 SELF-TEST CORRECT COUNT LO REGISTER

Index (In Decimal): 2.60 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count HI Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[15:0]**	RO	—

5.2.64 SELF-TEST CORRECT COUNT HI REGISTER

Index (In Decimal): 2.61 Size: 16 bits

Following a self-test, this register along with Self-Test Correct Count LO Register indicate the count of frames with a correct FCS.

Bits	Description	Type	Default
15:0	**Self_test_correct_cnt[31:16]**	RO	—

5.2.65 SELF-TEST ERROR COUNT LO REGISTER

Index (In Decimal): 2.62 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count HI Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[15:0]**	RO	—

5.2.66 SELF-TEST ERROR COUNT HI REGISTER

Index (In Decimal): 2.63 Size: 16 bits

Following a self-test, this register along with Self-Test Error Count LO Register indicate the count of frames with an incorrect FCS.

Bits	Description	Type	Default
15:0	**Self_test_error_cnt[31:16]**	RO	—

5.2.67 RX DLL CONTROL REGISTER

Index (In Decimal): 2.76 Size: 16 bits

Bits	Description	Type	Default
15	**rxdll_tune_disable** When this bit is set the DLL is not dynamically tuned. It is, however, still used to provide a fixed delay as set by rxdll_tap_sel.	R/W	0b
14	**bypass rxdll** 1 = RXC DLL delay is not used	R/W	0b
13:7	**rxdll_tap_sel** Used as the initial DLL tap setting before the first tuning cycle. Also used to set the delay value during manual tuning mode. **Note:** The rxdll_reset bit must be set following a change to this field.	R/W	1Bh
6:0	**rxdll_tap_adj** **Note:** Used to statically account for the output multiplexer stage in the delay chain when DLL tuning is enabled.	R/W	1Bh

5.2.68 TX DLL CONTROL REGISTER

Index (In Decimal): 2.77 Size: 16 bits

Bits	Description	Type	Default
15	**txdll_tune_disable** When this bit is set the DLL is not dynamically tuned. It is, however, still used to provide a fixed delay as set by txdll_tap_sel.	R/W	0b
14	**bypass txdll** 1 = TXC DLL delay is not used	R/W	1b
13:7	**txdll_tap_sel** Used as the initial DLL tap setting before the first tuning cycle. Also used to set the delay value during manual tuning mode. **Note:** The txdll_reset bit must be set following a change to this field.	R/W	1Bh
6:0	**txdll_tap_adj** **Note:** Used to statically account for the output multiplexer stage in the delay chain when DLL tuning is enabled.	R/W	1Bh

5.2.69 1000M FAST LINK DOWN ENABLE REGISTER

Index (In Decimal): 2.90 Size: 16 bits

Bits	Description	Type	Default
15:9	**RESERVED**	R/O	—
8	**1000M Fast Link Down Enable** Enable 1000BT fast link loss time (< 50 µs) onto Link Down Interrupt (PHY Register 27). Also maps Link Down Interrupt onto INT_N interrupt pin.	R/W	0b
7:0	**RESERVED**	R/O	—

5.2.70 DRIVING STRENGTH, FAST LINK DOWN, S2P RX PCS SELECT SETTING REGISTER

Index (In Decimal): 2.111 Size: 16 bits

Bits	Description	Type	Default
15:13	**RESERVED**	R/W	—
12	**Fast Link Fail Enable** Enable 1000/100 BT fast link loss time (< 15us) into in RGMII in-band status when not operating with EEE	R/W	0b
11:0	**RESERVED**	R/W	—

5.2.71 GENERAL PURPOSE IO ENABLE REGISTER (GPIO_EN)

Index (In Decimal): 2.128 Size: 16 bits

This register enables the GPIO onto its shared pin.

In order for a GPIO to function as an interrupt source, it must be configured as an input.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Enable (GPIO_EN)** When set, the pin functions as a GPIO.	R/W	000h

5.2.72 GENERAL PURPOSE IO DIRECTION REGISTER (GPIO_DIR)

Index (In Decimal): 2.129 Size: 16 bits

This register controls the GPIO direction.

In order for a GPIO to function as an interrupt source, it must be configured as an input.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Direction (GPIO_DIR)** When set, enables the corresponding GPIO as an output. When cleared the GPIO is enabled as an input.	R/W	000h

5.2.73 GENERAL PURPOSE IO BUFFER TYPE REGISTER (GPIO_BUF)

Index (In Decimal): 2.130 Size: 16 bits

This register sets the GPIO output buffer type.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Buffer Type (GPIO_BUF)** When set, the output buffer for the corresponding GPIO signal is configured as a push/pull driver. When cleared, the corresponding GPIO signal is configured as an open-drain driver.	R/W	000h

5.2.74 GENERAL PURPOSE IO DATA SELECT 1 REGISTER (GPIO_DATA_SEL1)

Index (In Decimal): 2.131 Size: 16 bits

This register selects the GPIO output data source value for GPIO 0-4.

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14:12	**GPIO 4 Data Select (GPIO4_DATA_SEL)** This field selects the output data source for GPIO 4. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
11:9	**GPIO 3 Data Select (GPIO3_DATA_SEL)** This field selects the output data source for GPIO 3. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
8:6	**GPIO 2 Data Select (GPIO2_DATA_SEL)** This field selects the output data source for GPIO 2. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
5:3	**GPIO 1 Data Select (GPIO1_DATA_SEL)** This field selects the output data source for GPIO 1. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
2:0	**GPIO 0 Data Select (GPIO0_DATA_SEL)** This field selects the output data source for GPIO 0. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b

5.2.75 GENERAL PURPOSE IO DATA SELECT 2 REGISTER (GPIO_DATA_SEL2)

Index (In Decimal): 2.132 Size: 16 bits

This register selects the GPIO output data source value for GPIO 5-6.

Bits	Description	Type	Default
15:6	**RESERVED**	RO	—
5:3	**GPIO 6 Data Select (GPIO6_DATA_SEL)** This field selects the output data source for GPIO 6. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b
2:0	**GPIO 5 Data Select (GPIO5_DATA_SEL)** This field selects the output data source for GPIO 5. 000 : GPIO data register 001 : 1588 Event A 010 : 1588 Event B 011 : PME_N 100 : TX SFD 101 : RX SFD 11x : reserved	R/W	000b

5.2.76 GENERAL PURPOSE IO DATA REGISTER (GPIO_DATA)

Index (In Decimal): 2.133 Size: 16 bits

This register sets or reads the GPIO data value.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Data (GPIO_D)** When enabled as an output, the value written is reflected on the GPIO. When read, the value always reflects the current state of the corresponding GPIO pin, regardless of the value written or the GPIO direction.	R/W	000h

5.2.77 GENERAL PURPOSE IO INTERRUPT STATUS REGISTER (GPIO_INT_STS)

Index (In Decimal): 2.134 Size: 16 bits

This register contains the GPIO interrupt status bits.

Reading this register clears the interrupt status.

Interrupt status bits in this register reflect the state of the interrupt source regardless of the state of the corresponding enable.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Interrupt (GPIO_INT)** Interrupts generated from the GPIOs. **Note:** The sources for these interrupts are level sensitive. **Note:** The GPIO inputs must be stable for ~85ns (2 consecutive 25MHz edges) to be recognized.	RC	Note 5-15

Note 5-15 The default depends on the state of the GPIO pin

5.2.78 GENERAL PURPOSE IO INTERRUPT ENABLE REGISTER (GPIO_INT_EN)

Index (In Decimal): 2.135 Size: 16 bits

This register is used to enable the corresponding bits in the General Purpose IO Interrupt Status Register (GPIO_INT_STS) as an interrupt source.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Interrupt Enable (GPIO_INT_EN)** When set, interrupts are enabled from the GPIOs.	R/W	000h

5.2.79 GENERAL PURPOSE IO INTERRUPT POLARITY REGISTER (GPIO_INT_POL)

Index (In Decimal): 2.136 Size: 16 bits

This register configures the interrupt polarity.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:0	**GPIO Interrupt Polarity (GPIO_INT_POL)** When clear, an interrupt is triggered when the GPIO input is low. When set, an interrupt is triggered when the GPIO input is high.	R/W	000h

5.2.80 PTP COMMAND AND CONTROL REGISTER (PTP_CMD_CTL)

Index (In Decimal): 2.256 Size: 16 bits

Bits	Description	Type	Default
15	**LTC Delayed Step Seconds (PTP_LTC_DLYD_STEP_SECONDS)** Writing a one to this bit arms the adding or subtracting of the lower four bits of the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE) field in the PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO) to or from the seconds portion of the 1588 Local Time Counter. The choice of adding or subtracting is set using the LTC Step Adjustment Direction (PTP_LTC_STEP_ADJ_DIR) bit. Once armed, the 1588 Local Time Counter is adjusted when the Local Time Counter nanoseconds rolls over to or past zero. This bit self-clears at that time. Writing a zero to this bit has no effect. This action is only valid when the LTC Adjustment Select (PTP_LTC_ADJ_SEL) bit in the PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_ADJ_CFG) = 0.	W1S/SC	0b
14	**LTC Delayed Load (PTP_LTC_DLYD_LOAD)** Writing a one to this bit arms the delayed writing of the value of the PTP LTC Set Seconds High/Mid/Low Registers (PTP_LTC_SET_SEC_HI/MID/LO), the PTP LTC Set Nanoseconds High/Low Registers (PTP_LTC_SET_NS_HI/LO) and the PTP LTC Set Sub-Nanoseconds High/Low Registers (PTP_LTC_SET_SUBNS_HI/LO) into the 1588 Local Time Counter. Once armed, the 1588 Local Time Counter is loaded when the Local Time Counter nanoseconds rolls over to or past zero. This bit self-clears at that time. Writing a zero to this bit has no effect. This action is only valid when the LTC Adjustment Select (PTP_LTC_ADJ_SEL) bit in the PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_ADJ_CFG) = 0.	W1S/SC	0b
13	**LTC Target Read (PTP_LTC_TARGET_READ)** Writing a one to this bit causes the current values of both of the 1588 Local Time targets (A and B) to be saved into the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and the PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) so they can be read. Writing a zero to this bit has no effect.	W1S/SC	0b
12:9	**PTP Manual Capture Select 3-0 (PTP_MANUAL_CAPTURE_SEL[3:0])** These bits specify which GPIO PTP LTC Capture Registers are used during a manual capture. Bit 3 selects the rising edge (0) or falling edge (1) registers. Bits 2-0 select the GPIO number. **Note:** All 8 GPIO register sets are available.	R/W	0000b

Bits	Description	Type	Default
8	**PTP Manual Capture (PTP_MANUAL_CAPTURE)** Writing a one to this bit causes the current value of the 1588 Local Time Counter to be saved into the GPIO PTP LTC Capture Registers specified above. The corresponding bit in the PTP Interrupt Status Register (PTP_INT_STS) is also set. Writing a zero to this bit has no effect.	W1S/SC	0b
7	**LTC Temporary Rate (PTP_LTC_TEMP_RATE)** Writing a one to this bit enables the use of the temporary Local Time rate adjustment specified in the PTP LTC Temporary Rate Adjustment High/Low Registers (PTP_LTC_TEMP_RATE_ADJ_HI/LO) for the duration specified in the PTP LTC Temporary Rate Duration High/Low Registers (PTP_LTC_-TEMP_RATE_DURATION_HI/LO). Writing a zero to this bit has no effect. This action is only valid when the LTC Adjustment Select (PTP_LTC_ADJ_-SEL) bit in the PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_ADJ_CFG) = 0.	W1S/SC	0b
6	**LTC Step Nanoseconds (PTP_LTC_STEP_NANOSECONDS)** Writing a one to this bit adds the value of the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE) field in the PTP LTC Step Adjustment High/Low Registers (PTP_LTC_STEP_ADJ_HI/LO) to the nanoseconds portion of the 1588 Local Time Counter. Writing a zero to this bit has no effect. This action is only valid when the LTC Adjustment Select (PTP_LTC_ADJ_-SEL) bit in the PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_ADJ_CFG) = 0.	W1S/SC	0b
5	**LTC Step Seconds (PTP_LTC_STEP_SECONDS)** Writing a one to this bit adds or subtracts the lower four bits of the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE) field in the PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO) to or from the seconds portion of the 1588 Local Time Counter. The choice of adding or subtracting is set using the LTC Step Adjustment Direction (PTP_LTC_STEP_ADJ_DIR) bit. Writing a zero to this bit has no effect. This action is only valid when the LTC Adjustment Select (PTP_LTC_ADJ_-SEL) bit in the PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_ADJ_CFG) = 0.	W1S/SC	0b

Bits	Description	Type	Default
4	**LTC Load (PTP_LTC_LOAD)** Writing a one to this bit writes the value of the PTP LTC Set Seconds High/Mid/Low Registers (PTP_LTC_SET_SEC_HI/MID/LO), the PTP LTC Set Nanoseconds High/Low Registers (PTP_LTC_SET_NS_HI/LO) and the PTP LTC Set Sub-Nanoseconds High/Low Registers (PTP_LTC_SET_-SUBNS_HI/LO) into the 1588 Local Time Counter. Writing a zero to this bit has no effect. This action is only valid when the LTC Adjustment Select (PTP_LTC_ADJ_-SEL) bit in the PTP LTC External Adjustment Configuration Register (PTP_LTC_EXT_ADJ_CFG) = 0.	W1S/SC	0b
3	**LTC Read (PTP_LTC_READ)** Writing a one to this bit causes the current value of the 1588 Local Time Counter to be saved into the PTP LTC Read Seconds High/Mid/Low Registers (PTP_LTC_RD_SEC_HI/MID/LO), the PTP LTC Read Nanoseconds High/Low Registers (PTP_LTC_RD_NS_HI/LO) and the PTP LTC Read Sub-Nanoseconds High/Low Registers (PTP_LTC_RD_SUBNS_HI/LO) so it can be read. Writing a zero to this bit has no effect.	W1S/SC	0b
2	**PTP Enable (PTP_ENABLE)** Writing a one to this bit will enable the 1588 unit. Reading this bit will return the current enabled value. Writing a zero to this bit has no effect.	R/W1S	0b
1	**PTP Disable (PTP_DISABLE)** Writing a one to this bit will cause the PTP Enable (PTP_ENABLE) to clear once all current frame processing is completed. No new frame processing will be started if this bit is set. Writing a zero to this bit has no effect.	W1S/SC	0b
0	**PTP Reset (PTP_RESET)** Writing a one to this bit resets the 1588 H/W, state machines and registers and disables the 1588 unit. Any frame modifications in progress are halted at the risk of causing frame data or FCS errors. PTP_Reset should only be used once the 1588 unit is disabled as indicated by the PTP Enable (PTP_ENABLE) bit. Writing a zero to this bit has no effect.	W1S/SC	0b

5.2.81 PTP GENERAL CONFIGURATION REGISTER (PTP_GENERAL_CONFIG)

Index (In Decimal): 2.257 Size: 16 bits

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Time-Stamp Unit Enable (TSU_ENABLE)** This bit enables the receive and transmit functions of the time-stamp unit. The PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) bit must also be set. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set. **ARCHITECTURE NOTE:** The design actually supports the changing of TSU_ENABLE when PTP_ENABLE is set. If this is to be supported, the various bits related to the TSU that are noted to “not be changed” when PTP_ENABLE is set need to be edited to state “not to be changed” when TSU_ENABLE is set (or perhaps when TSU_ENABLE and PTP_ENABLE are both set).	R/W	1b
13	**GPIO Falling Edge Capture Remap** This bit selects GPIOs 8-9 for falling edge capture in place of GPIOs 0-1.	R/W	0b
12	**GPIO Rising Edge Capture Remap** This bit selects GPIOs 8-9 for rising edge capture in place of GPIOs 0-1.	R/W	0b
11:8	**Local Time Event Channel B Mode (LTC_EVENT_B)** These bits determine the output on Local Time Event Channel B when a Local Time Target compare event occurs. 0000 : 100ns 0001 : 500ns 0010 : 1us 0011 : 5us 0100 : 10us 0101 : 50us 0110 : 100us 0111 : 500us 1000 : 1ms 1001 : 5ms 1010 : 10ms 1011 : 50ms 1100 : 100ms 1101 : 200ms 1110 : Toggle 1111 : PTP_TIMER_INT_B bit value in the PTP_INT_STS register	R/W	0h

Bits	Description	Type	Default
7:4	**Local Time Event Channel A Mode (LTC_EVENT_A)** These bits determine the output on Local Time Event Channel A when a Local Time Target compare event occurs. 0000 : 100ns 0001 : 500ns 0010 : 1us 0011 : 5us 0100 : 10us 0101 : 50us 0110 : 100us 0111 : 500us 1000 : 1ms 1001 : 5ms 1010 : 10ms 1011 : 50ms 1100 : 100ms 1101 : 200ms 1110 : Toggle 1111 : PTP_TIMER_INT_A bit value in the PTP_INT_STS register	R/W	0h
3	**Local Time Event Polarity Channel B (LTC_EVENT_POL_B)** This bit determines the output polarity of Local Time Event Channel B. 0 : Active low 1 : Active high **Note:** The polarity applies to all event modes including the Toggle mode.	R/W	0b
2	**Reload/Add B (RELOAD_ADD_B)** This bit determines the course of action when a Local Time Target compare event for Local Time Event Channel B occurs. When set, the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) are loaded from the PTP LTC Target x Reload / Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload / Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) x=B. When low, the Local Time Target Registers are incremented by the Local Time Target Reload Registers. 0 : Increment upon a Local Time target compare event 1 : Reload upon a Local Time target compare event	R/W	0b
1	**Local Time Event Polarity Channel A (LTC_EVENT_POL_A)** This bit determines the output polarity of Local Time Event Channel A. 0 : Active low 1 : Active high **Note:** The polarity applies to all event modes including the Toggle mode.	R/W	0b

Bits	Description	Type	Default
0	**Reload/Add A (RELOAD_ADD_A)** This bit determines the course of action when a Local Time Target compare event for Local Time Event Channel A occurs. When set, the PTP LTC Target x Seconds High/Low Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and PTP LTC Target x Nanoseconds High/Low Registers (PTP_LTC_TARGET_NS_HI/LO_x) are loaded from the PTP LTC Target x Reload / Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and PTP LTC Target x Reload / Add Nanoseconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) x=A. When low, the Local Time Target Registers are incremented by the Local Time Target Reload Registers. 0 : Increment upon a Local Time target compare event 1 : Reload upon a Local Time target compare event	R/W	0b

5.2.82 PTP REFERENCE CLOCK CONFIGURATION REGISTER (PTP_REF_CLK_CFG)

Index (In Decimal): 2.258 Size: 16 bits

This read/write register configures the 1588 reference clock.

Bits	Description	Type	Default
15:13	**Reference Clock Source** This field selects the source of the 1588 reference clock. 000 : internal 125MHz 001 : internal 200MHz 010 : internal 250MHz 011 : receive clock 100 : external input 101 : reserved 110 : reserved 111 : reserved **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000b
12	**Reference Clock Period Override** When clear, the period of the reference clock is determined by the H/W based on the source selection and the current receive data rate if needed. When set, the period of the reference clock is specified by the value in the Reference Clock Period field. This field is not use when the reference clock source is the external input. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
11:9	**RESERVED**	RO	—
8:0	**Reference Clock Period** This field specifies the period, in nanoseconds, of the reference clock. When the Reference Clock Period Override field is set or when the reference clock source is external, this field is read/write. Otherwise this field is read-only and contains the H/W calculated clock period. When an external reference clock is use, valid values are 8ns (125MHz) through 15ns (66.67Mhz). **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set. **Note:** The Reference Clock Source and Reference Clock Period Override bits must be set prior to updating this field.	RO R/W	008h

5.2.83 PTP INTERRUPT STATUS REGISTER (PTP_INT_STS)

Index (In Decimal): 2.259 Size: 16 bits

This register contains the 1588 interrupt status bits.

Reading this register clears the interrupt sources. RO sources must be cleared at their lower level register.

If enabled in the PTP Interrupt Enable Register (PTP_INT_EN), these interrupt bits are cascaded into the 1588 Interrupt bit of the Interrupt Status Register. Status bits will still reflect the status of the interrupt source regardless of whether the source is enabled as an interrupt. The 1588 Interrupt Enable bit of the Interrupt Enable Register must be set in order for an actual system level interrupt to occur.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**PTP TX Timestamp FIFO Overflow Interrupt (PTP_TX_TS_OVRFL_INT)** This interrupt indicates that a packet was transmitted but its egress time and associated data stored could not be stored.	RC	0b
12	**PTP TX Timestamp Interrupt (PTP_TX_TS_INT)** This interrupt indicates that the count of egress timestamps stored is equal to or greater than the Timestamp Count Threshold. This bit is read only and clears once the count falls below the threshold.	RO	0b
11:10	**RESERVED**	RO	—
9	**PTP RX Timestamp FIFO Overflow Interrupt (PTP_RX_TS_OVRFL_INT)** This interrupt indicates that a packet was received but its ingress time and associated data stored could not be stored.	RC	0b
8	**PTP RX Timestamp Interrupt (PTP_RX_TS_INT)** This interrupt indicates that the count of ingress timestamps stored is equal to or greater than the Timestamp Count Threshold. This bit is read only and clears once the count falls below the threshold.	RO	0b

Bits	Description	Type	Default
7:3	**RESERVED**	RO	—
2	**PTP GPIO Capture Interrupt (PTP_GPIO_CAP_INT)** This interrupt indicates that a GPIO capture event occurred and its time stored.	RO	0b
1	**PTP Timer Interrupt B (PTP_TIMER_INT_B)** This interrupt indicates that the 1588 Local Time Counter equaled or passed the Local Time Event Channel B Local Time Target value. **Note:** This bit is also cleared by an active edge on a GPIO if enabled.	RC	0b
0	**PTP Timer Interrupt A (PTP_TIMER_INT_A)** This interrupt indicates that the 1588 Local Time Counter equaled or passed the Local Time Event Channel A Local Time Target value. **Note:** This bit is also cleared by an active edge on a GPIO if enabled.	RC	0b

5.2.84 PTP INTERRUPT ENABLE REGISTER (PTP_INT_EN)

Index (In Decimal): 2.260 Size: 16 bits

This register enables the corresponding bits in the PTP Interrupt Status Register (PTP_INT_STS).

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**PTP TX Timestamp FIFO Overflow Interrupt Enable (PTP_TX_TS_OVRFL_EN)**	R/W	0b
12	**PTP TX Timestamp Interrupt Enable (PTP_TX_TS_EN)**	R/W	0b
11:10	**RESERVED**	RO	—
9	**PTP RX Timestamp FIFO Overflow Interrupt Enable (PTP_RX_TS_OVRFL_EN)**	R/W	0b
8	**PTP RX Timestamp Interrupt Enable (PTP_RX_TS_EN)**	R/W	0b
7:3	**RESERVED**	RO	—
2	**PTP GPIO Capture Interrupt Enable (PTP_GPIO_CAP_EN)**	R/W	0b
1	**PTP Timer B Interrupt Enable (PTP_TIMER_EN_B)**	R/W	0b
0	**PTP Timer A Interrupt Enable (PTP_TIMER_EN_A)**	R/W	0b

5.2.85 PTP MODIFICATION ERROR REGISTER (PTP_MOD_ERR)

Index (In Decimal): 2.261 Size: 16 bits

This register contains packet modification error status.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**Reserved Field Overwrite Error** This bit is set if the 4 byte reserved field was not zero when it was written with the ingress timestamp during Ingress Time Insertion into Packet or during Ingress Correction Field Residence Time Adjustment method A. This bit is also set if the 1 byte reserved field was not zero when it was written with the ingress timestamp during Ingress Time Insertion into Packet.	RC	0b
5	**Pdelay_Resp Overwrite Error** This bit is set if the Pdelay_Resp Egress timestamp registers are overwritten (Pdelay_Resp Timestamp Valid was already set) by another egress Pdelay_Resp message before the registers were used by the egress Pdelay_Resp_Follow_Up message. **Note:** If egress Pdelay_Resp_Follow_Up message offloading is not enable, this bit can be safely ignored.	RC	0b
4	**Pdelay_Req Overwrite Error** This bit is set if the Pdelay_Req Ingress timestamp and correction registers are overwritten (Pdelay_Req Timestamp Valid was already set) by another ingress Pdelay_Req message before the registers were used by the egress Pdelay_Resp or Pdelay_Resp_Follow_Up message. **Note:** If egress Pdelay_Resp or Pdelay_Resp_Follow_Up message offloading is not enable, this bit can be safely ignored.	RC	0b
3	**Sync Overwrite Error** This bit is set if the Sync Egress timestamp registers are overwritten (Sync Timestamp Valid was already set) by another egress Sync message before the registers were used by the egress Follow_Up message. **Note:** If egress Follow_Up message offloading is not enable, this bit can be safely ignored.	RC	0b
2	**Pdelay_Resp_Follow_Up Egress Error** This bit is set if the Pdelay_Req Ingress timestamp and correction field registers and / or the Pdelay_Resp Egress timestamp registers are not valid when a Pdelay_Resp_Follow_Up message is transmitted with offloading enable.	RC	0b
1	**Pdelay_Resp Egress Error** This bit is set if the Pdelay_Req Ingress timestamp and correction field registers are not valid when a Pdelay_Resp message is transmitted with offloading enable.	RC	0b
0	**Follow_Up Egress Error** This bit is set if the Sync Egress timestamp registers are not valid when a Follow_Up message is transmitted with offloading enable.	RC	0b

5.2.86 PTP LTC SET SECONDS HIGH REGISTER (PTP_LTC_SET_SEC_HI)

Index (In Decimal): 2.262 Size: 16 bits

This register contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[47:32])** This field contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.87 PTP LTC SET SECONDS MID REGISTER (PTP_LTC_SET_SEC_MID)

Index (In Decimal): 2.263 Size: 16 bits

This register contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[31:16])** This field contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.88 PTP LTC SET SECONDS LOW REGISTER (PTP_LTC_SET_SEC_LO)

Index (In Decimal): 2.264 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.89 PTP LTC SET NANOSECONDS HIGH REGISTER (PTP_LTC_SET_NS_HI)

Index (In Decimal): 2.265 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.90 PTP LTC SET NANOSECONDS LOW REGISTER (PTP_LTC_SET_NS_LO)

Index (In Decimal): 2.266 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.91 PTP LTC SET SUB-NANOSECONDS HIGH REGISTER (PTP_LTC_SET_SUBNS_HI)

Index (In Decimal): 2.267 Size: 16 bits

This register contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[31:16])** This field contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.92 PTP LTC SET SUB-NANOSECONDS LOW REGISTER (PTP_LTC_SET_SUBNS_LO)

Index (In Decimal): 2.268 Size: 16 bits

This register contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to directly change the 1588 Local Time Counter when the LTC Load (PTP_LTC_LOAD) bit is set.

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[15:0])** This field contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	R/W	0000h

5.2.93 PTP LTC RATE ADJUSTMENT HIGH REGISTER (PTP_LTC_RATE_ADJ_HI)

Index (In Decimal): 2.269 Size: 16 bits

This register along with the PTP LTC Rate Adjustment Low Register (PTP_LTC_RATE_ADJ_LO) is used to adjust the rate of the 1588 Local Time Counter. This register contains the upper 14 bits of the rate adjustment value and the adjustment direction bit.

Bits	Description	Type	Default
15	**LTC Rate Adjustment Direction (PTP_LTC_RATE_ADJ_DIR)** This field specifies if the 1588 Rate Adjustment causes the 1588 Local Time Counter to be faster or slower than the reference clock. 0 = slower (1588 Local Time Counter increments by 1 ns less) 1 = faster (1588 Local Time Counter increments by 1 ns more)	R/W	0b
14	**RESERVED**	RO	—
13:0	**LTC Rate Adjustment Value (PTP_LTC_RATE_ADJ_VALUE[29:16])** This field indicates an adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32}ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

Note: Both this register and the PTP LTC Rate Adjustment Low Register (PTP_LTC_RATE_ADJ_LO) must be written for either to be affected.

5.2.94 PTP LTC RATE ADJUSTMENT LOW REGISTER (PTP_LTC_RATE_ADJ_LO)

Index (In Decimal): 2.270 Size: 16 bits

This register contains the lower 16 bits of the rate adjustment value.

Bits	Description	Type	Default
15:0	**LTC Rate Adjustment Value (PTP_LTC_RATE_ADJ_VALUE[15:0])** This field indicates an adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32}ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

Note: Both this register and the PTP LTC Rate Adjustment High Register (PTP_LTC_RATE_ADJ_HI) must be written for either to be affected.

5.2.95 PTP LTC TEMPORARY RATE ADJUSTMENT HIGH REGISTER (PTP_LTC_TEMP_RATE_ADJ_HI)

Index (In Decimal): 2.271 Size: 16 bits

This register along with the PTP LTC Temporary Rate Adjustment Low Register (PTP_LTC_TEMP_RATE_ADJ_LO) is used to adjust the rate of the 1588 Local Time Counter. Every reference clock period, the 1588 Local Time Counter is normally incremented by the reference clock period value. This register is used to occasionally change that increment by one ns additional or one less. This register contains the upper 14 bits of the temporary rate adjustment value and the adjustment direction bit.

Bits	Description	Type	Default
15	**LTC Temporary Rate Adjustment Direction (PTP_LTC_TEMP_RATE_ADJ_DIR)** This field specifies if the 1588 Temporary Rate Adjustment causes the 1588 Local Time Counter to be faster or slower than the reference clock. 0 = slower (1588 Local Time Counter increments by 1 ns less) 1 = faster (1588 Local Time Counter increments by 1 ns more)	R/W	0b
14	**RESERVED**	RO	—
13:0	**LTC Temporary Rate Adjustment Value (PTP_LTC_TEMP_RATE_ADJ_VALUE[29:16])** This field indicates a temporary adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32}ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

5.2.96 PTP LTC TEMPORARY RATE ADJUSTMENT LOW REGISTER (PTP_LTC_TEMP_RATE_ADJ_LO)

Index (In Decimal): 2.272 Size: 16 bits

This register contains the lower 16 bits of the temporary rate adjustment value.

Bits	Description	Type	Default
15:0	**LTC Temporary Rate Adjustment Value (PTP_LTC_TEMP_RATE_ADJ_VALUE[15:0])** This field indicates a temporary adjustment to the reference clock period of the 1588 Local Time Counter in units of 2^{-32}ns. On each reference clock cycle, this value is added to the 32-bit sub-nanoseconds portion of the 1588 Local Time Counter. When the sub-nanoseconds portion rolls over past zero, the 1588 Local Time Counter will be adjusted by 1 ns.	R/W	0000h

5.2.97 PTP LTC TEMPORARY RATE DURATION HIGH REGISTER (PTP_LTC_TEMP_RATE_DURATION_HI)

Index (In Decimal): 2.273 Size: 16 bits

This register along with the PTP LTC Temporary Rate Duration Low Register (PTP_LTC_TEMP_RATE_DURATION_LO) specifies the active duration of the temporary rate adjustment. This register contains the upper 16 bits of the temporary rate duration value.

Bits	Description	Type	Default
15:0	**LTC Temporary Rate Duration (PTP_LTC_TEMP_RATE_DURATION[31:16])** This field specifies the duration of the temporary rate adjustment in reference clock cycles.	R/W	0000h

5.2.98 PTP LTC TEMPORARY RATE DURATION LOW REGISTER (PTP_LTC_TEMP_RATE_DURATION_LO)

Index (In Decimal): 2.274 Size: 16 bits

This register contains the lower 16 bits of the temporary rate duration value.

Bits	Description	Type	Default
15:0	**LTC Temporary Rate Duration (PTP_LTC_TEMP_RATE_DURATION[15:0])** This field specifies the duration of the temporary rate adjustment in reference clock cycles.	R/W	0000h

5.2.99 PTP LTC STEP ADJUSTMENT HIGH REGISTER (PTP_LTC_STEP_ADJ_HI)

Index (In Decimal): 2.275 Size: 16 bits

This register along with the PTP LTC Step Adjustment Low Register (PTP_LTC_STEP_ADJ_LO) is used to perform a one-time adjustment to either the seconds portion or the nanoseconds portion of the 1588 Local Time Counter. The amount and direction can be specified. This register contains the upper 14 bits of the step adjustment value and the step adjustment direction bit.

Bits	Description	Type	Default
15	**LTC Step Adjustment Direction (PTP_LTC_STEP_ADJ_DIR)** This field specifies if the LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE[29:16]) is added to or subtracted from the 1588 Local Time Counter. 0 = subtracted 1 = added **Note:** Only addition is supported for the nanoseconds portion of the 1588 Local Time Counter	R/W	0b
14	**RESERVED**	RO	—
13:0	**LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE[29:16])** When the nanoseconds portion of the 1588 Local Time Counter is being adjusted, this field specifies the amount to add. This is in lieu of the normal reference clock period increment. When the seconds portion of the 1588 Local Time Counter is being adjusted, this field is not used.	R/W	0000h

5.2.100 PTP LTC STEP ADJUSTMENT LOW REGISTER (PTP_LTC_STEP_ADJ_LO)

Index (In Decimal): 2.276 Size: 16 bits

This register contains the lower 16 bits of the step adjustment value.

Bits	Description	Type	Default
15:0	**LTC Step Adjustment Value (PTP_LTC_STEP_ADJ_VALUE[15:0])** When the nanoseconds portion of the 1588 Local Time Counter is being adjusted, this field specifies the amount to add. This is in lieu of the normal reference clock period increment. When the seconds portion of the 1588 Local Time Counter is being adjusted, the lower 4 bits of this field specify the amount to add to or subtract.	R/W	0000h

5.2.101 PTP LTC EXTERNAL ADJUSTMENT CONFIGURATION REGISTER (PTP_LTC_EXT_ADJ_CFG)

Index (In Decimal): 2.277 Size: 16 bits

This read/write register is used to configure GPIO control of the 1588 Local Time Counter adjustments.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:8	**LTC External Adjustment GPIO Select** These bits determine which GPIO is used for 1588 Local Time Counter adjustments	R/W	0h
7	**RESERVED**	RO	—
6	**LTC Adjustment Select (PTP_LTC_ADJ_SEL)** This field controls whether LTC adjustments are performed by software or GPIO. 0 = LTC is software-controlled using the bits in PTP_CMD_CTL 1 = LTC Temporary Rate Adjust is GPIO-controlled using the bits in this register	R/W	0b
5	**RESERVED**	RO	—
4	**LTC External Adjust Mode (PTP_LTC_EXTERNAL_MODE)** This bit configures whether only the first rising edge on the selected GPIO causes an adjustment (one-shot) or every rising edge on the selected GPIO causes adjustments (static). 0 = one-shot adjustment. To initiate a one-shot adjustment, software must first clear this bit to 0, then set the appropriate adjustment bit (one of PTP_LTC_EXT_ADJ_CFG bits 3:0). Hardware will self-clear the adjustment bit following the adjustment. 1= static (repeating) adjustments. To initiate static (repeating) adjustments, software must first set this bit to 1, then set the appropriate adjustment bit (one of PTP_LTC_EXT_ADJ_CFG bits 3:0). To terminate static (repeating) adjustments, software must clear this bit to 0. Hardware will self-clear the adjustment bit following the final adjustment.	R/W	0b

Bits	Description	Type	Default
3	**LTC Temporary Rate Adjustment External Enable** Enables a rising edge on the selected GPIO to cause a temporary rate adjustment to the 1588 Local Time Counter as specified by the PTP_LTC_TEMP_RATE_ADJ_HI/LO and PTP_LTC_TEMP_RATE_DURATION_HI/LO registers. External adjustment is only valid when LTC Adjustment Select (PTP_LTC_ADJ_SEL) = 1. One-shot or static/repeating adjustment is controlled by LTC External Adjust Mode (PTP_LTC_EXTERNAL_MODE). One-shot adjustment (PTP_LTC_EXTERNAL_MODE=0), Software sets the bit to 1, hardware clears the bit after one adjustment is completed. Software may also clear the bit to 0. If cleared by software before an adjustment has started, the adjustment will not start. If cleared by software during an adjustment, the adjustment will complete. Static (repeating) adjustment (PTP_LTC_EXTERNAL_MODE=1). Software sets the bit to 1, adjustments are made by hardware every time a rising edge is detected on the GPIO. Software may not clear the bit to 0, When software terminates repeating adjustments, hardware will clear the bit to 0. To terminate repeating adjustments, software must clear PTP_LTC_EXTERNAL_MODE to 0.	R/W/SC	0b
2	**LTC Step Nanoseconds External Enable** Enables a rising edge on the selected GPIO to cause a step adjustment to the 1588 Local Time Counter nanoseconds as specified by the PTP_LTC_STEP_ADJ_HI/LO registers. External adjustment is only valid when LTC Adjustment Select (PTP_LTC_ADJ_SEL) = 1. One-shot or static/repeating adjustment is controlled by LTC External Adjust Mode (PTP_LTC_EXTERNAL_MODE). One-shot adjustment (PTP_LTC_EXTERNAL_MODE=0), Software sets the bit to 1, hardware clears the bit after one adjustment is completed. Software may also clear the bit to 0. If cleared by software before an adjustment has started, the adjustment will not start. If cleared by software during an adjustment, the adjustment will complete. Static (repeating) adjustment (PTP_LTC_EXTERNAL_MODE=1). Software sets the bit to 1, adjustments are made by hardware every time a rising edge is detected on the GPIO. Software may not clear the bit to 0, When software terminates repeating adjustments, hardware will clear the bit to 0. To terminate repeating adjustments, software must clear PTP_LTC_EXTERNAL_MODE to 0.	R/W/SC	0b

Bits	Description	Type	Default
1	**LTC Step Seconds External Enable** Enables a rising edge on the selected GPIO to cause a step adjustment to the 1588 Local Time Counter seconds as specified by the PTP_LTC_STEP_-ADJ_HI/LO registers. External adjustment is only valid when LTC Adjustment Select (PTP_LTC_-ADJ_SEL) = 1. One-shot or static/repeating adjustment is controlled by LTC External Adjust Mode (PTP_LTC_EXTERNAL_MODE). One-shot adjustment (PTP_LTC_EXTERNAL_MODE=0), Software sets the bit to 1, hardware clears the bit after one adjustment is completed. Software may also clear the bit to 0. If cleared by software before an adjustment has started, the adjustment will not start. If cleared by software during an adjustment, the adjustment will complete. Static (repeating) adjustment (PTP_LTC_EXTERNAL_MODE=1). Software sets the bit to 1, adjustments are made by hardware every time a rising edge is detected on the GPIO. Software may not clear the bit to 0, When software terminates repeating adjustments, hardware will clear the bit to 0. To terminate repeating adjustments, software must clear PTP_LTC_EXTERNAL_-MODE to 0.	R/W/SC	0b
0	**LTC Load External Enable** Enables a rising edge on the selected GPIO to cause the 1588 Local Time Counter to be loaded from the PTP_LTC_SET_SEC_HI/LO, PTP_LTC_SET_NS_HI/LO and PTP_LTC_SET_SUBNS_HI/LO registers. External adjustment is only valid when LTC Adjustment Select (PTP_LTC_-ADJ_SEL) = 1. One-shot or static/repeating adjustment is controlled by LTC External Adjust Mode (PTP_LTC_EXTERNAL_MODE). One-shot LTC Load (PTP_LTC_EXTERNAL_MODE=0), Software sets the bit to 1, hardware clears the bit after one LTC Load is completed. Software may also clear the bit to 0. If cleared by software before an LTC Load has started, the LTC Load will not start. If cleared by software during an LTC Load, the LTC Load will complete. Static (repeating) LTC Load (PTP_LTC_EXTERNAL_MODE=1). Software sets the bit to 1, LTC Load is performed by hardware every time a rising edge is detected on the GPIO. Software may not clear the bit to 0, When software terminates repeating LTC Loads, hardware will clear the bit to 0. To terminate repeating LTC Loads, software must clear PTP_LTC_EXTERNAL_MODE to 0.	R/W/SC	0b

5.2.102 PTP LTC TARGET X SECONDS HIGH REGISTER (PTP_LTC_TARGET_SEC_HI_X)

Index (In Decimal): Channel A: 2.278 Size: 16 bits
Channel B: 2.288

This read/write register combined with the PTP LTC Target x Seconds Low Register (PTP_LTC_TARGET_SEC_LO_x) and the PTP LTC Target x Nanoseconds High/Lo Registers (PTP_LTC_TARGET_NS_HI/LO_x) form the 1588 Local Time Target value. This register contains the upper 16 bits of the target seconds.

Bits	Description	Type	Default
15:0	**LTC Target Seconds (LTC_TARGET_SEC[31:16])** This field contains the seconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

Note: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

Note: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

Note: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

5.2.103 PTP LTC TARGET X SECONDS LOW REGISTER (PTP_LTC_TARGET_SEC_LO_X)

Index (In Decimal): Channel A: 2.279 Size: 16 bits
Channel B: 2.289

This register contains the lower 16 bits of the target seconds.

Bits	Description	Type	Default
15:0	**LTC Target Seconds (LTC_TARGET_SEC[15:0])** This field contains the seconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

Note: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

Note: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

Note: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

5.2.104 PTP LTC TARGET X NANOSECONDS HIGH REGISTER (PTP_LTC_TARGET_NS_HI_X)

Index (In Decimal): Channel A: 2.280 Channel B: 2.290 Size: 16 bits

This read/write register combined with the PTP LTC Target x Seconds Low/High Registers (PTP_LTC_TARGET_SEC_HI/LO_x) and the PTP LTC Target x Nanoseconds Low Register (PTP_LTC_TARGET_NS_LO_x) form the 1588 Local Time Target value. This register contains the upper 14 bits of the target nanoseconds.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Target Nanoseconds (LTC_TARGET_NS[29:16])** This field contains the nanoseconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

Note: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

Note: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

Note: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

5.2.105 PTP LTC TARGET X NANOSECONDS LOW REGISTER (PTP_LTC_TARGET_NS_LO_X)

Index (In Decimal): Channel A: 2.281 Channel B: 2.291 Size: 16 bits

This register contains the lower 16 bits of the target nanoseconds.

Bits	Description	Type	Default
15:0	**LTC Target Nanoseconds (LTC_TARGET_NS[15:0])** This field contains the nanoseconds portion of the 1588 Local Time Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_SEC_LO/HI_x and PTP_LTC_TARGET_NS_HI/LO_x) must be written for any to be affected.

Note: The value read is the saved value of the 1588 Local Time Target when the LTC Target Read (PTP_LTC_TARGET_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set or the last value written.

Note: When the LTC Target Read (PTP_LTC_TARGET_READ) bit is set, the previous value written to this register is overwritten. Normally, a read command would not be requested in between writing this register and the other three.

Note: Writes to this register will overwrite the previous result of a LTC Target Read command. Normally, a write would not be done in between issuing LTC Target Read command and reading this register.

5.2.106 PTP LTC TARGET X RELOAD / ADD SECONDS HIGH REGISTER (PTP_LTC_TARGET_RELOAD_SEC_HI_X)

Index (In Decimal): Channel A: 2.282 Size: 16 bits
Channel B: 2.292

This read/write register combined with the PTP LTC Target x Reload / Add Seconds Low Register (PTP_LTC_TARGET_RELOAD_SEC_LO_x) and the PTP LTC Target x Reload / Add NanoSeconds High/Low Registers (PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) form the 1588 Local Time Target Reload value. This register contains the upper 16 bits of the target reload / add seconds.

Bits	Description	Type	Default
15:0	**LTC Target Reload Seconds (LTC_TARGET_RELOAD_SEC[31:16])** This field contains the seconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

5.2.107 PTP LTC TARGET X RELOAD / ADD SECONDS LOW REGISTER (PTP_LTC_TARGET_RELOAD_SEC_LO_X)

Index (In Decimal): Channel A: 2.283 Size: 16 bits
Channel B: 2.293

This register contains the lower 16 bits of the target reload / add seconds.

Bits	Description	Type	Default
15:0	**LTC Target Reload Seconds (LTC_TARGET_RELOAD_SEC[15:0])** This field contains the seconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

5.2.108 PTP LTC TARGET X RELOAD / ADD NANOSECONDS HIGH REGISTER (PTP_LTC_TARGET_RELOAD_NS_HI_X)

Index (In Decimal): Channel A: 2.284 Size: 16 bits
Channel B: 2.294

This read/write register combined with the PTP LTC Target x Reload / Add Seconds High/Low Registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x) and the PTP LTC Target x Reload / Add Nanoseconds Low Register (PTP_LTC_TARGET_RELOAD_NS_LO_x) form the 1588 Local Time Target Reload value. This register contains the upper 14 bits of the target reload / add nanoseconds.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Target Reload Nanoseconds (LTC_TARGET_RELOAD_NS[29:16])** This field contains the nanoseconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

5.2.109 PTP LTC TARGET X RELOAD / ADD NANOSECONDS LOW REGISTER (PTP_LTC_TARGET_RELOAD_NS_LO_X)

Index (In Decimal): Channel A: 2.285 Size: 16 bits
Channel B: 2.295

This register contains the lower 16 bits of the target reload / add nanoseconds.

Bits	Description	Type	Default
15:0	**LTC Target Reload Nanoseconds (LTC_TARGET_RELOAD_NS[15:0])** This field contains the nanoseconds portion of the 1588 Local Time Target Reload value that is reloaded to the 1588 Local Time Target Compare value.	R/W	0000h

Note: All four registers (PTP_LTC_TARGET_RELOAD_SEC_HI/LO_x and PTP_LTC_TARGET_RELOAD_NS_HI/LO_x) must be written for any to be affected.

5.2.110 PTP LTC TARGET X ACTUAL NANOSECONDS HIGH REGISTER (PTP_LTC_TARGET_ACT_NS_HI_X)

Index (In Decimal): Channel A: 2.286 Size: 16 bits
Channel B: 2.296

This read only register combined and the PTP LTC Target x Actual Nanoseconds Low Register (PTP_LTC_TARGET_ACT_NS_LO_x) contain the 1588 Local Time Counter nanoseconds value when the Local Time event occurs. This register contains the upper 14 bits of the LTC target actual nanoseconds.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Target Actual Nanoseconds (LTC_TARGET_ACT_NS[29:16])** This field contains the nanoseconds portion of the 1588 Local Time Target Compare value.	RO	0000h

5.2.111 PTP LTC TARGET X ACTUAL NANOSECONDS LOW REGISTER (PTP_LTC_TARGET_ACT_NS_LO_X)

Index (In Decimal): Channel A: 2.287 Size: 16 bits
Channel B: 2.297

This register contains the lower 16 bits of the target actual nanoseconds.

Bits	Description	Type	Default
15:0	**LTC Target Actual Nanoseconds (LTC_TARGET_ACT_NS[15:0])** This field contains the nanoseconds portion of the 1588 Local Time Target Compare value.	RO	0000h

5.2.112 PTP RX USER MAC ADDRESS HIGH REGISTER (PTP_RX_USER_MAC_HI)

Index (In Decimal): 2.298 Size: 16 bits

This read/write register combined with the PTP RX User MAC Address Mid/Low Registers (PTP_RX_USER_MAC_MID/LO) forms the 48-bit user defined MAC address. This register contains the upper 16 bits of the user MAC address.

The User MAC address can be enabled for each protocol via their respective User Defined MAC Address Enable bits (L2_USER_MAC_EN, IPV4_USER_MAC_EN or IPV6_USER_MAC_EN) in the corresponding Address Enable registers (PTP_RX_PARSE_L2_ADDR_EN, PTP_RX_PARSE_IP_ADDR_EN).

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[47:32])** This field contains the high 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.113 PTP RX USER MAC ADDRESS MID REGISTER (PTP_RX_USER_MAC_MID)

Index (In Decimal): 2.299 Size: 16 bits

This register contains the middle 16 bits of the user MAC address.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[31:16]** This field contains the middle 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.114 PTP RX USER MAC ADDRESS LOW REGISTER (PTP_RX_USER_MAC_LO)

Index (In Decimal): 2.300 Size: 16 bits

This register contains the lower 16 bits of the user MAC address.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[15:0]** This field contains the low 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.115 PTP RX USER IP ADDRESS REGISTERS (PTP_RX_USER_IP_ADDRx)

Index (In Decimal): x=0: 2.301
x=1: 2.302
x=2: 2.303
x=3: 2.304
x=4: 2.305
x=5: 2.306
x=6: 2.307
x=7: 2.308

Size: 16 bits

These read/write registers provide the 32-bit (IPv4) or 128-bit (IPv6) user defined IP address. Each register contains 16 bits of the address.

The User IP address can be enabled for the IPv4 or IPv6 protocols via their respective User Defined IP Address Enable bits in the PTP RX Parsing IP Format Address Enable Register (PTP_RX_PARSE_IP_ADDR_EN).

Register	Bits	Description	Type	Default
x=7 x=6	15:0	**IP Address[127:112]** **IP Address[111:96]** These fields contain the upper 32 bits of the 128 bit user defined IPv6 address and the entire 32 bits of the user defined IPv4 address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h 0000h
x=5 x=4 x=3 x=2 x=1 x=0	15:0	**IP Address[95:80]** **IP Address[79:64]** **IP Address[63:48]** **IP Address[47:32]** **IP Address[31:16]** **IP Address[15:0]** These fields contain the lower 96 bits of the 128 bit user defined IPv6 address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h 0000h 0000h 0000h 0000h 0000h

5.2.116 PTP RX USER IP MASK REGISTERS (PTP_RX_USER_IP_MASKx)

Index (In Decimal): x=0: 2.309 Size: 16 bits
x=1: 2.310
x=2: 2.311
x=3: 2.312
x=4: 2.313
x=5: 2.314
x=6: 2.315
x=7: 2.316

These read/write registers provide a 32-bit (IPv4) or 128-bit (IPv6) mask for the user defined IP address. Each register contains 16 bits of the mask.

Register	Bits	Description	Type	Default
x=7 x=6	15:0	**IP Mask[127:112]** **IP Mask[111:96]** These fields contain the upper 32 bits of the 128 bit user defined IPv6 mask and the entire 32 bits of the user defined IPv4 mask used for PTP packet detection. 0 : bit is ignored (considered a match) 1 : bit is compared **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	FFFFh FFFFh
x=5 x=4 x=3 x=2 x=1 x=0	15:0	**IP Mask[95:80]** **IP Mask[79:64]** **IP Mask[63:48]** **IP Mask[47:32]** **IP Mask[31:16]** **IP Mask[15:0]** These fields contain the lower 96 bits of the 128 bit user defined IPv6 mask used for PTP packet detection. 0 : bit is ignored (considered a match) 1 : bit is compared **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	FFFFh FFFFh FFFFh FFFFh FFFFh FFFFh

5.2.117 VLAN ETHERNET TYPE ID REGISTER (VLAN_TYPE_ID)

Index (In Decimal): 2.317 Size: 16 bits

This read/write register specifies an alternate VLAN type ID.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:0	**VLAN Ethernet Type** **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	8100h

5.2.118 VLAN 1 TYPE / ID REGISTER (VLAN1_TYPE_ID)

Index (In Decimal): 2.318 Size: 16 bits

This read/write register configures the Ethernet type and VID for VLAN 1.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:12	**VLAN Ethernet Type Select[1:0]** When VLAN checking enabled, this field is used to select the Ethernet Type. 11 : The fixed value of 0x88a8 is used 10 : The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used 01 : The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used 00 : The fixed value of 0x8100 is used **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b
11:0	**VLAN ID Value** This field contains the VLAN ID. Each bit may be masked using the VLAN ID Mask field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.119 VLAN 1 ID MASK REGISTER (VLAN1_ID_MASK)

Index (In Decimal): 2.319 Size: 16 bits

This read/write register configures the VID mask for VLAN 1.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Mask** This field contains the VLAN ID Mask. 0 : bit is ignored (considered a match) 1 : bit is compared **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.120 VLAN 1 VID RANGE UPPER REGISTER (VLAN1_VID_RANGE_UP)

Index (In Decimal): 2.320 Size: 16 bits

This read/write register configures VID range checking for VLAN 1.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**VLAN ID Range Enable** When set, this field enables VLAN ID range checking. When cleared, the VLAN ID Value is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
11:0	**VLAN ID Upper Range** This field contains the VLAN ID range upper limit. This field is used along with the VLAN ID range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.121 VLAN 1 VID RANGE LOWER REGISTER (VLAN1_VID_RANGE_LO)

Index (In Decimal): 2.321 Size: 16 bits

This read/write register configures VID range checking for VLAN 1.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Lower Range** This field contains the VLAN ID range lower limit. This field is used along with the VLAN ID range upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.122 VLAN 2 TYPE / ID REGISTER (VLAN2_TYPE_ID)

Index (In Decimal): 2.322 Size: 16 bits

This read/write register configures the Ethernet type and VID for VLAN 2.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:12	**VLAN Ethernet Type Select[1:0]** When VLAN checking enabled, this field is used to select the Ethernet Type. 11 : The fixed value of 0x88a8 is used 10 : The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used 01 : The value in the VLAN Ethernet Type ID Register (VLAN_TYPE_ID) is used 00 : The fixed value of 0x8100 is used **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b
11:0	**VLAN ID Value** This field contains the VLAN ID. Each bit may be masked using the VLAN ID Mask field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.123 VLAN 2 ID MASK REGISTER (VLAN2_ID_MASK)

Index (In Decimal): 2.323 Size: 16 bits

This read/write register configures the VID mask for VLAN 2.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Mask** This field contains the VLAN ID Mask. 0 : bit is ignored (considered a match) 1 : bit is compared **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.124 VLAN 2 VID RANGE UPPER REGISTER (VLAN2_VID_RANGE_UP)

Index (In Decimal): 2.324 Size: 16 bits

This read/write register configures VID range checking for VLAN 2.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:13	**RESERVED**	RO	—
12	**VLAN ID Range Enable** When set, this field enables VLAN ID range checking. When cleared, the VLAN ID Value is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
11:0	**VLAN ID Upper Range** This field contains the VLAN ID range upper limit. This field is used along with the VLAN ID range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.125 VLAN 2 VID RANGE LOWER REGISTER (VLAN2_VID_RANGE_LO)

Index (In Decimal): 2.325 Size: 16 bits

This read/write register configures VID range checking for VLAN 2.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**VLAN ID Lower Range** This field contains the VLAN ID range lower limit. This field is used along with the VLAN ID range upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.126 LLC ETHERNET TYPE ID REGISTER (LLC_TYPE_ID)

Index (In Decimal): 2.326 Size: 16 bits

This read/write register specifies the EtherType for LCC.

This register is common for the ingress and egress directions.

Bits	Description	Type	Default
15:0	**LLC Ethernet Type** **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	05DCh

5.2.127 PTP GPIO SELECT REGISTER (PTP_GPIO_SEL)

Index (In Decimal): 2.327 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	RO	—
10:8	**GPIO Select (GPIO_SEL[2:0])** This field specifies which GPIO the various GPIO x registers will access. **Note:** Although there are more GPIO inputs, there are eight sets of rising edge and eight sets of falling edge capture registers (x=0 through 7).	R/W	000b
7:0	**RESERVED**	RO	-

5.2.128 PTP RX LATENCY 10Mbps REGISTER (PTP_RX_LATENCY_10)

Index (In Decimal): 2.328 Size: 16 bits

Bits	Description	Type	Default
15:0	**RX Latency 10Mbps (RX_LATENCY_10[15:0])** This field specifies the ingress delay in nanoseconds between the network medium while operating at 10Mbps and the PTP timestamp point. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.129 PTP TX LATENCY 10Mbps REGISTER (PTP_TX_LATENCY_10)

Index (In Decimal): 2.329 Size: 16 bits

Bits	Description	Type	Default
15:0	**TX Latency 10Mbps (TX_LATENCY_10[15:0])** This field specifies the egress delay in nanoseconds between the PTP time-stamp point and the network medium while operating at 10Mbps. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.130 PTP RX LATENCY 100Mbps REGISTER (PTP_RX_LATENCY_100)

Index (In Decimal): 2.330 Size: 16 bits

Bits	Description	Type	Default
15:0	**RX Latency 100Mbps (RX_LATENCY_100[15:0])** This field specifies the ingress delay in nanoseconds between the network medium while operating at 100Mbps and the PTP timestamp point. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.131 PTP TX LATENCY 100Mbps REGISTER (PTP_TX_LATENCY_100)

Index (In Decimal): 2.331 Size: 16 bits

Bits	Description	Type	Default
15:0	**TX Latency 100Mbps (TX_LATENCY_100[15:0])** This field specifies the egress delay in nanoseconds between the PTP timestamp point and the network medium while operating at 100Mbps. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.132 PTP RX LATENCY 1000Mbps REGISTER (PTP_RX_LATENCY_1000)

Index (In Decimal): 2.332 Size: 16 bits

Bits	Description	Type	Default
15:0	**RX Latency 1000Mbps (RX_LATENCY_1000[15:0])** This field specifies the ingress delay in nanoseconds between the network medium while operating at 1000Mbps and the PTP timestamp point. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.133 PTP TX LATENCY 1000Mbps REGISTER (PTP_TX_LATENCY_1000)

Index (In Decimal): 2.333 Size: 16 bits

Bits	Description	Type	Default
15:0	**TX Latency 1000Mbps (TX_LATENCY_1000[15:0])** This field specifies the egress delay in nanoseconds between the PTP timestamp point and the network medium while operating at 1000Mbps. The setting is used to adjust the internally captured 1588 Local Time Counter value such that the resultant timestamp more accurately corresponds to the start of the frame's first symbol after the SFD on the network medium. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.134 PTP ASYMMETRY DELAY HIGH REGISTER (PTP_ASYM_DLY_HI)

Index (In Decimal): 2.334 Size: 16 bits

This register contains the upper 16 bits of the delay asymmetry.

When combined with the lower 16 bits, this forms a signed number.
The sub-nanoseconds portion of the delay asymmetry is fixed at 0.

Bits	Description	Type	Default
15:0	**Port Delay Asymmetry (DELAY_ASYM[31:16])** This field specifies the previously known delay asymmetry in nanoseconds. This is a signed 2's complement number. Positive values occur when the master-to-slave or responder-to-requestor propagation time is longer than the slave-to-master or requestor-to-responder propagation time. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.135 PTP ASYMMETRY DELAY LOW REGISTER (PTP_ASYM_DLY_LO)

Index (In Decimal): 2.335 Size: 16 bits

This register contains the lower 16 bits of the delay asymmetry.

Bits	Description	Type	Default
15:0	**Port Delay Asymmetry (DELAY_ASYM[15:0])** This field specifies the previously known delay asymmetry in nanoseconds. This is a signed 2's complement number. Positive values occur when the master-to-slave or responder-to-requestor propagation time is longer than the slave-to-master or requestor-to-responder propagation time. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL)is set.	R/W	0000h

5.2.136 PTP PEER DELAY HIGH REGISTER (PTP_PEERDLY_HI)

Index (In Decimal): 2.336 Size: 16 bits

This register contains the upper 16 bits of the RX peer delay.

When combined with the lower 16 bits, this forms an unsigned number and is either zero or a positive value. The sub-nanoseconds portion of the RX peer delay is fixed at 0.

Bits	Description	Type	Default
15:0	**RX Peer Delay (RX_PEER_DELAY[31:16])** This field specifies the measured peer delay in nanoseconds used during peer-to-peer mode.	R/W	0000h

5.2.137 PTP PEER DELAY LOW REGISTER (PTP_PEERDLY_LO)

Index (In Decimal): 2.337 Size: 16 bits

This register contains the lower 16 bits of the RX peer delay.

Bits	Description	Type	Default
15:0	**RX Peer Delay (RX_PEER_DELAY[15:0])** This field specifies the measured peer delay in nanoseconds used during peer-to-peer mode.	R/W	0000h

5.2.138 PTP CAPTURE INFORMATION REGISTER (PTP_CAP_INFO)

Index (In Decimal): 2.338 Size: 16 bits

This read only register provides information about transmit capture buffers.

Bits	Description	Type	Default
15:12	**PTP TX Timestamp Count Threshold (PTP_TX_TS_CNT_THRES[3:0])** An interrupt is generated whenever the TX Timestamp Count equals or exceeds this field.	R/W	1h
11:8	**PTP TX Timestamp Count (PTP_TX_TS_CNT[3:0])** This field indicates how many transmit timestamps are available to be read. It is incremented when a PTP packet is transmitted and decremented when the PTP_TX_MSG_HEADER2 register is read.	RO	0h
7:4	**PTP RX Timestamp Count Threshold (PTP_RX_TS_CNT_THRES[3:0])** An interrupt is generated whenever the RX Timestamp Count equals or exceeds this field.	R/W	1h
3:0	**PTP RX Timestamp Count (PTP_RX_TS_CNT[3:0])** This field indicates how many receive timestamps are available to be read. It is incremented when a PTP packet is received and decremented when the PTP_RX_MSG_HEADER2 register is read.	RO	0h

5.2.139 PTP TX USER MAC ADDRESS HIGH REGISTER (PTP_TX_USER_MAC_HI)

Index (In Decimal): 2.339 Size: 16 bits

This read/write register combined with the PTP TX User MAC Address Mid/Low Registers (PTP_TX_USER_MAC_MID/LO) forms the 48-bit user defined MAC address. This register contains the upper 16 bits of the user MAC address.

The User MAC address can be enabled for each protocol via their respective User Defined MAC Address Enable bits (L2_USER_MAC_EN, IPV4_USER_MAC_EN or IPV6_USER_MAC_EN) in the corresponding Address Enable registers (PTP_TX_PARSE_L2_ADDR_EN, PTP_TX_PARSE_IP_ADDR_EN).

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[47:32])** This field contains the high 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.140 PTP TX USER MAC ADDRESS MID REGISTER (PTP_TX_USER_MAC_MID)

Index (In Decimal): 2.340 Size: 16 bits

This register contains the middle 16 bits of the user MAC address.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[31:16]** This field contains the middle 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.141 PTP TX USER MAC ADDRESS LOW REGISTER (PTP_TX_USER_MAC_LO)

Index (In Decimal): 2.341 Size: 16 bits

This register contains the lower 16 bits of the user MAC address.

Bits	Description	Type	Default
15:0	**User MAC Address (USER_MAC[15:0]** This field contains the low 16 bits of the user defined MAC address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.142 PTP TX USER IP ADDRESS REGISTERS (PTP_TX_USER_IP_ADDRx)

Index (In Decimal): *x=0:* 2.342 *Size:* *16 bits*
x=1: 2.343
x=2: 2.344
x=3: 2.345
x=4: 2.346
x=5: 2.347
x=6: 2.348
x=7: 2.349

These read/write registers provide the 32-bit (IPv4) or 128-bit (IPv6) user defined IP address. Each register contains 16 bits of the address.

The User IP address can be enabled for the IPv4 or IPv6 protocols via their respective User Defined IP Address Enable bits in the PTP TX Parsing IP Format Address Enable Register (PTP_TX_PARSE_IP_ADDR_EN).

Register	Bits	Description	Type	Default
x=7 x=6	15:0	**IP Address[127:112]** **IP Address[111:96]** These fields contain the upper 32 bits of the 128 bit user defined IPv6 address and the entire 32 bits of the user defined IPv4 address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h 0000h
x=5 x=4 x=3 x=2 x=1 x=0	15:0	**IP Address[95:80]** **IP Address[79:64]** **IP Address[63:48]** **IP Address[47:32]** **IP Address[31:16]** **IP Address[15:0]** These fields contain the lower 96 bits of the 128 bit user defined IPv6 address used for PTP packet detection. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h 0000h 0000h 0000h 0000h 0000h

5.2.143 PTP TX USER IP MASK REGISTERS (PTP_TX_USER_IP_MASKx)

Index (In Decimal): x=0: 2.350 Size: 16 bits
x=1: 2.351
x=2: 2.352
x=3: 2.353
x=4: 2.354
x=5: 2.355
x=6: 2.356
x=7: 2.357

These read/write registers provide a 32-bit (IPv4) or 128-bit (IPv6) mask for the user defined IP address. Each register contains 16 bits of the mask.

Register	Bits	Description	Type	Default
x=7 x=6	15:0	**IP Mask[127:112]** **IP Mask[111:96]** These fields contain the upper 32 bits of the 128 bit user defined IPv6 mask and the entire 32 bits of the user defined IPv4 mask used for PTP packet detection. 0 : bit is ignored (considered a match) 1 : bit is compared **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	FFFFh FFFFh
x=5 x=4 x=3 x=2 x=1 x=0	15:0	**IP Mask[95:80]** **IP Mask[79:64]** **IP Mask[63:48]** **IP Mask[47:32]** **IP Mask[31:16]** **IP Mask[15:0]** These fields contain the lower 96 bits of the 128 bit user defined IPv6 mask used for PTP packet detection. 0 : bit is ignored (considered a match) 1 : bit is compared **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	FFFFh FFFFh FFFFh FFFFh FFFFh FFFFh

5.2.144 PTP LTC READ SECONDS HIGH REGISTER (PTP_LTC_RD_SEC_HI)

Index (In Decimal): 2.358 Size: 16 bits

This register contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[47:32])** This field contains the upper 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

5.2.145 PTP LTC READ SECONDS MID REGISTER (PTP_LTC_RD_SEC_MID)

Index (In Decimal): 2.359 Size: 16 bits

This register contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[31:16])** This field contains the middle 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

5.2.146 PTP LTC READ SECONDS LOW REGISTER (PTP_LTC_RD_SEC_LO)

Index (In Decimal): 2.360 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

5.2.147 PTP LTC READ NANOSECONDS HIGH REGISTER (PTP_LTC_RD_NS_HI)

Index (In Decimal): 2.361 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:14	***RESERVED***	*RO*	—
13:0	***LTC Nanoseconds (PTP_LTC_NS[29:16])*** *This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.*	*RO*	*0000h*

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

5.2.148 PTP LTC READ NANOSECONDS LOW REGISTER (PTP_LTC_RD_NS_LO)

Index (In Decimal): 2.362 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

5.2.149 PTP LTC READ SUB-NANOSECONDS HIGH REGISTER (PTP_LTC_RD_SUBNS_HI)

Index (In Decimal): 2.363 Size: 16 bits

This register contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[31:16])** This field contains the upper 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

5.2.150 PTP LTC READ SUB-NANOSECONDS LOW REGISTER (PTP_LTC_RD_SUBNS_LO)

Index (In Decimal): 2.364 Size: 16 bits

This register contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter. It is used to read the 1588 Local Time Counter following the setting of the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL).

Bits	Description	Type	Default
15:0	**LTC Sub-Nanoseconds (PTP_LTC_SUBNS[15:0])** This field contains the lower 16 bits of the sub-nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: The value read is the saved value of the 1588 Local Time Counter when the LTC Read (PTP_LTC_READ) bit in the PTP Command and Control Register (PTP_CMD_CTL) is set.

5.2.151 PTP REVISION REGISTER (PTP_REV)

Index (In Decimal): 2.365 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP_REVISON**	RO	Note 5-16

Note 5-16 The default value of the PTP Revision field varies dependent on the silicon revision number. For the initial revision of the device (mask set A0) this value is n/a since the register does not exist. For the second revision of the device (mask set A1) this value is n/a since the register does not exist. For the third revision of the device (mask set B0) this value defaults to 0001h.

5.2.152 PTP SPARE REGISTER (PTP_SPARE)

Index (In Decimal): 2.366 Size: 16 bits

Bits	Description	Type	Default
15:0	**PTP_SPARE**	R/W	0000h

5.2.153 PTP RX PARSING CONFIGURATION REGISTER (PTP_RX_PARSE_CONFIG)

Index (In Decimal): 2.368 Size: 32 bits

This register is used to configure the PTP receive message detection.

Bits	Description	Type	Default
15	**IPv6 Fragment Enable** This field determines if IPv6 fragmented frames are eligible for matching as a PTP frame. When set the presence of a Fragment extension header (a header value of 44) is allowed and skipped. When cleared, the presence of a Fragment extension header is not allowed and the frame rejected. 0 = fragments not allowed 1 = fragments allowed **Note:** This function must normally be disabled. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14	**Peer/Non-peer MAC / IP DA Mixing** When cleared, the MAC and IP Destination Addresses for peer delay messages and non-peer delay messages must match those assigned by the PTP specification for peer delay messages and non-peer delay messages respectively. When set, either destination address may be used for either peer delay messages or non-peer delay messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
13	**User IP DA Peer/Non-peer** When the Peer/Non-peer MAC / IP DA Mixing bit is cleared, this bit specifies whether the user defined IP Destination Address is used for peer or non-peer IPv4 and IPv6 formatted messages. 0 = peer messages 1 = non-peer messages When the Peer/Non-peer MAC / IP DA Mixing bit is set, the user defined IP Destination Address is used for both peer and non-peer IPv4 and IPv6 formatted messages. **Note:** This bit does not affect the IP Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
12	**User MAC DA Peer/Non-peer** When the Peer/Non-peer MAC / IP DA Mixing bit is cleared, this bit specifies whether the user defined MAC Destination Address is used for peer or non-peer Layer2, IPv4 and IPv6 formatted PTP messages. 0 = peer messages 1 = non-peer messages When the Peer/Non-peer MAC / IP DA Mixing bit is set, the user defined MAC Destination Address is used for both peer and non-peer Layer2, IPv4 and IPv6 formatted PTP messages. **Note:** This bit does not affect the MAC Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
11	**MAC Destination Address Enable (MAC_DA_EN)** This bit enables the checking of the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
10:8	**User MAC DA Mode** These three bits select the address match mode for the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. One or multiple bits can be set allowing any combination of match types. bit 0 : match the 48 bit address bit 1 : match any unicast address bit 2 : match any multicast address **Note:** These bits do not affect the MAC Source Address matching, which, if enabled, always matches against the 48 bit address. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000b
7	**IPv4 Fragment Enable** This field determines if IPv4 fragmented frames are eligible for matching as a PTP frame. When set, the More Fragments (MF) flag and Fragment Offset field are ignored. When cleared, the More Fragments (MF) flag and Fragment Offset field within the frame must equal 0. 0 = fragments not allowed 1 = fragments allowed **Note:** This function must normally be disabled. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
6	**UDP Source Port Number Enable** When set, the UDP source port number specified in the PTP RX Parsing UDP Source Port Register (PTP_RX_PARSE_UDP_SRC_PORT) is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
5	**UDP Destination Port Number Enable** When set, the UDP destination port number specified in the PTP RX Parsing UDP Destination Port Register (PTP_RX_PARSE_UDP_DEST_PORT) is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
4	**MAC / IP Address Consistency Checking** When cleared, the MAC and IP Destination Addresses are independently tested. When set, the MAC Destination Address must be consistent with the corresponding IP Destination Address. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
3	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the UDP checksum for PTP frame parsing. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not validated and the frame is not timestamped. When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not validated and the frame is not timestamped. **Note:** If PTP_UDP_CHKSUM_DIS is set then this bit does not matter since checksum testing is overridden. **Note:** If the checksum value is 0x0000 and PTP_UDPV6_ZERO_CHKSUM_EN is set then this bit does not matter since the checksum is always considered valid. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2	**IPv6 Enable (IPV6_EN)** This bit enables the detection of the UDP/IPv6 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b

Bits	Description	Type	Default
1	**IPv4 Enable (IPV4_EN)** This bit enables the detection of the UDP/IPv4 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
0	**Layer 2 Enable (LAYER2_EN)** This bit enables the detection of the Layer 2 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b

5.2.154 PTP RX PARSING VLAN CONFIGURATION REGISTER (PTP_RX_PARSE_VLAN_CONFIG)

Index (In Decimal): 2.369 Size: 32 bits

This register is used to configure the VLAN parsing for PTP receive messages.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:4	**VLAN Tag Count** When VLAN checking is enabled, this field specifies the expected number of VLAN tags. 000 : No VLAN tags allowed 001 : Exactly one VLAN tag expected 010 : Exactly two VLAN tags expected 101 : At least one VLAN tags expected 110 : At least two VLAN tags expected 111 : Any amount of VLAN tags allowed others: reserved **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000b
3	**RESERVED**	RO	—
2	**VLAN Checking Enable** When set, the number and contents of the VLAN tags is checked. When cleared, VLAN tags are parsed but skipped. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
1	**VLAN 2 Checking Enable** When set, the EtherType and VID value of VLAN 2 is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
0	**VLAN 1 Checking Enable** When set, the EtherType and VID value of VLAN 1 is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.155 PTP RX PARSING LAYER2 FORMAT ADDRESS ENABLE REGISTER (PTP_RX_PARSE_L2_ADDR_EN)

Index (In Decimal): 2.370 Size: 32 bits

This register is used to enable MAC addresses for Layer 2 formatted PTP receive messages.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**Layer 2 MAC Destination Address 1 Enable (L2_MAC_DA1_EN)** This bit enables the MAC Destination Address of 01:80:C2:00:00:0E for Layer 2 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
2	**Layer 2 MAC Destination Address 2 Enable (L2_MAC_DA2_EN)** This bit enables the MAC Destination Address of 01:1B:19:00:00:00 for Layer 2 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
1:0	**User Defined Layer 2 MAC Address Enable (L2_USER_MAC_EN)** These bits enable a user defined MAC address for Layer 2 PTP messages. The address is defined via the PTP RX User MAC Address High/Mid/Low Registers (PTP_RX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b

5.2.156 PTP RX PARSING IP FORMAT ADDRESS ENABLE REGISTER (PTP_RX_PARSE_IP_ADDR_EN)

Index (In Decimal): 2.371 Size: 32 bits

This register is used to enable MAC and IP addresses for IPv4 and IPv6 formatted PTP receive messages.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**IP Destination Address Enable (IP_DA_EN)** This bit enables the checking of the IP Destination Address in PTP messages for both IPv4 and IPv6 formats. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
12	**IP Destination Address 1 Enable (IP_DA1_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:81 and the IPv4 Destination Address of 224.0.1.129 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:81 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:181 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
11	**IP Destination Address 2 Enable (IP_DA2_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:82 and the IPv4 Destination Address of 224.0.1.130 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:82 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:182 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
10	**IP Destination Address 3 Enable (IP_DA3_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:83 and the IPv4 Destination Address of 224.0.1.131 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:83 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:183 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
9	**IP Destination Address 4 Enable (IP_DA4_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:84 and the IPv4 Destination Address of 224.0.1.132 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:84 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:184 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
8	**IP Destination Address 5 Enable (IP_DA5_EN)** This bit enables the MAC Destination Address of 01:00:5e:00:00:6B and the IPv4 Destination Address of 224.0.0.107 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:00:6B and the IPv6 Destination Address of FF02:0:0:0:0:0:0:6B for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
7:6	**User Defined IPv6 MAC Address Enable (IPV6_USER_MAC_EN)** These bits enable a user defined MAC address for IPv6 PTP messages. The address is defined via the PTP RX User MAC Address High/Mid/Low Registers (PTP_RX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b
5:4	**User Defined IPv6 IP Address Enable (IPV6_USER_IP_EN)** These bits enable a user defined IP address for IPv6 PTP messages. The address is defined via the PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) as masked by the PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b
3:2	**User Defined IPv4 MAC Address Enable (IPV4_USER_MAC_EN)** These bits enable a user defined MAC address for IPv4 PTP messages. The address is defined via the PTP RX User MAC Address High/Mid/Low Registers (PTP_RX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b

Bits	Description	Type	Default
1:0	**User Defined IPv4 IP Address Enable (IPV4_USER_IP_EN)** These bits enable a user defined MAC IP address for IPv4 PTP messages. The address is defined via the PTP RX User IP Address Registers (PTP_RX_USER_IP_ADDRx) as masked by the PTP RX User IP Mask Registers (PTP_RX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b

5.2.157 PTP RX PARSING UDP SOURCE PORT REGISTER (PTP_RX_PARSE_UDP_SRC_PORT)

Index (In Decimal): 2.372 Size: 16 bits

This register is used to configure the PTP receive message detection.

Bits	Description	Type	Default
15:0	**UDP Source Port Number (UDP_SOURCE_PORT[15:0])** This field specifies the UDP source port number. If UDP Source Port Number Enable is set, the UDP source port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.158 PTP RX PARSING UDP DESTINATION PORT REGISTER (PTP_RX_PARSE_UDP_DEST_PORT)

Index (In Decimal): 2.373 Size: 16 bits

This register is used to configure the PTP receive message detection.

Bits	Description	Type	Default
15:0	**UDP Destination Port Number (UDP_DEST_PORT[15:0])** This field specifies the UDP destination port number. If UDP Destination Port Number Enable is set, the UDP destination port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	319

5.2.159 PTP RX VERSION REGISTER (PTP_RX_VERSION)

Index (In Decimal): 2.374 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15:8	**PTP Version Upper Range (PTP_VERSION_UP[7:0])** This field contains the PTP version range upper limit. This field is used along with the PTP version range lower limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	20h
7:0	**PTP Version Lower Range (PTP_VERSION_LO[7:0])** This field contains the PTP version range lower limit. This field is used along with the PTP version range upper limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	20h

5.2.160 PTP RX DOMAIN / DOMAIN RANGE LOWER REGISTER (PTP_RX_DOMAIN_DOMAIN_LO)

Index (In Decimal): 2.375 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15	**PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN)** When this bit is cleared, the domainNumber in the PTP message is checked against the masked value in PTP Domain (PTP_DOMAIN[7:0]). When this bit is set, domainNumber range checking is used. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14:8	**RESERVED**	RO	—
7:0	**PTP Domain (PTP_DOMAIN[7:0])** **PTP Domain Lower Range (PTP_DOMAIN_LO[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN). This field contains the PTP domain in use. Each bit may be masked using the PTP Domain Mask field. This field contains the PTP domain range lower limit. This field is used along with the PTP domain upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00h

5.2.161 PTP RX DOMAIN MASK / DOMAIN RANGE UPPER REGISTER (PTP_RX_DOMAIN_MASK_DOMAIN_UP)

Index (In Decimal): 2.376 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**PTP Domain Mask (PTP_DOMAIN_MASK)** **PTP Domain Upper Range (PTP_DOMAIN_UP[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN) This field contains the PTP Domain Mask. 0 : bit is ignored (considered a match) 1 : bit is compared This field contains the PTP domain range upper limit. This field is used along with the PTP domain range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00h

5.2.162 PTP RX SDOID / SDOID RANGE LOWER REGISTER (PTP_RX_SDOID_SDOID_LO)

Index (In Decimal): 2.377 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15	**PTP SdoId Range Enable (PTP_SDOID_RANGE_EN)** When this bit is cleared, the majorSdoId and minorSdoId fields in the PTP message are checked against the masked value in PTP SdoId (PTP_SDOID[11:0]). When this bit is set, majorSdoId and minorSdoId range checking is used. The majorSdoId and minorSdoId fields are concatenate and treated as a 12 bit value. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14:12	**RESERVED**	RO	—
11:0	**PTP SdoId (PTP_SDOID[11:0])** **PTP SdoId Lower Range (PTP_SDOID_LO[11:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN). This field contains the PTP SdoId in use. Each bit may be masked using the PTP SdoId Mask field. This field contains the PTP SdoId range lower limit. This field is used along with the PTP SdoId upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.163 PTP RX SDOID MASK / SDOID RANGE UPPER REGISTER (PTP_RX_SDOID_MASK_SDOID_UP)

Index (In Decimal): 2.378 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**PTP Sdoid Mask (PTP_SDOID_MASK[11:0])** **PTP Sdoid Upper Range (PTP_SDOID_UP[11:0])** This field has two uses based on the PTP Sdoid Range Enable (PTP_SDOID_RANGE_EN) This field contains the PTP Sdoid Mask. 0 : bit is ignored (considered a match) 1 : bit is compared This field contains the PTP Sdoid range upper limit. This field is used along with the PTP Sdoid range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.164 PTP RX TIMESTAMP ENABLE REGISTER (PTP_RX_TIMESTAMP_EN)

Index (In Decimal): 2.379 Size: 32 bits

This register is used to enable PTP receive message timestamping.

Bits	Description	Type	Default
15:0	**PTP Message Type Enable (PTP_MESSAGE_EN[15:0])** These bits individually enable timestamping of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled.	R/W	0000h

5.2.165 PTP RX TIMESTAMP CONFIGURATION REGISTER (PTP_RX_TIMESTAMP_CONFIG)

Index (In Decimal): 2.380 Size: 32 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP Allow UDPv6 Zero Checksum (PTP_UDPV6_ZERO_CHKSUM_EN)** When this bit is set, a zero checksum value for IPv6/UDP frames is considered valid. **Note:** If PTP_UDP_CHKSUM_DIS is set then this bit does not matter since checksum testing is overridden. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2	**PTP Alternate Master Enable (PTP_ALT_MASTER_EN)** When this bit is set, the alternateMasterFlag in the PTP message is checked for a zero value. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
1	**PTP UDP Checksum Check Disable (PTP_UDP_CHKSUM_DIS)** When this bit is cleared, ingress times are not saved if the frame has an invalid UDP checksum. When this bit is set, the UDP checksum check is bypassed and the ingress time is saved regardless. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**PTP FCS Check Disable (PTP_FCS_DIS)** When this bit is cleared, ingress times are not saved if the frame has an invalid FCS. When this bit is set, the FCS check is bypassed. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.166 PTP RX MODIFICATION REGISTER (PTP_RX_MOD)

Index (In Decimal): 2.381 Size: 16 bits

This register is used to configure PTP message timestamp insertion.

Bits	Description	Type	Default
15:5	**RESERVED**	RO	-
4	**PTP Bad UDPv6 Checksum Force FCS Disable (PTP_BAD_UDPV6_CHKSUM_FORCE_FCS_DIS)** When this bit is cleared, IPv6 ingress packets that have an invalid UDP checksum will have a bad FCS forced if the packet is modified for timestamp or correction field reasons. When this bit is set, the UDP checksum check is bypassed. **Note:** This field should normally be left at its default value of 1 so that FCS errors are not forced. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
3	**PTP Bad UDPv4 Checksum Force FCS Disable (PTP_BAD_UDPV4_CHKSUM_FORCE_FCS_DIS)** When this bit is cleared, IPv4 ingress packets that have an invalid UDP checksum will have a bad FCS forced if the packet is modified for timestamp or correction field reasons. When this bit is set, the UDP checksum check is bypassed. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2	**PTP Insert Timestamp Seconds Enable (PTP_INSERT_TS_SEC_EN)** When PTP_INSERT_TS_EN is set, this bit enables bits 3:0 of the seconds portion of the receive ingress time to be inserted into the PTP message. This bit has no affect if PTP_INSERT_TS_EN is a low.	R/W	0b
1	**PTP Insert Timestamp 32 Bit Mode (PTP_INSERT_TS_32BIT)** When timestamps are inserted into the received PTP message, this bit enables bits 1:0 of the seconds portion of the receive ingress time to be inserted into the upper two bits of the 4 byte reserved field in the PTP message. Otherwise the upper two bits of the 4 byte reserved field will contain 00b.	R/W	0b
0	**PTP Insert Timestamp Enable (PTP_INSERT_TS_EN)** When set, receive ingress times are inserted into the PTP message.	R/W	0b

5.2.167 PTP RX RESERVED BYTES CONFIGURATION REGISTER (PTP_RX_RSVD_BYTE_CFG)

Index (In Decimal): 2.382 Size: 16 bits

This register is used to configure the location of the reserved bytes inside the RX PTP messages.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:6	**PTP 4 Reserved Bytes Offset (PTP_4_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header where the receive ingress time is inserted. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	010000b
5:0	**PTP 1 Reserved Byte Offset (PTP_1_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header where the seconds portion of the receive ingress time is inserted. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000101b

5.2.168 PTP RX TAIL TAG REGISTER (PTP_RX_TAIL_TAG)

Index (In Decimal): 2.383 Size: 16 bits

This register is used to configure tail tagging.

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**PTP Forward Tail Tag Clipped RX_ER (PTP_FWD_CLIPPED_ER)** 1 : forward RX_ER from clipped portion of frame 0 : ignore RX_ER from clipped portion of frame	R/W	1b
7:4	**PTP Tail Tag Insert Minimum IFG (PTP_TAIL_TAG_INSERT_IFG)** When the PTP_TAIL_TAG_EN and PTP_TAIL_TAG_INSERT bits are set, this field specifies the minimum IFG in bytes to enforces between resultant frames. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1
3	**PTP Tail Tag Insert (PTP_TAIL_TAG_INSERT)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that the timestamp is inserted before a new FCS. Otherwise the timestamp replaces the existing FCS without a new FCS. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
2	**PTP Tail Tag All (PTP_TAIL_TAG_ALL)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all frames are to be tail tagged. Otherwise only 1588 messages are tail tagged. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
1	**PTP Tail Tag All 1588 (PTP_TAIL_TAG_ALL_1588)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all 1588 frames are to be tail tagged. Otherwise only those messages enabled via the PTP_RX_TIMESTAMP_EN register are tail tagged. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**PTP Tail Tag Timestamp Enable (PTP_TAIL_TAG_EN)** When this bit is set, the FCS will be replaced by the ingress timestamp. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.169 PTP RX CORRECTION FIELD MODIFICATION ENABLE REGISTER (PTP_RX_CF_MOD_EN)

Index (In Decimal): 2.384 Size: 16 bits

This register is used to enable RX PTP message correction field modifications.

Bits	Description	Type	Default
15:0	**PTP Correction Field Message Type Enable (PTP_CF_MSG_EN[15:0])** These bits individually enable correction field modification of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled.	R/W	0000h

5.2.170 PTP RX CORRECTION FIELD CONFIGURATION REGISTER (PTP_RX_CF_CFG)

Index (In Decimal): 2.385 Size: 16 bits

This register is used to configure RX PTP message correction field modifications.

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1	**PTP Correction Field Maximum Value Test Disable (PTP_MAX_CF_DIS)** This bit disables the checking for the maximum correction field value of 7FFF_FFFF_FFFF_FFFFh. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**PTP Correction Field Method (PTP_CF_METHOD)** This bit determines the method of correction field modification. 0 : Method A - CF_RSVD_4 - ingress time stored in 4 reserved bytes 1 : Method B - CF_SUB_ADD_64 - ingress time subtracted from correction field **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.171 PTP RX INGRESS TIME NANOSECONDS HIGH REGISTER (PTP_RX_INGRESS_NS_HI)

Index (In Decimal): 2.386 Size: 16 bits

This read only register combined with the PTP RX Ingress Time Seconds High/Low Registers (PTP_RX_INGRESS_SEC_HI/LO) and the PTP RX Ingress Time Nanoseconds Low Register (PTP_RX_INGRESS_NS_LO) contains the RX timestamp capture. Up to eight captures are buffered. This register contains the upper 14 bits of the timestamps nanoseconds.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15	**PTP RX Timestamp Valid (PTP_RX_TS_VALID)** This field indicates that the timestamp is valid (there is at least one timestamp available to be read).	RO	0b
14	**RESERVED**	RO	-
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the receive ingress time.	RO	0000h

5.2.172 PTP RX INGRESS TIME NANOSECONDS LOW REGISTER (PTP_RX_INGRESS_NS_LO)

Index (In Decimal): 2.387 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the receive ingress time.	RO	0000h

5.2.173 PTP RX INGRESS TIME SECONDS HIGH REGISTER (PTP_RX_INGRESS_SEC_HI)

Index (In Decimal): 2.388 Size: 16 bits

This read only register combined with the PTP RX Ingress Time Seconds Low Register (PTP_RX_INGRESS_SEC_LO) and the PTP RX Ingress Time Nanoseconds High/Low Registers (PTP_RX_INGRESS_NS_HI/LO) contains the RX timestamp captures. Up to eight captures are buffered. This register contains the upper 16 bits of the timestamps seconds.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the receive ingress time.	RO	0000h

5.2.174 PTP RX INGRESS TIME SECONDS LOW REGISTER (PTP_RX_INGRESS_SEC_LO)

Index (In Decimal): 2.389 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC15:0])** This field contains the seconds portion of the receive ingress time.	RO	0000h

5.2.175 PTP RX MESSAGE HEADER 1 REGISTER (PTP_RX_MSG_HEADER1)

Index (In Decimal): 2.390 Size: 16 bits

This read only register contains the sourcePortIdentity and messageType of the RX message header. Up to eight captures are buffered.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:4	**Source Port Identity CRC (SRC_PRT_CRC)** This field contains the 12-bit CRC of the sourcePortIdentity field of the received PTP packet.	RO	000h
3:0	**Message Type (MSG_TYPE)** This field contains the messageType field of the received PTP packet.	RO	0h

5.2.176 PTP RX MESSAGE HEADER 2 REGISTER (PTP_RX_MSG_HEADER2)

Index (In Decimal): 2.391 Size: 16 bits

This read only register contains the sequenceId of the RX message header. Up to eight captures are buffered.

Note: Values are only valid if the PTP RX Timestamp Interrupt (PTP_RX_TS_INT) field or the PTP RX Timestamp Valid (PTP_RX_TS_VALID) field is set indicating that at least one timestamp is available.

Reading this register will pop the capture FIFO.

Note: This register may be read without causing a FIFO underflow.

Bits	Description	Type	Default
15:0	**Sequence ID (SEQ_ID)** This field contains the sequenceId field of the received PTP packet.	RO	0000h

5.2.177 PTP RX PDELAY_REQ INGRESS TIME SECONDS HIGH REGISTER (PTP_RX_PDREQ_SEC_HI)

Index (In Decimal): 2.392 Size: 16 bits

This register combined with the PTP RX Pdelay_Req Ingress Time Seconds Mid/Low Registers (PTP_RX_PDREQ_SEC_MID/LO) and the PTP RX Pdelay_Req Ingress Time Nanoseconds High/Low Registers (PTP_RX_PDREQ_NS_HI/LO) contains the ingress time of the last Pdelay_Req message. This register contains the upper 16 bits of the timestamps seconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[47:32])** This field contains the seconds portion of the receive ingress time.	R/W	0000h

5.2.178 PTP RX PDELAY_REQ INGRESS TIME SECONDS MID REGISTER (PTP_RX_PDREQ_SEC_MID)

Index (In Decimal): 2.393 Size: 16 bits

This register contains the middle 16 bits of the timestamps seconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the receive ingress time.	R/W	0000h

5.2.179 PTP RX PDELAY_REQ INGRESS TIME SECONDS LOW REGISTER (PTP_RX_PDREQ_SEC_LOW)

Index (In Decimal): 2.394 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the receive ingress time.	R/W	0000h

5.2.180 PTP RX PDELAY_REQ INGRESS TIME NANOSECONDS HIGH REGISTER (PTP_RX_PDREQ_NS_HI)

Index (In Decimal): 2.395 Size: 16 bits

This register combined with the PTP RX Pdelay_Req Ingress Time Seconds High/Mid/Low Registers (PTP_RX_PDREQ_SEC_HI/MID/LO) and the PTP RX Pdelay_Req Ingress Time Nanoseconds Low Register (PTP_RX_PDREQ_NS_LO) contains the ingress time of the last Pdelay_Req message. This register contains the upper 14 bits of the timestamps nanoseconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**Auto Update (AUTO)** If this bit is set, the TS_NS field in this register and PTP_RX_PDREQ_NS_LO, the TS_SEC field in PTP_RX_PDREQ_SEC_HI/MID/LO and the CF field in PTP_RX_PDREQ_CF_HI/MID/LO are updated when a Pdelay_Req message is received. When cleared, S/W is responsible to maintain those fields. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14	**Pdelay_Req Timestamp Valid (PDREQ_TS_VLD)** This field indicates if the RX Pdelay_Req Ingress Time and Correction Field registers are valid. This bit should be set by software after programming the registers. It is automatically set when a Pdelay_Req message is received with the Auto Update (AUTO) bit set. Depending on the egress offload mode used, this bit is cleared once the Pdelay_Resp or Pdelay_Resp_Follow_Up is transmitted. It can also be cleared by software.	R/W/SC	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the receive ingress time.	R/W	00000000h

5.2.181 PTP RX PDELAY_REQ INGRESS TIME NANOSECONDS LOW REGISTER (PTP_RX_PDREQ_NS_LO)

Index (In Decimal): 2.396 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

This register is automatically updated if the Auto Update (AUTO) bit is set.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the receive ingress time.	R/W	0000h

5.2.182 PTP RX RAW INGRESS TIME SECONDS REGISTER (PTP_RX_RAW_TS_SEC)

Index (In Decimal): 2.397 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter captured at the start of each frame.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

5.2.183 PTP RX RAW INGRESS TIME NANOSECONDS HIGH REGISTER (PTP_RX_RAW_TS_NS_HI)

Index (In Decimal): 2.398 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	-
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

5.2.184 PTP RX RAW INGRESS TIME NANOSECONDS LOW REGISTER (PTP_RX_RAW_TS_NS_LO)

Index (In Decimal): 2.399 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

5.2.185 PTP RX CHECKSUM DROPPED COUNT HIGH REGISTER (PTP_RX_CHKSUM_DROPPED_CNT_HI)

Index (In Decimal): 2.400 Size: 16 bits

This register along with the PTP RX Checksum Dropped Count Low Register (PTP_RX_CHKSUM_DROPPED_CNT_LO) counts the number of ingress packets forced to have an FCS error due to a bad original UDP checksum. This register contains the upper 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[31:16])** This field is a count of ingress packets forced to have an FCS error due to a bad original UDP checksum. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. **Note:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

5.2.186 PTP RX CHECKSUM DROPPED COUNT LOW REGISTER (PTP_RX_CHKSUM_DROPPED_CNT_LO)

Index (In Decimal): 2.401 Size: 16 bits

This register contains the lower 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[15:0])** This field is a count of ingress packets forced to have an FCS error due to a bad original UDP checksum. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. **Note:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

5.2.187 PTP RX FRAMES MODIFIED COUNT HIGH REGISTER (PTP_RX_FRMS_MOD_CNT_HI)

Index (In Decimal): 2.402 Size: 16 bits

This register along with the PTP RX Frames Modified Count Low Register (PTP_RX_FRMS_MOD_CNT_LO) counts the number of packets that were modified on ingress. This register contains the upper 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**RX Frames Modified Count (RX_FRMS_MOD_CNT[31:16])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

5.2.188 PTP RX FRAMES MODIFIED COUNT LOW REGISTER (PTP_RX_FRMS_MOD_CNT_LO)

Index (In Decimal): 2.403 Size: 16 bits

This register contains the lower 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**RX Frames Modified Count (RX_FRMS_MOD_CNT[15:0])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

5.2.189 PTP TX PARSING CONFIGURATION REGISTER (PTP_TX_PARSE_CONFIG)

Index (In Decimal): 2.432 Size: 32 bits

This register is used to configure the PTP transmit message detection.

Bits	Description	Type	Default
15	**IPv6 Fragment Enable** This field determines if IPv6 fragmented frames are eligible for matching as a PTP frame. When set the presence of a Fragment extension header (a header value of 44) is allowed and skipped. When cleared, the presence of a Fragment extension header is not allowed and the frame rejected. 0 = fragments not allowed 1 = fragments allowed **Note:** This function must normally be disabled. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14	**Peer/Non-peer MAC / IP DA Mixing** When cleared, the MAC and IP Destination Addresses for peer delay messages and non-peer delay messages must match those assigned by the PTP specification for peer delay messages and non-peer delay messages respectively. When set, either destination address may be used for either peer delay messages or non-peer delay messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
13	**User IP DA Peer/Non-peer** When the Peer/Non-peer MAC / IP DA Mixing bit is cleared, this bit specifies whether the user defined IP Destination Address is used for peer or non-peer IPv4 and IPv6 formatted messages. 0 = peer messages 1 = non-peer messages When the Peer/Non-peer MAC / IP DA Mixing bit is set, the user defined IP Destination Address is used for both peer and non-peer IPv4 and IPv6 formatted messages. **Note:** This bit does not affect the IP Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
12	**User MAC DA Peer/Non-peer** When the Peer/Non-peer MAC / IP DA Mixing bit is cleared, this bit specifies whether the user defined MAC Destination Address is used for peer or non-peer Layer2, IPv4 and IPv6 formatted PTP messages. 0 = peer messages 1 = non-peer messages When the Peer/Non-peer MAC / IP DA Mixing bit is set, the user defined MAC Destination Address is used for both peer and non-peer Layer2, IPv4 and IPv6 formatted PTP messages. **Note:** This bit does not affect the MAC Source Address matching, which, if enabled, matches for Peer and Non-peer messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
11	**MAC Destination Address Enable (MAC_DA_EN)** This bit enables the checking of the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
10:8	**User MAC DA Mode** These three bits select the address match mode for the MAC Destination Address in Layer2, IPv4 and IPv6 formatted PTP messages. One or multiple bits can be set allowing any combination of match types. bit 0 : match the 48 bit address bit 1 : match any unicast address bit 2 : match any multicast address **Note:** These bits do not affect the MAC Source Address matching, which, if enabled, always matches against the 48 bit address. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000b

Bits	Description	Type	Default
7	**IPv4 Fragment Enable** This field determines if IPv4 fragmented frames are eligible for matching as a PTP frame. When set, the More Fragments (MF) flag and Fragment Offset field are ignored. When cleared, the More Fragments (MF) flag and Fragment Offset field within the frame must equal 0. 0 = fragments not allowed 1 = fragments allowed **Note:** This function must normally be disabled. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
6	**UDP Source Port Number Enable** When set, the UDP source port number specified in the PTP TX Parsing UDP Source Port Register (PTP_TX_PARSE_UDP_SRC_PORT) is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
5	**UDP Destination Port Number Enable** When set, the UDP destination port number specified in the PTP TX Parsing UDP Destination Port Register (PTP_TX_PARSE_UDP_DEST_PORT) is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
4	**MAC / IP Address Consistency Checking** When cleared, the MAC and IP Destination Addresses are independently tested. When set, the MAC Destination Address must be consistent with the corresponding IP Destination Address. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
3	**Enable Other Routing Headers** This bit allows the usage of IPv6 Routing headers other than type 0 and 2 when validating the UDP checksum for PTP frame parsing. When cleared, IPv6 Routing headers other than type 0 and 2 are not supported and the checksum is not validated and the frame is not timestamped. When set, IPv6 Routing headers other than type 0 and 2 are skipped, if the Segments Left field in the header is zero, otherwise, the checksum is not validated and the frame is not timestamped. **Note:** If PTP_UDP_CHKSUM_DIS is set then this bit does not matter since checksum testing is overridden. **Note:** If the checksum value is 0x0000 and PTP_UDPV6_ZERO_CHKSUM_EN is set then this bit does not matter since the checksum is always considered valid. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2	**IPv6 Enable (IPV6_EN)** This bit enables the detection of the UDP/IPv6 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
1	**IPv4 Enable (IPV4_EN)** This bit enables the detection of the UDP/IPv4 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
0	**Layer 2 Enable (LAYER2_EN)** This bit enables the detection of the Layer 2 formatted PTP messages. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b

5.2.190 PTP TX PARSING VLAN CONFIGURATION REGISTER (PTP_TX_PARSE_VLAN_CONFIG)

Index (In Decimal): 2.433 Size: 32 bits

This register is used to configure the VLAN parsing for PTP transmit messages.

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6:4	**VLAN Tag Count** When VLAN checking is enabled, this field specifies the expected number of VLAN tags. 000 : No VLAN tags allowed 001 : Exactly one VLAN tag expected 010 : Exactly two VLAN tags expected 101 : At least one VLAN tags expected 110 : At least two VLAN tags expected 111 : Any amount of VLAN tags allowed others: reserved **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000b
3	**RESERVED**	RO	—
2	**VLAN Checking Enable** When set, the number and contents of the VLAN tags is checked. When cleared, VLAN tags are parsed but skipped. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
1	**VLAN 2 Checking Enable** When set, the EtherType and VID value of VLAN 2 is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**VLAN 1 Checking Enable** When set, the EtherType and VID value of VLAN 1 is checked. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.191 PTP TX PARSING LAYER2 FORMAT ADDRESS ENABLE REGISTER (PTP_TX_PARSE_L2_ADDR_EN)

Index (In Decimal): 2.434 Size: 32 bits

This register is used to enable MAC addresses for Layer 2 formatted PTP transmit messages.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**Layer 2 MAC Destination Address 1 Enable (L2_MAC_DA1_EN)** This bit enables the MAC Destination Address of 01:80:C2:00:00:0E for Layer 2 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
2	**Layer 2 MAC Destination Address 2 Enable (L2_MAC_DA2_EN)** This bit enables the MAC Destination Address of 01:1B:19:00:00:00 for Layer 2 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
1:0	**User Defined Layer 2 MAC Address Enable (L2_USER_MAC_EN)** These bits enable a user defined MAC address for Layer 2 PTP messages. The address is defined via the PTP TX User MAC Address High/Mid/Low Registers (PTP_TX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b

5.2.192 PTP TX PARSING IP FORMAT ADDRESS ENABLE REGISTER (PTP_TX_PARSE_IP_ADDR_EN)

Index (In Decimal): 2.435 Size: 32 bits

This register is used to enable MAC and IP addresses for IPv4 and IPv6 formatted PTP transmit messages.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**IP Destination Address Enable (IP_DA_EN)** This bit enables the checking of the IP Destination Address in PTP messages for both IPv4 and IPv6 formats. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
12	**IP Destination Address 1 Enable (IP_DA1_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:81 and the IPv4 Destination Address of 224.0.1.129 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:81 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:181 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
11	**IP Destination Address 2 Enable (IP_DA2_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:82 and the IPv4 Destination Address of 224.0.1.130 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:82 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:182 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
10	**IP Destination Address 3 Enable (IP_DA3_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:83 and the IPv4 Destination Address of 224.0.1.131 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:83 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:183 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
9	**IP Destination Address 4 Enable (IP_DA4_EN)** This bit enables the MAC Destination Address of 01:00:5E:00:01:84 and the IPv4 Destination Address of 224.0.1.132 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:01:84 and the IPv6 Destination Address of FF0X:0:0:0:0:0:0:184 for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

Bits	Description	Type	Default
8	**IP Destination Address 5 Enable (IP_DA5_EN)** This bit enables the MAC Destination Address of 01:00:5e:00:00:6B and the IPv4 Destination Address of 224.0.0.107 for IPv4 PTP packets. This bit enables the MAC Destination Address of 33:33:00:00:00:6B and the IPv6 Destination Address of FF02:0:0:0:0:0:0:6B for IPv6 PTP packets. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
7:6	**User Defined IPv6 MAC Address Enable (IPV6_USER_MAC_EN)** These bits enable a user defined MAC address for IPv6 PTP messages. The address is defined via the PTP TX User MAC Address High/Mid/Low Registers (PTP_TX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b
5:4	**User Defined IPv6 IP Address Enable (IPV6_USER_IP_EN)** These bits enable a user defined IP address for IPv6 PTP messages. The address is defined via the PTP TX User IP Address Registers (PTP_TX_USER_IP_ADDRx) as masked by the PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b
3:2	**User Defined IPv4 MAC Address Enable (IPV4_USER_MAC_EN)** These bits enable a user defined MAC address for IPv4 PTP messages. The address is defined via the PTP TX User MAC Address High/Mid/Low Registers (PTP_TX_USER_MAC_HI/MID/LO). The user defined MAC address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b

Bits	Description	Type	Default
1:0	**User Defined IPv4 IP Address Enable (IPV4_USER_IP_EN)** These bits enable a user defined MAC IP address for IPv4 PTP messages. The address is defined via the PTP TX User IP Address Registers (PTP_TX-_USER_IP_ADDRx) as masked by the PTP TX User IP Mask Registers (PTP_TX_USER_IP_MASKx). The user defined IP address may be enabled for the destination or source address as follows: 11 : either source or destination address 10 : source address 01 : destination address 00 : neither **Note:** The host S/W must not change these bits while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00b

5.2.193 PTP TX PARSING UDP SOURCE PORT REGISTER (PTP_TX_PARSE_UDP_SRC_PORT)

Index (In Decimal): 2.436 Size: 16 bits

This register is used to configure the PTP transmit message detection.

Bits	Description	Type	Default
15:0	**UDP Source Port Number (UDP_SOURCE_PORT[15:0])** This field specifies the UDP source port number. If UDP Source Port Number Enable is set, the UDP source port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0000h

5.2.194 PTP TX PARSING UDP DESTINATION PORT REGISTER (PTP_TX_PARSE_UDP_DEST_PORT)

Index (In Decimal): 2.437 Size: 16 bits

This register is used to configure the PTP transmit message detection.

Bits	Description	Type	Default
15:0	**UDP Destination Port Number (UDP_DEST_PORT[15:0])** This field specifies the UDP destination port number. If UDP Destination Port Number Enable is set, the UDP destination port number in the frame must match the value in this field in order for the frame to be considered a PTP frame. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	319

5.2.195 PTP TX VERSION REGISTER (PTP_TX_VERSION)

Index (In Decimal): 2.438 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

Bits	Description	Type	Default
15:8	**PTP Version Upper Range (PTP_VERSION_UP[7:0])** This field contains the PTP version range upper limit. This field is used along with the PTP version range lower limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	20h
7:0	**PTP Version Lower Range (PTP_VERSION_LO[7:0])** This field contains the PTP version range lower limit. This field is used along with the PTP version range upper limit field. Values are inclusive. The upper four bits correspond to the versionPTP message field, while the lower four bits correspond to the minorVersionPTP message field. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	20h

5.2.196 PTP TX DOMAIN / DOMAIN RANGE LOWER REGISTER (PTP_TX_DOMAIN_DOMAIN_LO)

Index (In Decimal): 2.439 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

Bits	Description	Type	Default
15	**PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN)** When this bit is cleared, the domainNumber in the PTP message is checked against the masked value in PTP Domain (PTP_DOMAIN[7:0]). When this bit is set, domainNumber range checking is used. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14:8	**RESERVED**	RO	—
7:0	**PTP Domain (PTP_DOMAIN[7:0])** **PTP Domain Lower Range (PTP_DOMAIN_LO[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN). This field contains the PTP domain in use. Each bit may be masked using the PTP Domain Mask field. This field contains the PTP domain range lower limit. This field is used along with the PTP domain upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00h

5.2.197 PTP TX DOMAIN MASK / DOMAIN RANGE UPPER REGISTER (PTP_TX_DOMAIN_MASK_DOMAIN_UP)

Index (In Decimal): 2.440 Size: 16 bits

This register is used to configure PTP transmit message timestamping and modification.

Bits	Description	Type	Default
15:8	**RESERVED**	RO	—
7:0	**PTP Domain Mask (PTP_DOMAIN_MASK)** **PTP Domain Upper Range (PTP_DOMAIN_UP[7:0])** This field has two uses based on the PTP Domain Range Enable (PTP_DOMAIN_RANGE_EN) This field contains the PTP Domain Mask. 0 : bit is ignored (considered a match) 1 : bit is compared This field contains the PTP domain range upper limit. This field is used along with the PTP domain range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	00h

5.2.198 PTP TX SDOID / SDOID RANGE LOWER REGISTER (PTP_TX_SDOID_SDOID_LO)

Index (In Decimal): 2.441 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15	**PTP Sdoid Range Enable (PTP_SDOID_RANGE_EN)** When this bit is cleared, the majorSdoId and minorSdoId fields in the PTP message are checked against the masked value in PTP SdoId (PTP_SDOID[11:0]). When this bit is set, majorSdoId and minorSdoId range checking is used. The majorSdoId and minorSdoId fields are concatenate and treated as a 12 bit value. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
14:12	**RESERVED**	RO	—
11:0	**PTP SdoId (PTP_SDOID[11:0])** **PTP SdoId Lower Range (PTP_SDOID_LO[11:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN). This field contains the PTP SdoId in use. Each bit may be masked using the PTP SdoId Mask field. This field contains the PTP SdoId range lower limit. This field is used along with the PTP SdoId upper limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.199 PTP TX SDOID MASK / SDOID RANGE UPPER REGISTER (PTP_TX_SDOID_MASK_SDOID_UP)

Index (In Decimal): 2.442 Size: 16 bits

This register is used to configure PTP receive message timestamping and modification.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:0	**PTP SdoId Mask (PTP_SDOID_MASK[11:0])** **PTP SdoId Upper Range (PTP_SDOID_UP[11:0])** This field has two uses based on the PTP SdoId Range Enable (PTP_SDOID_RANGE_EN) This field contains the PTP SdoId Mask. 0 : bit is ignored (considered a match) 1 : bit is compared This field contains the PTP SdoId range upper limit. This field is used along with the PTP SdoId range lower limit field. Values are inclusive. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000h

5.2.200 PTP TX TIMESTAMP ENABLE REGISTER (PTP_TX_TIMESTAMP_EN)

Index (In Decimal): 2.443 Size: 32 bits

This register is used to enable PTP transmit message timestamping.

Bits	Description	Type	Default
15:0	**PTP Message Type Enable (PTP_MESSAGE_EN[15:0])** These bits individually enable timestamping of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled	R/W	0000h

5.2.201 PTP TX TIMESTAMP CONFIGURATION REGISTER (PTP_TX_TIMESTAMP_CONFIG)

Index (In Decimal): 2.444 Size: 32 bits

This register is used to configure PTP transmit message timestamping and modification.

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3	**PTP Allow UDPv6 Zero Checksum (PTP_UDPV6_ZERO_CHKSUM_EN)** When this bit is set, a zero checksum value for IPv6/UDP frames is considered valid. **Note:** If PTP_UDP_CHKSUM_DIS is set then this bit does not matter since checksum testing is overridden. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2	**PTP Alternate Master Enable (PTP_ALT_MASTER_EN)** When this bit is set, the alternateMasterFlag in the PTP message is checked for a zero value. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
1	**PTP UDP Checksum Check Disable (PTP_UDP_CHKSUM_DIS)** When this bit is cleared, egress times are not saved if the frame has an invalid UDP checksum. When this bit is set, the UDP checksum check is bypassed and the egress time is saved regardless. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**PTP FCS Check Disable (PTP_FCS_DIS)** When this bit is cleared, egress times are not saved if the frame has an invalid FCS. When this bit is set, the FCS check is bypassed. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.202 PTP TX MODIFICATION REGISTER (PTP_TX_MOD)

Index (In Decimal): 2.445 Size: 16 bits

This register is used to configure TX PTP message modifications.

Bits	Description	Type	Default
15	**PTP Clear One Byte Reserved Field (PTP_CLR_1_RSVRD)** This bit enables the clearing of the one byte reserved field.	R/W	0b
14	**PTP Clear Four Byte Reserved Field (PTP_CLR_4_RSVRD)** This bit enables the clearing of the four byte reserved field.	R/W	0b
13	**PTP Pdelay_Resp Message Turnaround Time Insertion (PTP_PDRESP_TA_INSERT)** This bit enables the turnaround time between the received Pdelay_Req and the transmitted Pdelay_Resp to be inserted into the correctionfield of the Pdelay_Resp message sent by the Host.	R/W	0b
12	**PTP Sync Message Egress Time Insertion (PTP_SYNC_TS_INSERT)** This bit enables the egress time to be inserted into the originTimestamp field of Sync messages sent by the Host.	R/W	0b
11	**PTP Follow_Up Message Egress Time Insertion (PTP_FOLLOWUP_TS_INSERT)** This bit enables the egress time of the preceding Sync message to be inserted into the preciseOriginTimestamp field of the Follow_Up message sent by the Host.	R/W	0b
10	**PTP Pdelay_Resp Message Egress Time Insertion (PTP_PDRESP_TS_INSERT)** This bit enables the ingress time of the preceding Pdelay_Req message to be inserted into the requestReceiptTimestamp field of the Pdelay_Resp message sent by the Host.	R/W	0b
9	**PTP Pdelay_Resp_Follow_Up Message Egress Time Insertion (PTP_PDRESPFOLLOWUP_TS_INSERT)** This bit enables the egress time of the preceding Pdelay_Resp message to be inserted into the responseOriginTimestamp field of the Pdelay_Resp_Follow_Up message sent by the Host.	R/W	0b
8	**PTP Pdelay_Resp_Follow_Up Message Turnaround Time Insertion (PTP_PDRESPFOLLOWUP_TA_INSERT)** This bit enables the turnaround time between the received Pdelay_Req and the transmitted Pdelay_Resp to be inserted into the correctionfield of the Pdelay_Resp_Follow_Up message sent by the Host.	R/W	0b
7:5	**RESERVED**	RO	—
4	**PTP Bad UDPv6 Checksum Force FCS Disable (PTP_BAD_UDPV6_CHKSUM_FORCE_FCS_DIS)** When this bit is cleared, IPv6 egress packets that have an invalid UDP checksum will have a bad FCS forced if the packet is modified for timestamp or correction field reasons. When this bit is set, the UDP checksum check is bypassed. **Note:** This field should normally be left at its default value of 1 so that FCS errors are not forced. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b

Bits	Description	Type	Default
3	**PTP Bad UDPv4 Checksum Force FCS Disable (PTP_BAD_UDPV4_CHKSUM_FORCE_FCS_DIS)** When this bit is cleared, IPv6 egress packets that have an invalid UDP checksum will have a bad FCS forced if the packet is modified for timestamp or correction field reasons. When this bit is set, the UDP checksum check is bypassed. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2:0	**RESERVED**	RO	—

5.2.203 PTP TX RESERVED BYTES CONFIGURATION REGISTER (PTP_TX_RSVD_BYTE_CFG)

Index (In Decimal): 2.446 Size: 16 bits

This register is used to configure the location of the reserved bytes inside the TX PTP messages.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11:6	**PTP 4 Reserved Bytes Offset (PTP_4_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header of the four reserved bytes which the transmitter would clear if enabled. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	010000b
5:0	**PTP 1 Reserved Byte Offset (PTP_1_RSVD_OFFSET[5:0])** This field specifies the offset into the PTP header where the transmitter can retrieve the seconds portion of the ingress time. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	000101b

5.2.204 PTP TX TAIL TAG REGISTER (PTP_TX_TAIL_TAG)

Index (In Decimal): 2.447 Size: 16 bits

This register is used to configure tail tagging.

Bits	Description	Type	Default
15:9	**RESERVED**	RO	—
8	**PTP Forward Tail Tag Clipped TX_ER (PTP_FWD_CLIPPED_ER)** 1 : forward TX_ER from clipped portion of frame 0 : ignore TX_ER from clipped portion of frame	R/W	1b
7:4	**PTP Tail Tag Insert Minimum IFG (PTP_TAIL_TAG_INSERT_IFG)** When the PTP_TAIL_TAG_EN and PTP_TAIL_TAG_INSERT bits are set, this field specifies the minimum IFG in bytes to enforces between resultant frames. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	1b
3	**PTP Tail Tag Insert (PTP_TAIL_TAG_INSERT)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that the timestamp is inserted before a new FCS. Otherwise the timestamp replaces the existing FCS without a new FCS. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
2	**PTP Tail Tag All (PTP_TAIL_TAG_ALL)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all frames are to be tail tagged. Otherwise only 1588 messages are tail tagged. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
1	**PTP Tail Tag All 1588 (PTP_TAIL_TAG_ALL_1588)** When the PTP_TAIL_TAG_EN bit is set, this bit, when set, indicates that all 1588 frames are to be tail tagged. Otherwise only those messages enabled via the PTP_TX_TIMESTAMP_EN register are tail tagged. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**PTP Tail Tag Timestamp Enable (PTP_TAIL_TAG_EN)** When this bit is set, the FCS will be replaced by the egress timestamp. **Note:** The host S/W must not change this bit while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.205 PTP TX CORRECTION FIELD MODIFICATION ENABLE REGISTER (PTP_TX_CF_MOD_EN)

Index (In Decimal): 2.448 Size: 16 bits

This register is used to configure TX PTP message correction field modifications.

Bits	Description	Type	Default
15:0	**PTP Correction Field Message Type Enable (PTP_CF_MSG_EN[15:0])** These bits individually enable correction field modification of their respective message types. Bit 0 of this field corresponds to a message type value of 0 (Sync), bit 1 to message type value 1 (Delay_Req), etc. Typically Sync, Delay_Req, Pdelay_Req and Pdelay_Resp messages are enabled	R/W	0000h

5.2.206 PTP TX CORRECTION FIELD CONFIGURATION REGISTER (PTP_TX_CF_CFG)

Index (In Decimal): 2.449 Size: 16 bits

This register is used to configure TX PTP message correction field modifications.

Bits	Description	Type	Default
15:3	**RESERVED**	RO	—
2	**PTP CF 32 Bit Mode (PTP_CF_32BIT)** When residence time correction field adjustments are made using Method A, this bit enables 32 bit mode, where bits 1:0 of the seconds portion of the receive ingress are taken from the upper two bits of the 4 byte reserved field in the PTP message. Otherwise only 30 bits of nanoseconds are used.	R/W	0b
1	**PTP Correction Field Maximum Value Test Disable (PTP_MAX_CF_DIS)** This bit disables the checking for the maximum correction field value of 7FFF_FFFF_FFFF_FFFFh. **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b
0	**PTP Correction Field Method (PTP_CF_METHOD)** This bit determines the method of correction field modification. 0 : Method A - CF_RSVD_4 - ingress time retrieved from 4 reserved bytes 1 : Method B - CF_SUB_ADD_64 - ingress time pre-subtracted from correction field **Note:** The host S/W must not change this field while the PTP Enable (PTP_ENABLE) bit in PTP Command and Control Register (PTP_CMD_CTL) is set.	R/W	0b

5.2.207 PTP TX EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_EGRESS_NS_HI)

Index (In Decimal): 2.450 Size: 16 bits

This read only register combined with the PTP TX Egress Time Seconds High/Low Registers (PTP_TX_EGRESS_SEC_HI/LO) and the PTP TX Egress Time Nanoseconds Low Register (PTP_TX_EGRESS_NS_LO) contains the TX timestamp capture. Up to eight captures are buffered. This register contains the upper 14 bits of the timestamps nanoseconds.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15	**PTP TX Timestamp Valid (PTP_TX_TS_VALID)** This field indicates that the timestamp is valid (there is at least one timestamp available to be read).	RO	0b
14	**RESERVED**	RO	—
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

5.2.208 PTP TX EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_EGRESS_NS_LO)

Index (In Decimal): 2.451 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

5.2.209 PTP TX EGRESS TIME SECONDS HIGH REGISTER (PTP_TX_EGRESS_SEC_HI)

Index (In Decimal): 2.452 Size: 16 bits

This read only register combined with the PTP TX Egress Time Seconds Low Register (PTP_TX_EGRESS_SEC_LO) and the PTP TX Egress Time Nanoseconds High/Low Registers (PTP_TX_EGRESS_NS_HI/LO) contains the TX timestamp captures. Up to eight captures are buffered. This register contains the upper 16 bits of the timestamps seconds.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.210 PTP TX EGRESS TIME SECONDS LOW REGISTER (PTP_TX_EGRESS_SEC_LO)

Index (In Decimal): 2.453 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.211 PTP TX MESSAGE HEADER 1 REGISTER (PTP_TX_MSG_HEADER1)

Index (In Decimal): 2.454 Size: 16 bits

This read only register contains the sourcePortIdentity and messageType of the TX message header. Up to eight captures are buffered.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

Bits	Description	Type	Default
15:4	**Source Port Identity CRC (SRC_PRT_CRC)** This field contains the 12-bit CRC of the sourcePortIdentity field of the transmitted PTP packet.	RO	000h
3:0	**Message Type (MSG_TYPE)** This field contains the messageType field of the transmitted PTP packet.	RO	0h

5.2.212 PTP TX MESSAGE HEADER 2 REGISTER (PTP_TX_MSG_HEADER2)

Index (In Decimal): 2.455 Size: 16 bits

This read only register contains the sequenceId of the TX message header. Up to eight captures are buffered.

Note: Values are only valid if the PTP TX Timestamp Interrupt (PTP_TX_TS_INT) field or the PTP TX Timestamp Valid (PTP_TX_TS_VALID) field is set indicating that at least one timestamp is available.

Reading this register will pop the capture FIFO.

Note: This register may be read without causing a FIFO underflow.

Bits	Description	Type	Default
15:0	**Sequence ID (SEQ_ID)** This field contains the sequenceId field of the transmitted PTP packet.	RO	0000h

5.2.213 PTP TX SYNC EGRESS TIME SECONDS HIGH REGISTER (PTP_TX_SYNC_SEC_HI)

Index (In Decimal): 2.456 Size: 16 bits

This register combined with the PTP TX Sync Egress Time Seconds Mid/Low Registers (PTP_TX_SYNC_SEC_MID/LO) and the PTP TX Sync Egress Time Nanoseconds High/Low Registers (PTP_TX_SYNC_NS_HI/LO) contains the egress time of the last Sync message. This register contains the upper 16 bits of the timestamps seconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[47:32])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.214 PTP TX SYNC EGRESS TIME SECONDS MID REGISTER (PTP_TX_SYNC_SEC_MID)

Index (In Decimal): 2.457 Size: 16 bits

This register contains the middle 16 bits of the timestamps seconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.215 PTP TX SYNC EGRESS TIME SECONDS LOW REGISTER (PTP_TX_SYNC_SEC_LOW)

Index (In Decimal): 2.458 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.216 PTP TX SYNC EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_SYNC_NS_HI)

Index (In Decimal): 2.459 Size: 16 bits

This register combined with the PTP TX Sync Egress Time Seconds High/Mid/Low Registers (PTP_TX_SYNC_SEC_HI/MID/LO) and the PTP TX Sync Egress Time Nanoseconds Low Register (PTP_TX_SYNC_NS_LO) contains the egress time of the last Sync message. This register contains the upper 14 bits of the timestamps nanoseconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**RESERVED**	RO	—
14	**Sync Timestamp Valid (SYNC_TS_VLD)** This field indicates if the TX Sync Egress Time registers are valid. It is automatically set when a Sync message is transmitted. If Follow_Up Message Egress Time Insertion (Two Step Offload) is used, this bit is cleared once the Follow_Up is transmitted.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the transmit egress time.	RO	00000000h

5.2.217 PTP TX SYNC EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_SYNC_NS_LO)

Index (In Decimal): 2.460 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

5.2.218 PTP TX PDELAY_RESP EGRESS TIME SECONDS HIGH REGISTER (PTP_TX_PDRESP_SEC_HI)

Index (In Decimal): 2.461 Size: 16 bits

This register combined with the PTP TX Pdelay_Resp Egress Time Seconds Mid/Low Registers (PTP_TX_PDRESP_SEC_MID/LO) and the PTP TX Pdelay_Resp Egress Time Nanoseconds High/Low Registers (PTP_TX_PDRESP_NS_HI/LO) contains the egress time of the last Pdelay_Resp message. This register contains the upper 16 bits of the timestamps seconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[47:32])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.219 PTP TX PDELAY_RESP EGRESS TIME SECONDS MID REGISTER (PTP_TX_PDRESP_SEC_MID)

Index (In Decimal): 2.462 Size: 16 bits

This register contains the middle 16 bits of the timestamps seconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.220 PTP TX PDELAY_RESP EGRESS TIME SECONDS LOW REGISTER (PTP_TX_PDRESP_SEC_LOW)

Index (In Decimal): 2.463 Size: 16 bits

This register contains the lower 16 bits of the timestamps seconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the seconds portion of the transmit egress time.	RO	0000h

5.2.221 PTP TX PDELAY_RESP EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_PDRESP_NS_HI)

Index (In Decimal): 2.464 Size: 16 bits

This register combined with the PTP TX Pdelay_Resp Egress Time Seconds High/Mid/Low Registers (PTP_TX_PDRESP_SEC_HI/MID/LO) and the PTP TX Pdelay_Resp Egress Time Nanoseconds Low Register (PTP_TX_PDRESP_NS_LO) contains the egress time of the last Pdelay_Resp message. This register contains the upper 14 bits of the timestamps nanoseconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15	**RESERVED**	RO	—
14	**Pdelay_Resp Timestamp Valid (PDRESP_TS_VLD)** This field indicates if the TX Pdelay_Resp Egress Time registers are valid. It is automatically set when a Pdelay_Resp message is transmitted. If Pdelay_Resp_Follow_Up Message Egress Time Insertion (Two Step Offload) or Pdelay_Resp_Follow_Up Message Egress Correction Field Turnaround Time Adjustment (Two Step Offload) is used, this bit is cleared once the Pdelay_Resp_Follow_Up is transmitted.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the nanoseconds portion of the transmit egress time.	RO	00000000h

5.2.222 PTP TX PDELAY_RESP EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_PDRESP_NS_LO)

Index (In Decimal): 2.465 Size: 16 bits

This register contains the lower 16 bits of the timestamps nanoseconds.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the nanoseconds portion of the transmit egress time.	RO	0000h

5.2.223 PTP TX RAW EGRESS TIME SECONDS REGISTER (PTP_TX_RAW_TS_SEC)

Index (In Decimal): 2.466 Size: 16 bits

This register contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter captured at the start of each frame.

Bits	Description	Type	Default
15:0	**LTC Seconds (PTP_LTC_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

5.2.224 PTP TX RAW EGRESS TIME NANOSECONDS HIGH REGISTER (PTP_TX_RAW_TS_NS_HI)

Index (In Decimal): 2.467 Size: 16 bits

This register contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13:0	**LTC Nanoseconds (PTP_LTC_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

5.2.225 PTP TX RAW EGRESS TIME NANOSECONDS LOW REGISTER (PTP_TX_RAW_TS_NS_LO)

Index (In Decimal): 2.468 Size: 16 bits

This register contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter captured at the start of each frame.

Bits	Description	Type	Default
15:0	**LTC Nanoseconds (PTP_LTC_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the 1588 Local Time Counter.	RO	0000h

Note: This value is live.

5.2.226 PTP TX CHECKSUM DROPPED COUNT HIGH REGISTER (PTP_TX_CHKSUM_DROPPED_CNT_HI)

Index (In Decimal): 2.469 Size: 16 bits

This register along with the PTP TX Checksum Dropped Count Low Register (PTP_TX_CHKSUM_DROPPED_CNT_LO) counts the number of egress packets forced to have an FCS error due to a bad original UDP checksum. Since the packet was dropped by forcing an TX error, the packet will also be counted as an error by the receiving MAC. This register contains the upper 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[31:16])** This field is a count of egress packets forced to have an FCS error due to a bad original UDP checksum. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. **Note:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

5.2.227 PTP TX CHECKSUM DROPPED COUNT LOW REGISTER (PTP_TX_CHKSUM_DROPPED_CNT_LO)

Index (In Decimal): 2.470 Size: 16 bits

This register contains the lower 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**Bad Checksum Dropped Count (BAD_CHKSUM_DROPPED_CNT[15:0])** This field is a count of egress packets forced to have an FCS error due to a bad original UDP checksum. **Note:** The counter will stop at its maximum value of FFFF_FFFFh. **Note:** For test purposes, the contents of this counter can be set to any desired value via a write.	RC/W	0000h

5.2.228 PTP TX FRAMES MODIFIED COUNT HIGH REGISTER (PTP_TX_FRMS_MOD_CNT_HI)

Index (In Decimal): 2.471 Size: 16 bits

This register along with the PTP TX Frames Modified Count Low Register (PTP_TX_FRMS_MOD_CNT_LO) counts the number of packets that were modified on egress. This register contains the upper 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**TX Frames Modified Count (TX_FRMS_MOD_CNT[31:16])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

5.2.229 PTP TX FRAMES MODIFIED COUNT LOW REGISTER (PTP_TX_FRMS_MOD_CNT_LO)

Index (In Decimal): 2.472 Size: 16 bits

This register contains the lower 16 bits of the count.

BITS	DESCRIPTION	TYPE	DEFAULT
15:0	**TX Frames Modified Count (TX_FRMS_MOD_CNT[15:0])** **Note:** The counter will roll over its maximum value of FFFF_FFFFh.	RC	0000h

5.2.230 PTP GPIO CAPTURE ENABLE REGISTER (PTP_GPIO_CAP_EN)

Index (In Decimal): 2.496 Size: 16 bits

Note: There are eight sets of rising edge and eight sets of falling edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:8	**GPIO Falling Edge Capture Enable 7-0 (GPIO_FE_CAPTURE_ENABLE[7:0])** These bits enable the falling edge of the respective GPIO input to capture the 1588 Local Time Counter value and to set the respective PTP_GPIO interrupt. 0 : Disables GPIO Capture 1 : Enables GPIO Capture	R/W	00h
7:0	**GPIO Rising Edge Capture Enable 7-0 (GPIO_RE_CAPTURE_ENABLE[7:0])** These bits enable the rising edge of the respective GPIO input to capture the 1588 Local Time Counter value and to set the respective PTP_GPIO interrupt. 0 : Disables GPIO Capture 1 : Enables GPIO Capture	R/W	00h

5.2.231 PTP GPIO CAPTURE LOCK REGISTER (PTP_GPIO_CAP_LOCK)

Index (In Decimal): 2.497 Size: 16 bits

Note: There are eight sets of rising edge and eight sets of falling edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:8	**Lock Enable GPIO Falling Edge (LOCK_GPIO_FE)** These bits enable/disables the GPIO falling edge lock. This lock prevents a 1588 capture from overwriting the Local Time value if the GPIO falling edge interrupt is already set due to a previous capture. 0 : Disables GPIO falling edge lock 1 : Enables GPIO falling edge lock	R/W	FFh
7:0	**Lock Enable GPIO Rising Edge (LOCK_GPIO_RE)** These bits enable/disables the GPIO rising edge lock. This lock prevents a 1588 capture from overwriting the Local Time value if the GPIO rising edge interrupt is already set due to a previous capture. 0 : Disables GPIO rising edge lock 1 : Enables GPIO rising edge lock	R/W	FFh

5.2.232 PTP GPIO X RISING EDGE LTC SECONDS HIGH CAPTURE REGISTER (PTP_GPIO_RE_LTC_SEC_HI_CAP_X)

Index (In Decimal): 2.498 Size: 16 bits

This read only register contains the upper 16 bits of seconds of the GPIO rising edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other 3 rising edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed (“x”) is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of rising edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the upper 16 bits of the seconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.233 PTP GPIO X RISING EDGE LTC SECONDS LOW CAPTURE REGISTER (PTP_GPIO_RE_LTC_SEC_LO_CAP_X)

Index (In Decimal): 2.499 Size: 16 bits

This read only register contains the lower 16 bits of seconds of the GPIO rising edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other 3 rising edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of rising edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.234 PTP GPIO X RISING EDGE LTC NANOSECONDS HIGH CAPTURE REGISTER (PTP_GPIO_RE_LTC_NS_HI_CAP_X)

Index (In Decimal): 2.500 Size: 16 bits

This read only register contains the upper 14 bits of nanoseconds of the GPIO rising edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other 3 rising edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of rising edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Timestamp Input Phase (TS_PHASE)** This bit indicates if the GPIO input occurred in the first or second half of the 1588 reference clock period and can be used to reduce the asynchronous uncertainly. 1 : Input occurred in the first half period 0 : Input occurred in the second half period **Note:** This bit is not valid for a software commanded manual capture.	RO	0b

Bits	Description	Type	Default
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.235 PTP GPIO X RISING EDGE LTC NANOSECONDS LOW CAPTURE REGISTER (PTP_GPIO_RE_LTC_NS_LO_CAP_X)

Index (In Decimal): 2.501 Size: 16 bits

This read only register contains the lower 16 bits of nanoseconds of the GPIO rising edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Rising Edge (LOCK_GPIO_RE) bit is set, a new capture may occur between reads of this and the other 3 rising edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed (“x”) is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of rising edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the timestamp upon the rising edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.236 PTP GPIO X FALLING EDGE LTC SECONDS HIGH CAPTURE REGISTER (PTP_GPIO_FE_LTC_SEC_HI_CAP_X)

Index (In Decimal): 2.502 Size: 16 bits

This read only register contains the upper 16 bits of seconds of the GPIO falling edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_FE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_FE) bit is set, a new capture may occur between reads of this and the other 3 falling edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of falling edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[31:16])** This field contains the upper 16 bits of the seconds portion of the timestamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.237 PTP GPIO X FALLING EDGE LTC SECONDS LOW CAPTURE REGISTER (PTP_GPIO_FE_LTC_SEC_LO_CAP_X)

Index (In Decimal): 2.503 Size: 16 bits

This read only register contains the lower 16 bits of seconds of the GPIO falling edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_FE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_FE) bit is set, a new capture may occur between reads of this and the other 3 falling edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of falling edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:0	**Timestamp Seconds (TS_SEC[15:0])** This field contains the lower 16 bits of the seconds portion of the timestamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.238 PTP GPIO X FALLING EDGE LTC NANOSECONDS HIGH CAPTURE REGISTER (PTP_GPIO_FE_LTC_NS_HI_CAP_X)

Index (In Decimal): 2.504 Size: 16 bits

This read only register contains the upper 14 bits of nanoseconds of the GPIO falling edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_FE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_FE) bit is set, a new capture may occur between reads of this and the other 3 falling edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of falling edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15	**RESERVED**	RO	—
14	**Timestamp Input Phase (TS_PHASE)** This bit indicates if the GPIO input occurred in the first or second half of the 1588 reference clock period and can be used to reduce the asynchronous uncertainly. 1 : Input occurred in the first half period 0 : Input occurred in the second half period **Note:** This bit is not valid for a software commanded manual capture.	RO	0b
13:0	**Timestamp Nanoseconds (TS_NS[29:16])** This field contains the upper 14 bits of the nanoseconds portion of the time-stamp upon the falling edge of a GPIO or upon a software commanded man-ual capture.	RO	0000h

5.2.239 PTP GPIO X FALLING EDGE LTC NANOSECONDS LOW CAPTURE REGISTER (PTP_GPIO_FE_LTC_NS_LO_CAP_X)

Index (In Decimal): 2.505 Size: 16 bits

This read only register contains the lower 16 bits of nanoseconds of the GPIO falling edge timestamp capture.

Note: Values are only valid if the appropriate PTP GPIO Falling Edge Capture Status (PTP_GPIO_FE_STS[7:0]) bit indicates that a timestamp is available.

Note: Unless the corresponding Lock Enable GPIO Falling Edge (LOCK_GPIO_FE) bit is set, a new capture may occur between reads of this and the other 3 falling edge capture registers. Software techniques are required to avoid reading intermediate values.

Note: The GPIO accessed ("x") is set by the GPIO Select (GPIO_SEL[2:0]) field in the PTP GPIO Select Register (PTP_GPIO_SEL).

Note: There are eight sets of falling edge capture registers (x=0 through 7).

Bits	Description	Type	Default
15:0	**Timestamp Nanoseconds (TS_NS[15:0])** This field contains the lower 16 bits of the nanoseconds portion of the time-stamp upon the falling edge of a GPIO or upon a software commanded manual capture.	RO	0000h

5.2.240 PTP GPIO CAPTURE STATUS REGISTER (PTP_GPIO_CAP_STS)

Index (In Decimal): 2.506 Size: 16 bits

This register contains the GPIO capture status bits.

Reading this register clears the interrupt sources.

Bits	Description	Type	Default
15:8	**PTP GPIO Falling Edge Capture Status (PTP_GPIO_FE_STS[7:0])** This interrupt indicates that a falling event occurred and the 1588 Local Time Counter was captured. These bits can also be set due to a manual capture via PTP Manual Capture (PTP_MANUAL_CAPTURE).	RC	00h
7:0	**PTP GPIO Rising Edge Capture Status (PTP_GPIO_RE_STS[7:0])** This interrupt indicates that a rising event occurred and the 1588 Local Time Counter was captured. These bits can also be set due to a manual capture via PTP Manual Capture (PTP_MANUAL_CAPTURE).	RC	00h

5.2.241 PTP GPIO INTERRUPT CLEAR CONFIGURATION REGISTER (PTP_GPIO_INT_CLR_CFG)

Index (In Decimal): 2.507 Size: 16 bits

Bits	Description	Type	Default
15:12	**GPIO PTP Timer Interrupt B Clear Select (GPIO_PTP_TIMER_INT_B_CLEAR_SEL[3:0])** These bits determine which GPIO is used to clear the PTP Timer Interrupt B (PTP_TIMER_INT_B) bit of the PTP Interrupt Status Register (PTP_INT_STS).	R/W	0h
11:10	**RESERVED**	RO	—
9	**GPIO PTP Timer Interrupt B Clear Polarity (GPIO_PTP_TIMER_INT_B_CLEAR_POL)** This bit selects the polarity of the selected GPIO. 0 = active low 1 = active high	R/W	0b
8	**GPIO PTP Timer Interrupt B Clear Enable (GPIO_PTP_TIMER_INT_B_CLEAR_EN)** This bit enables the selected GPIO to clear the PTP Timer Interrupt B (PTP_TIMER_INT_B) bit of the PTP Interrupt Status Register (PTP_INT_STS).	R/W	0b
7:4	**GPIO PTP Timer Interrupt A Clear Select (GPIO_PTP_TIMER_INT_A_CLEAR_SEL[3:0])** These bits determine which GPIO is used to clear the PTP Timer Interrupt A (PTP_TIMER_INT_A) bit of the PTP Interrupt Status Register (PTP_INT_STS).	R/W	0h
3:2	**RESERVED**	RO	—
1	**GPIO PTP Timer Interrupt A Clear Polarity (GPIO_PTP_TIMER_INT_A_CLEAR_POL)** This bit selects the polarity of the selected GPIO. 0 = active low 1 = active high	R/W	0b
0	**GPIO PTP Timer Interrupt A Clear Enable (GPIO_PTP_TIMER_INT_A_CLEAR_EN)** This bit enables the selected GPIO to clear the PTP Timer Interrupt A (PTP_TIMER_INT_A) bit of the PTP Interrupt Status Register (PTP_INT_STS).	R/W	0b

5.2.242 PTP DEBUG BUS SIGNAL GROUP SELECT (PTP_DEBUG_SEL)

Index (In Decimal): 2.510 Size: 16 bits

Bits	Description	Type	Default
15:4	**RESERVED**	RO	—
3:0	**Signal Group Selection (SIG_GROUP_SEL[3:0])** This field is used for debugging to select various signals.	R/W	0h

5.2.243 PCS CONTROL 1 REGISTER

Index (In Decimal): 3.0 Size: 16 bits

Bits	Description	Type	Default
15	**RESET** 1=PCS reset 0=Normal Operation This bit is not used	R/W	0b
14	**Loop Back** 1 = enable loop-back mode 0 = Normal Operation This bit is not used	R/W	0b
13	**RESERVED**	R/W	—
12	**EEE100_idle_sel** 0 = 9031 1 = 8050	R/W	0b
11	**Low power** 1 = low-power-mode 0 = normal operation	R/W	0b
10	**Clock-stop enable** 1 = the PHY may stop the clock during LPI 0 = clock not stoppable	R/W	0b
9:7	**TX FIFO threshold 1000**	R/W	100b
6:4	**TX FIFO threshold 100**	R/W	111b
3:1	**RESERVED**	R/W	—
0	**Dbg_pcs100_sel** 1 = select eee100 RX signals 0 = original	R/W	0b

5.2.244 PCS STATUS 1 REGISTER

Index (In Decimal): 3.1 Size: 16 bits

For the LL and LH bits, if the host reads this register as a new condition corresponding to the same bit occurs, the LL/LH bit will remain cleared/set. If a level event remains asserted, then the corresponding bit will remain cleared/set.

Bits	Description	Type	Default
15:12	**RESERVED**	RO	—
11	**TX LPI received** 1 = TX PCS has received LPI 0 = LPI not received	RO/LH	0b
10	**RX LPI received** 1 = RX PCS has received LPI 0 = LPI not received	RO/LH	0b
9	**TX LPI indication** 1 = TX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
8	**RX LPI indication** 1 = RX PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO	0b
7	**Fault** 1 = Fault condition detected 0 = No fault condition detected	RO	0b
6	**Clock stop capable** 1 = The MAC may stop the clock during LPI 0 = Clock not stoppable	RO	1b
5:3	**RESERVED**	RO	—
2	**PCS receive link status** 1 = PCS receive link up 0 = PCS receive link down	RO	0b
1	**Low-power ability** 1 = PCS supports low-power mode 0 = PCS does not support low-power mode	RO	Note 5-17
0	**RESERVED**	RO	—

Note 5-17 This bit is a 1 if either the 1000BASE-T EEE or 100BASE-TX EEE bit in the EEE Advertisement Register is set. Otherwise it is a 0.

5.2.245 EEE QUIET TIMER REGISTER

Index (In Decimal): 3.8 Size: 16 bits

Bits	Description	Type	Default
15:0	**Quiet-Timer** 1G-EEE quieter Timer Max Value	R/W	006Eh

5.2.246 EEE UPDATE TIMER REGISTER

Index (In Decimal): 3.9 Size: 16 bits

Bits	Description	Type	Default
15:0	**Update-Timer** 1G-EEE Update Timer Max Value	R/W	005Fh

5.2.247 EEE LINK-FAIL TIMER REGISTER

Index (In Decimal): 3.10 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**Link-Fail-Timer** 1G-EEE Link-Fail Timer Max Value	R/W	5Ah

5.2.248 EEE POST-UPDATE TIMER REGISTER

Index (In Decimal): 3.11 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**Post-Update-Timer** 1G-EEE Post-Update Timer Max Value	R/W	50h

5.2.249 EEE WAITWQ TIMER REGISTER

Index (In Decimal): 3.12 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**WaitWQ-Timer** 1G-EEE WaitWQ Timer Max Value	R/W	5Bh

5.2.250 EEE WAKE TIMER REGISTER

Index (In Decimal): 3.13 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**Wake-Timer** 1G-EEE Wake Timer Max Value	R/W	89h

5.2.251 EEE WAKETX TIMER REGISTER

Index (In Decimal): 3.14 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**WakeTX-Timer** 1G-EEE WakeTX Timer Max Value	R/W	1Fh

5.2.252 EEE WAKEMZ TIMER REGISTER

Index (In Decimal): 3.15 Size: 16 bits

Bits	Description	Type	Default
15:8	**RESERVED**	R/W	—
7:0	**WakeMz-Timer** 1G-EEE WakeMz Timer Max Value	R/W	6Eh

5.2.253 EEE CONTROL AND CAPABILITY REGISTER

Index (In Decimal): 3.20 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	RO	—
13	**100GBASE-R deep sleep** 1 = EEE deep sleep is supported for 100GBASE-R 0 = EEE deep sleep is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
12	**100GBASE-R fast wake** 1 = EEE fast wake is supported for 100GBASE-R 0 = EEE fast wake is not supported for 100GBASE-R **Note:** The device does not support this mode.	RO	0b
11:10	**RESERVED**	RO	—
9	**40GBASE-R deep sleep** 1 = EEE deep sleep is supported for 40GBASE-R 0 = EEE deep sleep is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b
8	**40GBASE-R fast wake** 1 = EEE fast wake is supported for 40GBASE-R 0 = EEE fast wake is not supported for 40GBASE-R **Note:** The device does not support this mode.	RO	0b
7	**RESERVED**	RO	—
6	**10GBASE-KR EEE** 0 = EEE is not supported for 10GBASE-KR. 1 = EEE is supported for 10GBASE-KR. **Note:** The device does not support this mode.	RO	0b

Bits	Description	Type	Default
5	**10GBASE-KX4 EEE** 0 = EEE is not supported for 10GBASE-KX4. 1 = EEE is supported for 10GBASE-KX4. **Note:** The device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = EEE is not supported for 10GBASE-KX. 1 = EEE is supported for 10GBASE-KX. **Note:** The device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = EEE is not supported for 10GBASE-T. 1 = EEE is supported for 10GBASE-T. **Note:** The device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = EEE is not supported for 1000BASE-T. 1 = EEE is supported for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = EEE is not supported for 100BASE-TX. 1 = EEE is supported for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	—

5.2.254 EEE WAKE ERROR COUNTER REGISTER

Index (In Decimal): 3.22 Size: 16 bits

Bits	Description	Type	Default
15:0	**EEE Wake Error Counter** This counter is cleared to zeros on read and is held to all ones on overflow.	RC	0000h

5.2.255 EEE 100 TIMER-0 REGISTER

Index (In Decimal): 3.24 Size: 16 bits

Bits	Description	Type	Default
15:8	**TX_SLEEP_TIMER_ADD** tx_sleep_time = (5250 + TX_SLEEP_TIMER_ADD * 32) * 40ns	R/W	00h
7:1	**TX_WAKE_TIMER_ADD** tx_wake_time = (513 + TX_WAKE_TIMER_ADD * 4) * 40ns	R/W	00h
0	**RESERVED**	R/W	0b

5.2.256 EEE 100 TIMER-1 REGISTER

Index (In Decimal): 3.25 Size: 16 bits

Bits	Description	Type	Default
15:8	**RX_SLEEP_TIMER_ADD** rx_sleep_time = (6250 + RX_SLEEP_TIMER_ADD * 32) * 40ns	R/W	00h
7:1	**TX_QUIET_TIMER_ADD** tx_quiet_time = (525000 + TX_QUIET_TIMER_ADD * 8192) * 40ns	R/W	00h
0	**eee_100_test** 1 = force TX LPI	R/W	0b

5.2.257 EEE 100 TIMER-2 REGISTER

Index (In Decimal): 3.26 Size: 16 bits

Bits	Description	Type	Default
15:12	**RX_WAIT_IDLE_EXIT_TIMER_ADD** rx_wait_idle_exit_time = (16 + RX_WAIT_IDLE_EXIT_TIMER_ADD * 2) * 40ns	R/W	0h
11:8	**RX_IDLE_WAIT_TIMER_ADD** rx_idle_wait_time = (20 + RX_IDLE_WAIT_TIMER_ADD * 2) * 40ns	R/W	0h
7:0	**RX_QUIET_TIMER_ADD** rx_quiet_time = (625000 + RX_QUIET_TIMER_ADD * 4096) * 40ns	R/W	00h

5.2.258 EEE 100 TIMER-3 REGISTER

Index (In Decimal): 3.27 Size: 16 bits

Bits	Description	Type	Default
15:8	**RX_WAKE_TIMER_ADD** rx_wake_time = (512 + RX_WAKE_TIMER_ADD * 4) * 40ns	R/W	00h
7:0	**RX_LINK_FAIL_TIMER_ADD** rx_link_fail_time = (2500 + RX_LINK_FAIL_TIMER_ADD * 16) * 40ns	R/W	00h

5.2.259 EEE ADVERTISEMENT REGISTER

Index (In Decimal): 7.60 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	—
13	**100GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR4 deep sleep 1 = Advertise EEE capability for 100GBASE-CR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
12	**100GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KR4 deep sleep 1 = Advertise EEE capability for 100GBASE-KR4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
11	**100GBASE-KP4 EEE** 0 = Do not advertise EEE capability for 100GBASE-KP4 deep sleep 1 = Advertise EEE capability for 100GBASE-KP4 deep sleep **Note:** The device does not support this mode. This bit is not used.	R/W	0b
10	**100GBASE-CR10 EEE** 0 = Do not advertise EEE capability for 100GBASE-CR10 deep sleep 1 = Advertise EEE capability for 100GBASE-CR10 deep sleep **Note:** The device does not support this mode.	R/W	0b
9	**RESERVED**	R/W	—
8	**40GBASE-CR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-CR4 deep sleep 1 = Advertise EEE capability for 40GBASE-CR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
7	**40GBASE-KR4 EEE** 0 = Do not advertise EEE capability for 40GBASE-KR4 deep sleep 1 = Advertise EEE capability for 40GBASE-KR4 deep sleep **Note:** The device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Do not advertise EEE capability for 10GBASE-KR 1 = Advertise EEE capability for 10GBASE-KR **Note:** The device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Do not advertise EEE capability for 10GBASE-KX4 1 = Advertise EEE capability for 10GBASE-KX4 **Note:** The device does not support this mode.	R/W	0b

Bits	Description	Type	Default
4	**10GBASE-KX EEE** 0 = Do not advertise EEE capability for 10GBASE-KX 1 = Advertise EEE capability for 10GBASE-KX **Note:** The device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Do not advertise EEE capability for 10GBASE-T 1 = Advertise EEE capability for 10GBASE-T **Note:** The device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Do not advertise EEE capability for 1000BASE-T 1 = Advertise EEE capability for 1000BASE-T	R/W	1b
1	**100BASE-TX EEE** 0 = Do not advertise EEE capability for 100BASE-TX. 1 = Advertise EEE capability for 100BASE-TX.	R/W	1b
0	**RESERVED**	R/W	—

5.2.260 EEE LINK PARTNER ABILITY REGISTER

Index (In Decimal): 7.61 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	R/W	—
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	RO	0b
9	**RESERVED**	RO	0b
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	RO	0b
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	RO	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	RO	0b

Bits	Description	Type	Default
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	RO	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	RO	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	RO	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	RO	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	RO	0b
0	**RESERVED**	RO	—

5.2.261 EEE LINK PARTNER ABILITY OVERRIDE REGISTER

Index (In Decimal): 7.62 Size: 16 bits

Bits	Description	Type	Default
15	**LP AN Override** 0 = Use Link partner AN results 1 = Use bits 10:0 as Link partner results	R/W	0b
14:11	**RESERVED**	R/W	—
10	**100GBASE-CR10 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 100GBASE-CR10. 1 = Link partner advertises EEE deep sleep capability for 100GBASE-CR10. **Note:** This device does not support this mode.	R/W	0b
9	**RESERVED**	R/W	—
8	**40GBASE-CR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-CR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-CR4. **Note:** This device does not support this mode.	R/W	0b

Bits	Description	Type	Default
7	**40GBASE-KR4 EEE** 0 = Link partner does not advertise EEE deep sleep capability for 40GBASE-KR4. 1 = Link partner advertises EEE deep sleep capability for 40GBASE-KR4. **Note:** This device does not support this mode.	R/W	0b
6	**10GBASE-KR EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KR. 1 = Link partner advertises EEE capability for 10GBASE-KR. **Note:** This device does not support this mode.	R/W	0b
5	**10GBASE-KX4 EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX4. 1 = Link partner advertises EEE capability for 10GBASE-KX4. **Note:** This device does not support this mode.	R/W	0b
4	**10GBASE-KX EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-KX. 1 = Link partner advertises EEE capability for 10GBASE-KX. **Note:** This device does not support this mode.	R/W	0b
3	**10GBASE-T EEE** 0 = Link partner does not advertise EEE capability for 10GBASE-T. 1 = Link partner advertises EEE capability for 10GBASE-T. **Note:** This device does not support this mode.	R/W	0b
2	**1000BASE-T EEE** 0 = Link partner does not advertise EEE capability for 1000BASE-T. 1 = Link partner advertises EEE capability for 1000BASE-T.	R/W	0b
1	**100BASE-TX EEE** 0 = Link partner does not advertise EEE capability for 100BASE-TX. 1 = Link partner advertises EEE capability for 100BASE-TX.	R/W	0b
0	**RESERVED**	R/W	—

5.2.262 EEE MESSAGE CODE REGISTER

Index (In Decimal): 7.63 Size: 16 bits

Bits	Description	Type	Default
15:11	**RESERVED**	R/W	—
10:0	**EEE_message_code** Programmable EEE specific message code for AN	R/W	00Ah

5.2.263 XTAL CONTROL REGISTER

Index (In Decimal): 28.1 Size: 16 bits

Bits	Description	Type	Default
15:14	**RESERVED**	R/W	—
13	**XTAL Disable** Crystal oscillator disable 0 = XTAL enabled 1 = XTAL disabled	R/W NASR	0b
12:0	**RESERVED**	R/W NASR	—

5.2.264 AFED CONTROL REGISTER

Index (In Decimal): 28.9 Size: 16 bits

Bits	Description	Type	Default
15:10	**RESERVED**	RO	—
9	**p_cat3** 0 = cat5 parameter for 10 Base-Te TX 1 = cat3 parameter for 10 Base-T TX	R/W	0b
8:0	**RESERVED**	RO	—

5.2.265 LDO CONTROL REGISTER

Index (In Decimal): 28.14 Size: 16 bits

Bits	Description	Type	Default
15	**LDO enable** turn off VDD regulator by software 1 = off 0 = on	R/W NASR	0b
14:12	**LDO reference tune<2:0>** Tune LDO output voltage @Iload=200mA 000 = 1.097 V 001 = 1.139 V 010 = RESERVED 011 = RESERVED 100 = RESERVED 101 = RESERVED 110 = RESERVED 111 = RESERVED	R/W NASR	000b
11:0	**RESERVED**	R/W	—

5.2.266 EDPD CONTROL REGISTER

Index (In Decimal): 28.36 Size: 16 bits

Bits	Description	Type	Default
15:7	**RESERVED**	RO	—
6	**EDPD Low Power** 0 = EDPD mode disabled 1 = EDPD mode enabled	RO	0b
5:4	**p_edpd_mask_timer[1:0]** 00 = EDPD mask for 2.6us 01 = 3.2us 10 = 4.0us 11 = 5.0us	R/W	00b
3:2	**p_edpd_timer[1:0]** 00 = EDPD pulse separation for 1s 01 = 1.3s 10 = 1.6s 11 = 1.9s	R/W	00b
1	**p_EDPD_random_dis** 1 = use edpd_timer value as EDPD pulse separation selection 0 = use random seed value as EDPD pulse separation selection	R/W	0b

Bits	Description	Type	Default
0	**EDPD Mode Enable** 0 = EDPD mode disabled 1 = EDPD mode enabled	R/W	0b

5.2.267 EMITX CONTROL REGISTER

Index (In Decimal): 28.37 Size: 16 bits

Bits	Description	Type	Default
15:2	**RESERVED**	RO	—
1:0	**p_scale**	RO	00b

5.2.268 EMITX COEFFICIENT REGISTERS

Index (In Decimal): 28.38-52 Size: 16 bits

Register	Bits	Description	Type	Default
38	15	**RESERVED**	RO	—
	14:8	**p_coeff1**	RO	31d
	7	**RESERVED**	RO	—
	6:0	**p_coeff0**	RO	15d
39	15	**RESERVED**	RO	—
	14:8	**p_coeff3**	RO	31d
	7	**RESERVED**	RO	—
	6:0	**p_coeff2**	RO	31d
40	15	**RESERVED**	RO	—
	14:8	**p_coeff5**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff4**	RO	16d

Register	Bits	Description	Type	Default
41	15	**RESERVED**	RO	—
	14:8	**p_coeff7**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff6**	RO	0d
42	15	**RESERVED**	RO	—
	14:8	**p_coeff9**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff8**	RO	0d
43	15	**RESERVED**	RO	—
	14:8	**p_coeff11**	RO	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff10**	RO	0d
44	15	**RESERVED**	RO	—
	14:8	**p_coeff13**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff12**	R/W	0d
45	15	**RESERVED**	RO	—
	14:8	**p_coeff15**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff14**	R/W	0d
46	15	**RESERVED**	RO	—
	14:8	**p_coeff17**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff16**	R/W	0d
47	15	**RESERVED**	RO	—
	14:8	**p_coeff19**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff18**	R/W	0d
48	15	**RESERVED**	RO	—
	14:8	**p_coeff21**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff20**	R/W	0d

Register	Bits	Description	Type	Default
49	15	**RESERVED**	RO	—
	14:8	**p_coeff23**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff22**	R/W	0d
50	15	**RESERVED**	RO	—
	14:8	**p_coeff25**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff24**	R/W	0d
51	15	**RESERVED**	RO	—
	14:8	**p_coeff27**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff26**	R/W	0d
52	15	**RESERVED**	RO	—
	14:8	**p_coeff29**	R/W	0d
	7	**RESERVED**	RO	—
	6:0	**p_coeff28**	R/W	0d

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004784B (01-10-25)	Section 3.1, Register Nomenclature	New section
	Section 5.1.15, PCS Loopback Swap/Polarity Control Register	Renamed table as PCS LOOPBACK SWAP/ POLARITY CONTROL REGISTER. Added bits 7:6 and bit 2.
	Section 5.1.21, Output Control Register	Changed LED Polarity bits 5:0 to RO.
	Section 5.2.69, 1000M Fast Link Down Enable Register	New section
DS00004784A (10-12-22)	Initial release	

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