

MEC142x Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON DEV/REV VALUES

Part Number	Device ID ⁽¹⁾	Device Sub ID ⁽²⁾	Revision ID for Silicon Revision ⁽³⁾	
			A (C0)	B (C1)
MEC1424	0011h	10h	00h	01h
MEC1426	0013h	10h	00h	01h
MEC1428	0015h	10h	00h	01h

Note 1: The Device ID is a 16-bit value. Device ID[15:8] is visible as an 8-bit number at Plug and Play Configuration Index 1Fh. Device ID[7:0] is visible at an 8-bit number at Plug and Play Configuration index 1Eh.

2: The Device Sub ID is an 8-bit number at Plug and Play Configuration Index 1Dh.

3: The Device Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 1Ch.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A (C0)	B (C1)
SMBus 2.0 Host Controller	SMB Master	1.	SMBus Master Controller violates Bus Idle Time between STO and STA in Byte mode only	X	X
UART	LoopBack Test Mode	2.	UART interrupts do not function in loop-back test mode	X	X
ADC	Single Mode	3.	Status bit may not get set after a Power On	X	X
RTOS Timer	RTOS Timer Interrupt	4.	GIRQ24 Bit 3 cannot be used for wake up	X	X
Comparator 0	Comparator 0	5.	Comparator 0 cannot be used		X
eSPI	Flash Channel, SAFS mode, Prefetch	6.	SAFS mode with Prefetch enabled - may return extra bytes if reads don't end on a 64 byte block	X	X
eSPI	Flash Channel, MAFS mode	7.	MAFS mode requires 4-byte SRAM address alignment	X	X
eSPI	Flash Channel, MAFS mode	8.	A 30-second timeout in the MAFS mode configuration routine may cause a platform error.	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

MEC142x

Silicon Errata Issues

1. Module: SMBus 2.0 Host Controller

DESCRIPTION

SMBus Master Controller violates Bus Idle Time between STO and STA in Byte mode only. This issue only occurs in a multi-master environment.

Under firmware control, it is possible to generate a new command on the bus before the Bus Idle time expires, thereby violating the SMBus Idle time.

END USER IMPLICATIONS

The SMBus Master Controller may generate a START condition too soon. The two consequences of this scenario are that another master will issue a transaction that will get clobbered, which is handled by the lost arbitration mechanism, or the MEC142x master will unfairly claim the bus too often.

Work Around

There are two solutions:

- a) Use the Network Layer instead of Byte mode. This anomaly does not apply to the SMBus Network Layer operation.
- b) If firmware polls the nBB bit to indicate not busy before asserting the PIN bit and writing the data register, the SMBus Controller will not violate the Bus Idle time.

2. Module: UART

DESCRIPTION

UART interrupts do not function in loop-back test mode.

Setting bit[4] LOOPBACK in the Modem Control Register at offset 4h enables the internal loop-back feature. However, when internal loop-back mode is enabled the UART interrupt does not get set for Tx or Rx transfers.

END USER IMPLICATIONS

Cannot use internal loop-back mode for testing UART EC interrupts or UART Serial IRQ events.

Work Around

Implement External Loop-Back.

3. Module: ADC

DESCRIPTION

An issue may be seen under certain conditions when using the ADC in Single Mode.

The 'Single_Done_Status' bit in the ADC Control Register may not get set on the first ADC single conversion cycle after a Power On. In this case, the 'Single_Done_Status' will also not be set on subsequent attempts of single ADC conversions.

END USER IMPLICATIONS

The 'Single_Done_Status' bit of ADC Control Register may not set on ADC single conversion cycles after a Power On.

Work Around

Issue an ADC Soft Reset during (after) the first ADC conversion cycle, approximately 2ms after enabling Single Mode (setting the Start_Single bit in the ADC Control Register).

Suggested procedure:

- a) Power On
- b) Set ADC_CONTROL bit [0] = 1 // Activate ADC
- c) Set ADC_SINGLE_REG = 0xNN // Enable appropriate ADC Channels
- d) Set ADC_CONTROL bit [1] = 1 // Start single conversion cycle

- e) Delay 2ms // Wait approx. 2ms
- f) Set ADC_CONTROL bit [4] =1 // ADC Soft Reset
- g) Clear ADC_CONTROL bit [4] =0
- h) Set ADC_CONTROL bit [1] = 1 // Start new conversion cycle.

4. Module: RTOS Timer

DESCRIPTION

The RTOS Timer interrupt, GIRQ24 bit 3, does not function as a wake event.

END USER IMPLICATIONS

The RTOS Timer interrupt, GIRQ24 bit 3, cannot be used to wake the chip up.

Work Around

If the RTOS Timer Interrupt is to be used as a wake event, use RTOS Timer interrupt GIRQ23 bit 4 to wake the chip up.

5. Module: Comparator 0

DESCRIPTION

Comparator 0 is locked disabled and cannot be enabled.

In the COMPARATOR CONTROL register at Offset 18h: Bit 2, Comparator 0 Configuration Locked, defaults to 1 (locked) and bit 0, Comparator 0 Enable, defaults to 0 (disabled).

END USER IMPLICATIONS

Comparator 0 is locked disabled and cannot be used.

Work Around

None.

6. Module: eSPI

DESCRIPTION

The issue involves prefetched flash reads using eSPI SAFS mode. During consecutive prefetch aligned reads (successive reads from consecutive 64-byte aligned Flash addresses), if the second or subsequent read requests less than 64 bytes, the device returns a full 64 bytes of data instead of the number of bytes that was requested.

For example, in the two consecutive flash reads below:

- Read of 64 bytes starting at 0x40
- Read of 24 bytes starting at 0x80

On the second read completion, 64 bytes are returned instead of the requested 24 bytes.

END USER IMPLICATIONS

This may cause a boot failure in a system that is sensitive to the extra data that is returned by the flash read.

Work Around

Do not enable prefetch for eSPI SAFS flash reads in a system that is sensitive to this extra data. Prefetch can be enabled if it can be insured that consecutive prefetch aligned reads that follow the first read will always request 64 bytes. If unsure whether this will be an issue, do not enable prefetch for eSPI SAFS mode.

7. Module: eSPI

DESCRIPTION

All MAFS flash transfers must be to/from 4-byte aligned SRAM buffer starting addresses. The low-order 2 bits of the BUFFER ADDRESS register are reserved and must be written as zeros.

MEC142x

END USER IMPLICATIONS

Customers are required to start all MAFS flash transfers to/from 4-byte aligned SRAM buffer starting addresses.

Work Around

Start MAFS flash transfers to/from 4-byte aligned SRAM buffer starting addresses.

8. Module: eSPI

DESCRIPTION

A 30-second timeout in the MAFS mode configuration routine may cause a platform error on certain platforms, including Gemini Lake (GLK), when booting from the eSPI Flash Channel in MAFS mode.

After driving RSMRST# (the GPIO123/SHD_CS# pin) high, the device will wait up to 30sec for the eSPI Flash channel to be enabled by the eSPI Master; if there is a time-out the part will stop.

END USER IMPLICATIONS

A platform error may occur when booting from the eSPI Flash Channel in MAFS mode, if it takes more than 30sec for the eSPI Flash channel to be enabled by the eSPI Master.

Work Around

None. Rev B (C1) parts do not have this timeout; the Rev B (C1) parts wait indefinitely for the eSPI Flash channel to be enabled by the eSPI Master after driving RSMRST# high when booting from the eSPI Flash Channel in MAFS mode.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the MEC142x data sheet:

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
SMBus	1.	Program Data Timing Register to meet SMBus timing
eSPI Operating Frequency	2.	eSPI mode defaults to 50MHz operation
PWM	3.	Updated PWM Duty Cycle equation
SPI	4.	Shared SPI Flash Chip Select Pull-up Resistor Recommendation
eSPI BAR Init Register	5.	Incorrect Default value

1. Module: SMBus

This is a clarification of the “SMBus Controller Core with Network Layer Support (SMB2) - 16MHz I²C Baud Clock”, Revision 3.52, Core Level Architecture Specification, MCHP, 10/25/13.

The Data Timing Register (Offset 40h) must be programmed to 040A0F01h in order to meet the SMBus timing requirements for Fast Mode.

2. Module: eSPI Operating Frequency

The part defaults to a maximum operating frequency of 50MHz, but it can support 66MHz under user control.

Changing the operating frequency to 66 MHz also requires changing the Drive Strength and Slew Rate fields of the Pin Control Register 2 associated with the eSPI Clock and Data pins to 12mA and fast, respectively.

3. Module: PWM

The PWM Duty Cycle equation is incorrect in the Data Sheet. The correct equation is shown below.

Note that Setting the PWMX_COUNTER_ON_TIME field in the PWMX COUNTER ON TIME REGISTER to a value of n will cause the On time of the PWM to be n+1 cycles of the PWM Clock Source. Setting the PWMX_COUNTER_OFF_TIME field in the PWMX COUNTER OFF TIME REGISTER to a value of n will cause the Off time of the PWM to be n+1 cycles of the PWM Clock Source.

EQUATION 1: PWM DUTY CYCLE EQUATION

$$\text{PWM Duty Cycle} = \frac{(PWMCounterOnTime + 1)}{((PWMCounterOnTime + 1) + (PWMCounterOffTime + 1))}$$

4. Module: SPI

Shared SPI Flash Chip Select Pull-up Resistor Recommendation:

The MEC142x uses the GPIO123/SHD_CS# pin as a strap to determine the boot source (eSPI Flash channel or shared SPI).

In addition, the device uses the GPIO123/SHD_CS# pin as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the GPIO123/SHD_CS# pin on the board if the Shared SPI flash is used so that the SPI_CS# is detected high while RSMRST# is low.

The recommended value of the pull-up resistor on the GPIO123/SHD_CS# pin may vary depending on the version of the Intel PCH that is used.

MEC142x

This is based on information in the current Intel PCH device specifications regarding the SPI0_CS0# pin. This information, as well as the information regarding other PCH devices, must be verified with Intel:

- Skylake PCH LP: the signal is tri-stated with no pull-up or pull-down
 - Use a resistor in the 4.7K-100K range (pulled-up to the 3.3V rail that powers the SPI device)
- Skylake PCH H: the signal is tri-stated with a weak pull down (~ 20K)
 - Use a resistor in the 4.7K-8K range (pulled-up to the 3.3V rail that powers the SPI device).

These pull-up values must be validated in the system (i.e., must guarantee the input level for the MEC14xx device to detect a high is $V_{TR} \cdot 0.7$ as per the data sheet).

5. Module: eSPI BAR Init Register

In the eSPI Controller Specification, the default value of the eSPI BAR Init Register (F4128h) on a RESET_SYS Reset event is shown as 002Eh; the actual default value is 0000h. It also refers to Logical Device Ch for the eSPI I/O Component Configuration Port; this should be Logical Device 10h. See Section 2.8.1.6 eSPI BAR Init Register.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level and Date	Description
DS80000765B (11-30-17)	Updated Revision information in Table 1 and Table 2 to include Cx. Added Silicon Errata Issue 8 .
DS80000765A (10-31-17)	Initial Release

MEC142X

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