AVR354: Using the Deep Under-Voltage Recovery Mode (DUVR)

Features

- **Charging Li-Ion battery cells from 0V without using a pre-charge FET or current limiting resistor.**
- **Current limited charger kept in pre-charge mode by regulating the voltage at the positive battery terminal below fast-charge threshold.**
- **MCU fully operational throughout the charging sequence.**

1 Introduction

Charging Li-ion battery cells from a deeply discharged condition and at the same time keep full control of the charging sequence, is a challenge in many applications. A commonly used method for high-side FET solutions is to apply a pre-charge FET in series with a resistor between the common-drain node of the charge/discharge FETs and the battery cells, as shown in Figure 1-1 for an NFET solution. The charge current is initially supplied through the pre-charge FET until the cell voltage rises to a level where it is safe to switch the charge FET completely ON. Switching on the charge FET with a deeply discharged battery cell will lead to immediate drop in the input voltage to the smart battery device, potentially shutting down the microcontroller.

**Figure 1-1.** Circuit Diagram with pre-charge FET
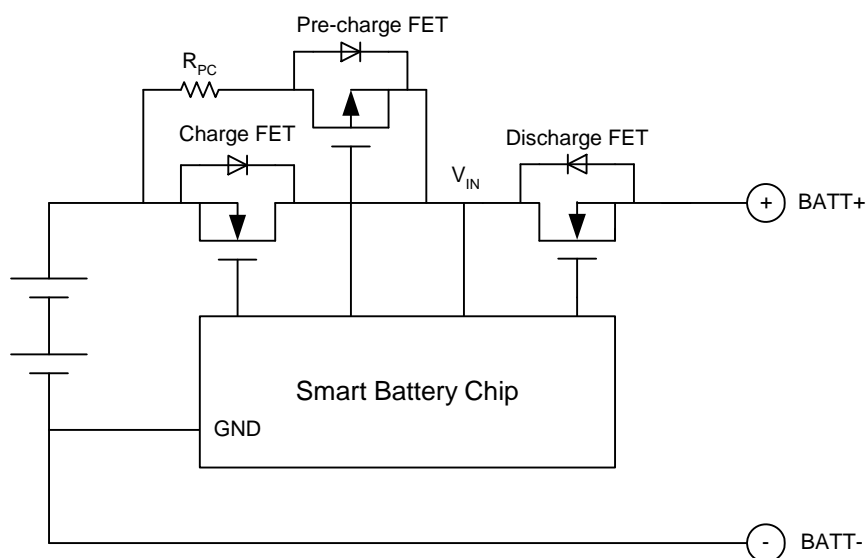
An obvious disadvantage of the scheme presented above, is the extra system cost of the external pre-charge FET and series resistor, and the excessive power dissipated in the external resistor.

2 Charger with current limitation

Many Li-ion battery chargers have a built-in current limitation for pre-charging of deeply discharged cells. The current supplied by the charger is determined by the voltage seen at the positive battery pack terminal, V_{BATT}. If the voltage on the BATT terminal is below a pre-defined (or programmable) fast-charge threshold V_{FC}, the charger will supply a pre-charge current I_{PC}. Above the fast-charge threshold the charger will source a fast-charge current, I_{FC}. A typical I-V characteristic for a charger with current limitation is shown in Figure 2-1. The actual value of V_{FC} must be confirmed for the charger that is used in the application.

The charger usually has a detection time t_{DET} from the battery is inserted in the charger until the charge cycle begins. During this time, the charger supplies a pre-charge current. After t_{DET} has expired, the charger measures the voltage on the BATT terminal before starting the charging sequence. If V_{BATT} is below the fast-charge threshold when t_{DET} expires, this indicates that the cells are deeply discharged, and the charger starts up in the Pre-charge mode. Correspondingly, if the voltage is above the fast-charge threshold, the charger starts up directly in Fast-charge mode.

Figure 2-1. Typical charge current as function of time for a current-limited charger.
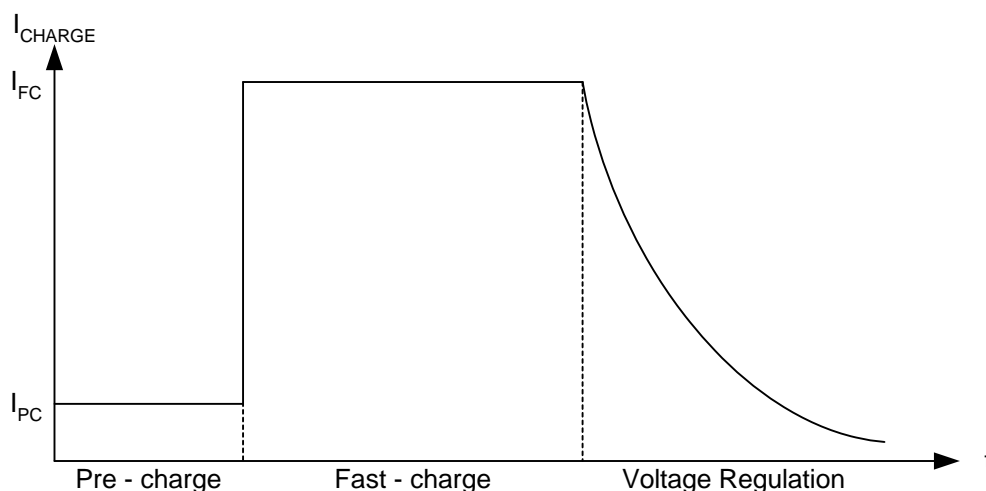
3 Deep Under-Voltage Recovery (DUVR) mode – theory of operation

DUVR mode represents the intelligent pre-charge mode for Atmel's smart battery microcontrollers ATmega16HVA, ATmega8HVA, ATmega8HVD and ATmega4HVD. It is intended for controlled charging of cells even when the cell voltage is below the minimum operating voltage of the chip. The charging is done without using a pre-charge FET or current limiting resistor, and assumes that the charger is current-limited during the pre-charge phase. ATmega16HVA is used as an example in this application note, but unless otherwise noted one can assume that any of the devices can be used. The operating circuit is shown in Figure 3-1.

Figure 3-1. Operating circuit.
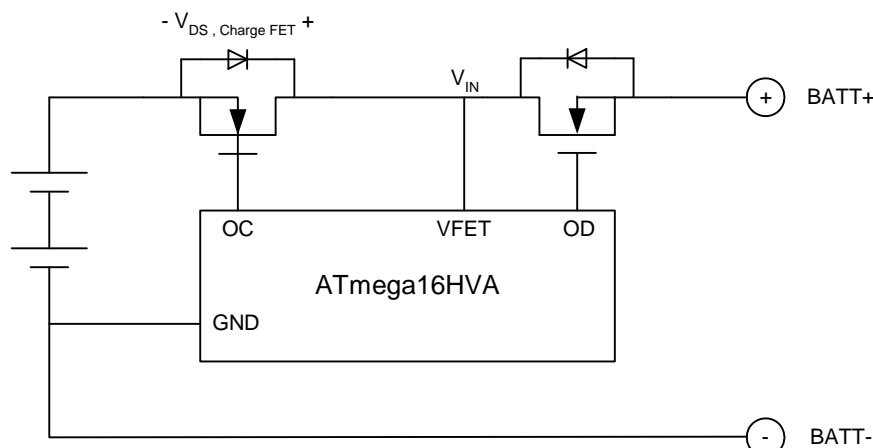
The principle is to keep the VFET node sufficiently high to ensure stable chip operation while keeping the positive battery terminal voltage (V_{BATT}) below the fast-charge threshold of the charger when the cell voltage is low. In DUVR mode the charge FET is completely controlled by autonomous hardware, overriding the software-controlled charge FET Enable (CFE) bit. The charge FET is switched partly ON, and provides a path for the pre-charge current. VFET is regulated at a constant level that is above the minimum operating voltage of the smart battery chip while keeping V_{BATT} below the fast-charge threshold of the charger. This is done by regulating the charge FET resistance to a point that provides a suitable voltage drop ($V_{DS, CFET}$) between VFET and the battery cell.

As the cell voltage increases, $V_{DS, CFET}$ will gradually decrease, and eventually the charge FET is switched completely ON. At this point it is safe to exit DUVR mode as long as software makes sure that the charge FET is enabled (CFE bit is set). A complete application example is given in section 6.

As a safety precaution, the charge FET will always be switched OFF during RESET or if a Battery Protection event has occurred (see data sheet for details on Battery Protection). This functionality is fully autonomous and independent of the DUVR mode operation. The requirement of disabling the charge FET during the RESET mode is the reason why DUVR mode cannot be enabled before the start-up time of the chip has expired. Hence, the smart battery chip provides full safety for the battery pack even though autonomous hardware controls the charge FET in Pre-charge mode.

4 System design considerations

Some important considerations have to be taken into account before using the Deep Under-Voltage Recovery mode. The following subsections contain the information needed to utilize DUVR mode in an optimized way.

4.1 Avoiding premature fast-charge

In order to keep the voltage at the BATT terminal (V_{BATT}) lower than a specified fast-charge threshold during pre-charge, it is important to consider the parameters of the external discharge FET. V_{BATT} in DUVR mode for deeply discharged battery cells can be calculated as specified in Equation 4-1.

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Equation 4-1. Voltage at positive battery pack terminal.
$$V_{BATT} = VFET_{DUVR} + V_B$$

$VFET_{DUVR}$ represents the regulated VFET voltage in DUVR mode for low cell voltages, and V_B is the voltage drop over the body-diode of the discharge FET. Note that the VFET voltage will eventually increase above $VFET_{DUVR}$ when the cell voltage exceeds $VFET_{DUVR}$, so the equation is only valid as long as the cell voltage is low. If the fast-charge threshold of the charger for an application is V_{FC} the maximum allowed body diode drop of the discharge FET is given in Equation 4-2.

Equation 4-2. Maximum allowable DFET body diode voltage drop.
$$V_{B,\,max} = V_{FC} - VFET_{DUVR} - margin$$

Using V_{FC} =3.0V and $VFET_{DUVR}$ =2.1V with 100mV margin, this gives a maximum allowed voltage drop of 800mV over the diode. For pre-charge currents in the order of 100mA, this voltage will never be exceeded for most FETs used in smart battery applications.

In case a discharge FET with high V_B is used, or the fast-charge threshold of the charger is very low, the system may switch on the discharge FET even during pre-charge to eliminate V_B from Equation 4-1.

Opening the discharge FET while charging, may increase the need to check if the charger is still connected. The presence of a charger can easily be measured by monitoring the polarity of the CC-ADC conversion results (ATmega8HVA/16HVA). If a discharge current (or no current) is flowing, this indicates that the charger has been removed and the DFET could be disabled to reduce the risk of the battery cells being drained unintentionally.

The battery cells will be protected from high charge and discharge currents during the complete charging cycle as long as the Battery Protection circuitry is enabled.

4.2 Selecting correct start-up time.

It is important to harmonize the start-up time of the ATmega8HVA/16HVA, and ATmega4HVD/8HVD with the t_{DET} parameter of the charger. This will ensure that the charger never enters Fast-charge mode unintentionally. The start-up time of the microcontroller is mainly determined by the Start-Up Time (SUT) fuse settings. However, some other parameters should also be considered in the system design. The timing values involved in the start-up scheme are listed in Table 4-1.

Table 4-1. System level start-up considerations.

Ref	Parameter	Time[(1)]	Comment
1	Time from charger connected until the internal Power-on Reset is released.	5 ms	Typical value, depending on size of external capacitor CREG.
2	Time from Power-on Reset is released until Internal reset is released	4-512ms	Nominal range, depending on SUT fuse settings. Actual range depends on ULP oscillator frequency.
3	Time from Internal reset is released until DUVR mode is enabled	0 ms	Enabled immediately after reset.
4	Time from DUVR mode enabled until VFET voltage stabilizes at $VFET_{DUVR}$	1ms	Typical value, depending on cell voltage and type of FET.
5	Total time from charger connected to DUVR mode is efficient	10-518 ms	Nominal value depending on SUT fuse settings, calculated as sum of points 1 through 4.

Ref	Parameter	Time[1]	Comment
6	Time from Internal reset is released until discharge FET can be enabled by application code	1ms	Depending on SW implementation.
7	Time from the discharge FET is enabled in application code until VB is reduced	1ms	Typical value, depending on VFET and type of FET.
8	Time from charger connected until VB is reduced	11-519ms	Nominal value depending on SUT fuse settings, calculated as sum of points 1, 2, 6 and 7.

Notes: 1. Values in this column are typical values for a given application. Actual values may deviate from these numbers and must be checked explicitly for each application. For chip parameters that have a minimum and maximum value specified in the data sheet, worst-case considerations should be used if timing is critical.

Once the internal reset is released, DUVR mode is entered as default. For low cell voltages, VFET will stabilize at the $VFET_{DUVR}$ level as soon as the charge FET has been sufficiently switched ON by hardware. For more details on SUT fuse selection and start-up please refer to the datasheet.

The t_{DET} parameter is important to consider in the system design, since V_{BATT} will rise above the fast-charge threshold during start-up. Selecting a start-up time for the smart battery microcontroller that is longer than t_{DET}, may bring the charger into Fast-charge mode too soon.

4.3 Minimizing power consumption

Since DUVR mode is using a clocked regulation scheme to regulate VFET, this mode of operation always requires a fixed, high frequency clock. In practice this means that the Fast RC oscillator of the chip will always be enabled in DUVR mode independent of the various sleep modes of the chip. For the Power Save sleep mode, DUVR mode will increase the power consumption significantly. As long as the charger is connected, the increased power consumption is insignificant. However, the application should make sure to always disable DUVR mode whenever it is not needed to avoid excessive current consumption during battery discharge. This is especially important when using the deep sleep modes.

4.4 Enabling charge FET when cell voltage is too low.

If the charge FET is switched completely ON (charge FET enabled by software) before the cell voltage has reached a level where the chip can operate, VFET drops quickly and the Voltage Regulator can no longer keep the VREG voltage at a sufficient level. For ATmega8/16HVA, the chip enters BOD reset when the VREG voltage drops below the BOD level. The BOD reset immediately switches off the charge FET, causing the VFET voltage to rise again if a charger is present. This causes the chip to recover from BOD reset almost immediately and normal operation can be resumed once the start-up time after reset has elapsed. For ATmega4/8HVD, the chip enters BLOD reset/power off when VREG drops too low.

4.5 Premature charger disconnection /pulse charging

If the charger is using a pulse-charging scheme or for any reason the charger is disconnected when the cell voltage is below the minimum operating voltage of the chip, the device will enter power-off when either VFET or VREG drops too low. When the charger is switched on again, a normal start-up sequence from Power-off will take place.

If the charger is re-connected or the pulse-charging is resumed before VFET or VREG drop below their minimum values, the chip will continue normal operation without entering BOD reset or Power-off.

5 Application example

This section includes an example of a system design including start-up from power-off using the DUVR mode and a current-limited charger. The following assumptions are made:

- Cell voltage (V_{CELL}) is initially 1.0V and the chip is in power-off mode.
- The fast-charge threshold of the charger is 3.0V
- The detection time of the charger, t_{DET} = 60ms
- The body-diode drop of the discharge FET is 0.5V@50mA pre-charge current

Since the body-diode drop of the discharge FET is low compared to the fast-charge threshold (V_{FC}) of the charger, the discharge FET is switched off during initial charging. The start-up time for the microcontroller is set to 32ms to ensure that the positive battery pack terminal is regulated below V_{FC} before the battery is detected.

The charging sequence is illustrated in Figure 5-1. The operating circuit is described in Figure 1-1.

Figure 5-1. Application example (1-cell application).
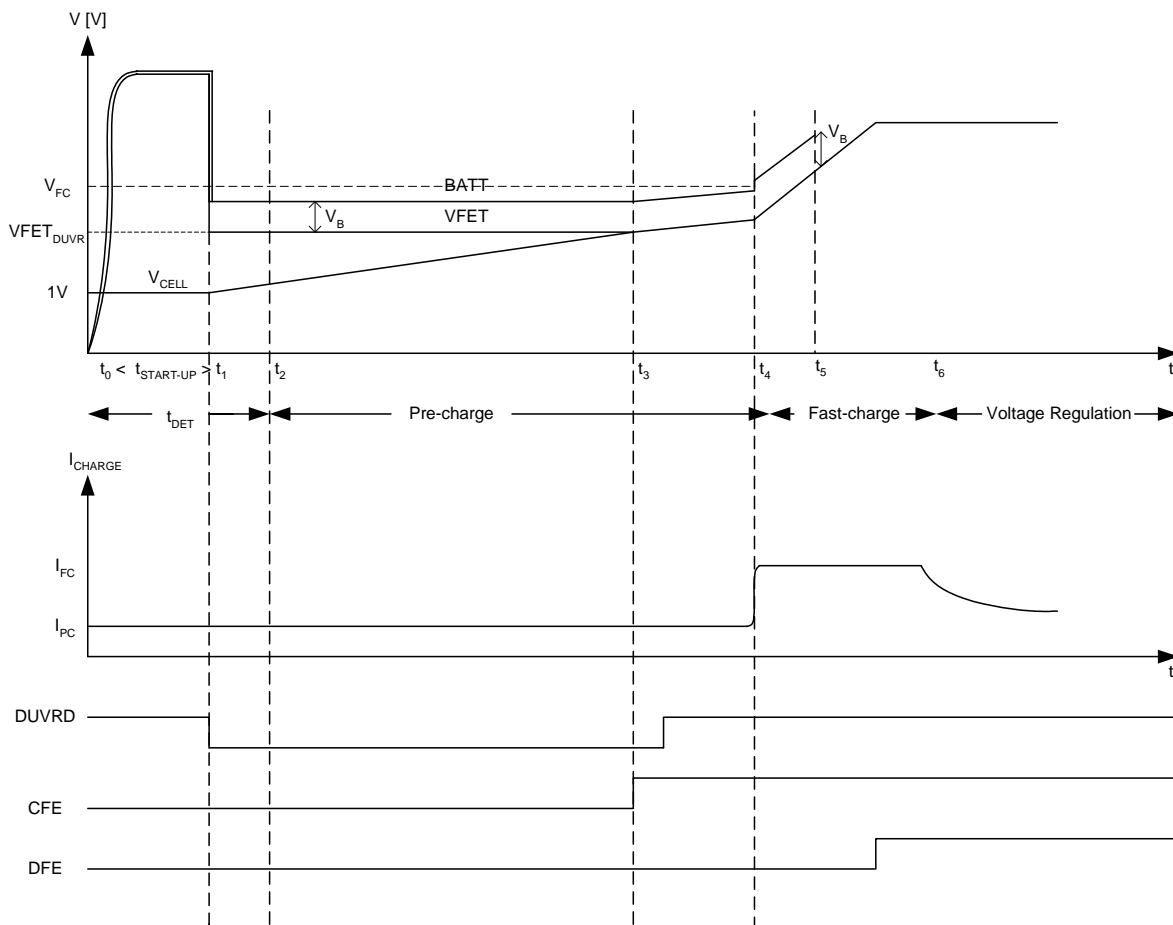
An explanation to the events shown in Figure 5-1 is listed in Table 5-1.

Table 5-1. Explanation to Figure 5-1.

Time	Comment
t=t_0	The charger is connected. Both the charge FET and the discharge FET are switched completely OFF, causing VFET and V_{BATT} to rise quickly towards the battery charger voltage. The device is kept in the RESET state until the start-up time has expired (time indicated as t1). Throughout the RESET period, V_{BATT} is above the V_{FC} threshold. V_{BATT} and VFET are almost equal since the current flowing through the body-diode of the discharge FET is very low.
t=t_1	The start-up time of the microcontroller has elapsed, and the chip exits from RESET state. DUVR mode is enabled automatically and the charge FET is switched partly ON even if the charge FET Enable bit (CFE) is cleared. The enabling of the charge FET causes the VFET voltage to decrease rapidly towards VFET$_{DUVR}$. The BATT voltage equals VFET + V_B and is now well below V_{FC}. The battery cell is being charged through the body-diode of the discharge FET and the drain-source channel of the charge FET.
t=t_2	t_{DET} has expired and the charger measures the V_{BATT} voltage. Since the voltage is well below V_{FC}, the charger continues to apply a pre-charge current. The VFET voltage is kept constant at VFET$_{DUVR}$ while the V_{CELL} increases.
t=t_3	V_{CELL} has increased so that it now equals VFET$_{DUVR}$. In practice, the charge FET is switched completely ON and DUVR mode has no effect anymore. From this point, VFET will follow V_{CELL}, and as it increases, both VFET and V_{BATT} will start to increase. It is now safe to switch ON the charge FET by enabling the CFE bit, and disable DUVR mode. It is important to note that the CFE bit must always be set before DUVR mode is disabled. Failing to comply with this rule will make the VFET voltage drop, potentially causing a Brown-Out (BOD) Reset or power-off in the chip.
t=t_4	V_{BATT} has now reached V_{FC}, and the charger enters the Fast-Charge mode. The voltage over the body-diode of the discharge FET V_B increases as the current increases.
t=t_5	The discharge FET should be switched ON to avoid large power dissipation in the body-diode of the FET. When the FET is switched ON the BATT voltage drops with a voltage corresponding to V_B. Enabling the discharge FET too early may cause V_{BATT} to temporarily drop below V_{FC}. The charger continues to supply a constant fast-charge current until it enters the Voltage regulation phase.
t=t_6	The charger enters Voltage regulation phase and the charge current decreases.

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
avr@atmel.com

Sales Contact
www.atmel.com/contacts

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