Application Note 35

Tracking Bus Termination Voltage Regulators

by Charles Coles

Introduction

This application note presents both low noise linear and high efficiency switch mode solutions for the SSTL type tracking bus termination voltage regulators.

Linear Solutions

This solution for bus termination is a simple, low cost, low noise and ripple, tracking regulator. It is capable of sourcing or sinking up to 5 Amps. The regulator utilizes an operational amplifier to control both the “high side” open loop linear regulator while sourcing current and the “low side” MOSFET when the regulator sinks current.

The DC current rating of the evaluation board is limited thermally to less than 5 Amps. Higher load current can be achieved with additional heatsinking or larger PCB ground plane surface area.

Theory of operation

Source In this circuit the MIC29502 linear regulator is operated open loop. For the condition where the high side regulator is sourcing current, the input to the MIC29502 will remain at 1.24 Volts. Since the open loop gain of the linear regulator is as much as 60dB, very little change will be seen on the error amp output while the regulator is sourcing current. With 1.24 Volts at the adjust pin of the LDO, the low side MOSFET gate voltage will be a diode drop below this at roughly 0.6 Volts. This is a low enough voltage to prevent the MOSFET from conducting while the high side LDO is sourcing current.

Sink The low side MOSFET will begin conducting above 1 Volt at the output of U2. For 1 volt at the output of the error amplifier, the adjust pin of the high side LDO will be forced above the internal reference voltage (1.25 Volts), disabling the high side LDO.

Tracking and Reference

The reference to the error amplifier is developed from the resistive divider and is equal to one half of the input voltage. This forces the output voltage to track one-half of the input voltage. The regulator can be made a non-tracking fixed output by substituting Vref with a fixed voltage.

Typical Applications and Configurations

Various configuration of the circuit are shown in figure 1 through 3. For applications that have an additional bias voltage available such as a 3.3V, 5V, or 12V, figure 3 can be used. This circuit also allows Vddq to be reduced below 2.5 Volts.

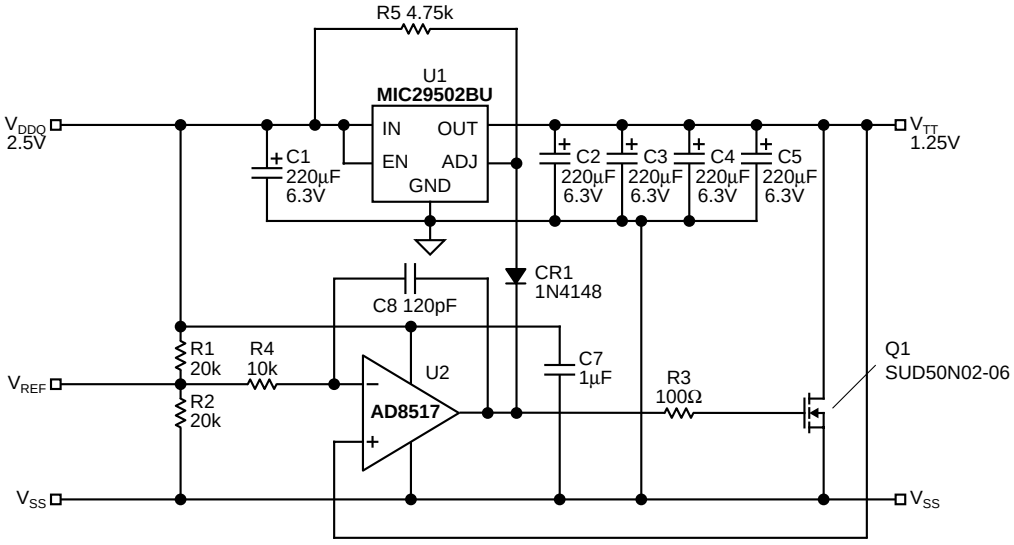


Figure 1. SSTL Bus Termination

Output Capacitor Requirements

Transient response to high-speed logic switching transitions depends largely on layout and bypass capacitor selection. For transient and decoupling considerations refer to the MICRON technical note TB-00-06 for a discussion on important decoupling capacitor characteristics and layout considerations. Very low ESR and ESL capacitors are required at the output for decoupling at frequencies above the bandwidth of the regulator and the bulk energy storage capacitor.

The edges of the logic transitions will be supported by high frequency low ESL MLC capacitors. Typically use only what is necessary to supply the current during the transitions, as more capacitance typically will result in higher inductance. New, low ESL capacitors are available in shapes which minimize inductance for high-speed digital logic transitions. AVX and muRata both have new, low inductance MLC capacitors available and, as mentioned in Micron's application note TB-00-06, the components are typically placed adjacent to the logic device. The bulk capacitance must sustain the voltage following the logic transitions until the regulator can respond and compensate for the droop in the output.

DC Regulation

Any potential difference from the feedback of the error amplifier to the output voltage will result in a DC error in the output voltage. This can be minimized by sensing the output as close as possible to the actual load such that any IR drop in the PCB copper can be compensated for by the regulator. The positive input to the error amplifier is the feedback input. It will typically be an independent Vtt trace sensing Vtt as close as possible to the actual load, avoiding any IR drops in the printed circuit board. The inherent DC gain in the high and low side feedback loops are more than enough to maintain the output within the regulation limits specified in the SSTL standards. So, typical regulation errors will be due to PCB IR drops.

Load Regulation

High Side

The maximum change in the output of the MIC29502 error amplifier is 0.7 Volts. Assuming a DC gain of 40 dB this would require a change to the input to the MIC29502 of 0.7V/100= 0.007 Volts. This would be the change in output voltage required by the error amp U2. Using a DC gain of 60dB for this amplifier, the input voltage change required would be .007V/ 1000=7uV. This is the change that would be seen at the output to accommodate a no-load to full-load change in the MIC29502 Linear Regulator output current. The percentage error is 7uV/1.25V=0.0006%. It is obvious then that the load regulation for the high side driver is dominated by how the output voltage is sensed and PCB layout, not the circuitry involved.

Low Side

The maximum change in the output to the error amplifier in the low side regulation is dictated by the transconductance of the MOSFET QI. Assuming a minimum transconductance of 20 mhOs, a 0.25 V change in the error amp output voltage would be required for a 5 A change in output current (5 A / 20 mhO = 0.25 V). Assuming a 60 dB dc gain for the error amplifier, a 0.25 V change in the error amp output voltage will correspond to a 0.25 V/ 1000 = 0.25 mV change in the input. This percentage error is 0.25 mV/1.25 V = .02%. Again, it is obvious then that the load regulation for the low side driver is going to be dominated by how the output voltage is sensed and PCB layout, not the circuitry involved.

Error Amplifier Offset Voltage

The offset voltage of the error amplifier will cause an additional error in the output voltage, which will be equal to the offset voltage. The worst case offset voltage over temperature for the AD8517 is 5 mV. This correlates to a 5 mV error in the output voltage or an additional 0.4% error.

Table 1 below summarizes the regulation errors with respect to the reference voltage. Any additional errors in the reference voltage can be included as "line regulation" errors.

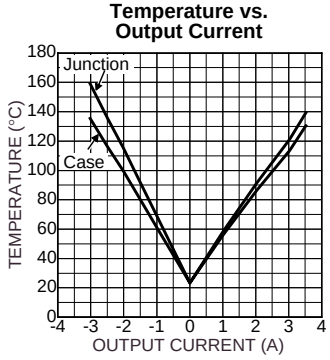
The SSTL specification details a tolerance on V_{TT} with respect to Vref. It does not specify a tolerance on the resistive divider ratio.

$-40 < T_A < 125C$	High Side	Low Side
Load Regulation	0.0006% (7uV)	.02% (0.25mV)
Offsets	0.4% (5mV)	0.4% (5mV)
Total	0.4006% (5.007 mV)	0.402% (5.25 mV)

Table 1

Thermal Characteristics

Figure 8 displays the evaluation board case temperatures of Q1 and U1 versus the load current at room temperature. For the evaluation board the maximum continuous current at room temperature is limited to -2.8A or +3.4 Amps. Higher continuous currents or ambient temperature will require additional heatsinking.



Temperature vs Output Current

Switch Mode Method for generating V_{DDQ} from 3.3V

Figure 4 displays a method for developing Vddq from a 3.3Volt source using the MIC 2182. This design example is capable of 11 Amps output current and requires an additional 5-Volt bias supply. It features current mode control with short circuit protection with high efficiency synchronous rectification.

Bill of Materials

Item	Part Number	Manufacturer	Description	Quantity
C1–C5	TPSD227M006R0100	AVX	220µF ±20%, 6.3V, 100mΩ ESR, tantalum	1
C7	1206YC105MAT2A	AVX	1µF ±10%, 10V, X7R MLC	1
C8	VJ0805121KxxAT	Vitramon	120pF 25V	1
CR1	LL4148	Vishay		1
Q1	SUD50N02-06	Vishay-Siliconix	N-channel MOSFET, 20V, 6mΩ	1
R1, R2	CRCW08052002FRT1	Vishay-Dale	20k ±1%, 1/10W	2
R3	CRCW08051000FRT1	Vishay-Dale	100Ω ±1%, 1/10W	1
R4	CRCW08051002FRT1	Vishay-Dale	10k ±1%, 1/10W	1
R5	CRCW08054751FRT1	Vishay-Dale	4.75k ±1%, 1/10W	1
U1	**MIC29502BU**	**Micrel**	5A low-dropout regulator	1
U2	**AD8517**	**Analog Devices**	high output drive rail-to-rail op amp	1

Vendor	Telephone
Vishay-Dale	(402) 644-4218
Vishay-Siliconix	(408) 988-8000
AVX	(803) 448-9411
Micrel, Inc.	(408) 944-0800

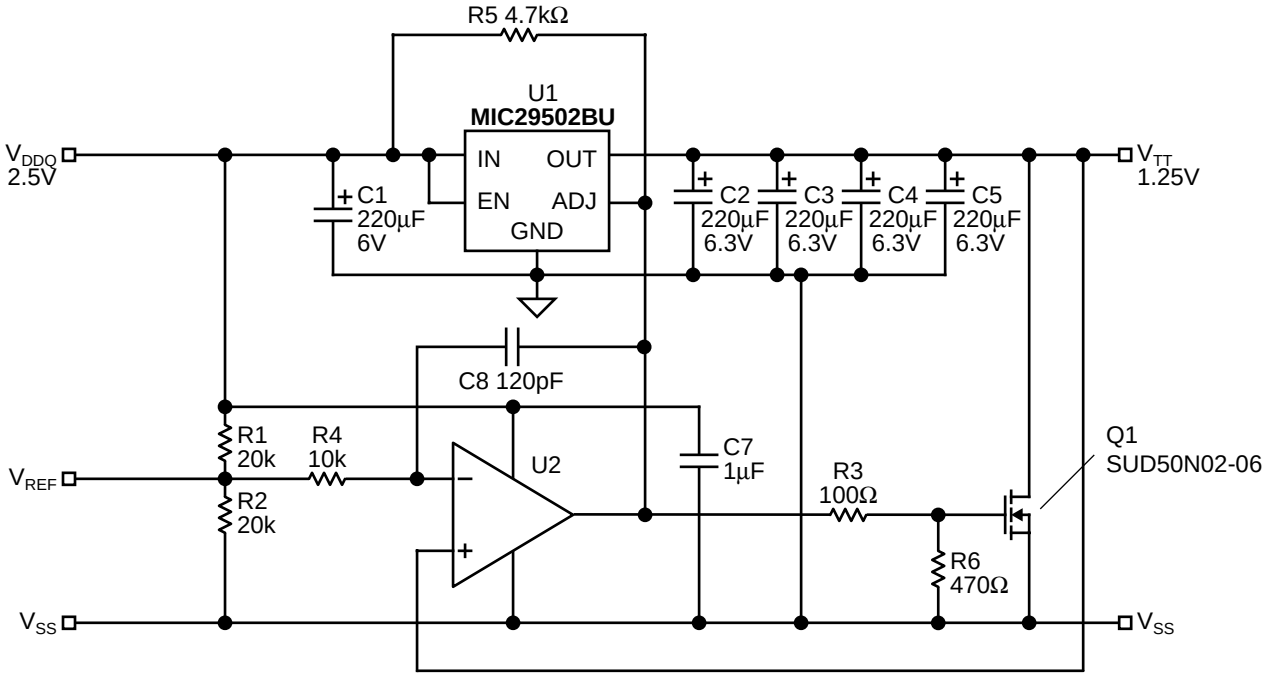


FIgure 2

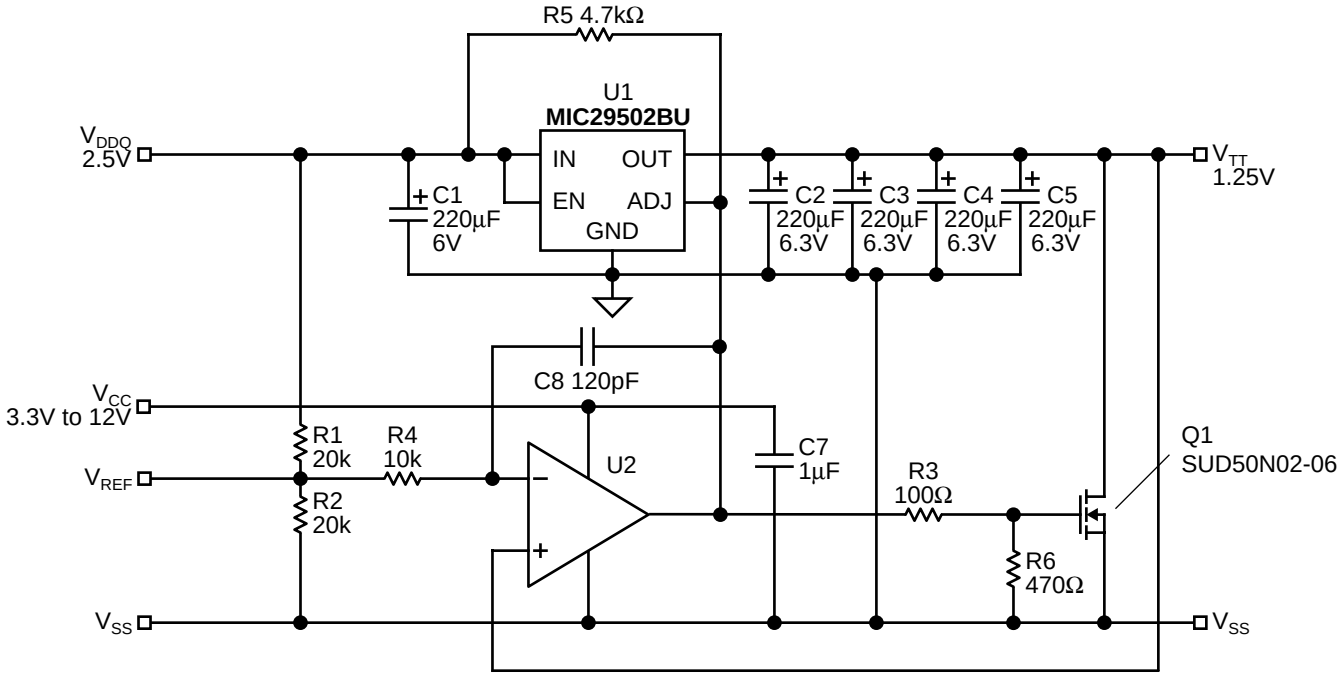


Figure 3

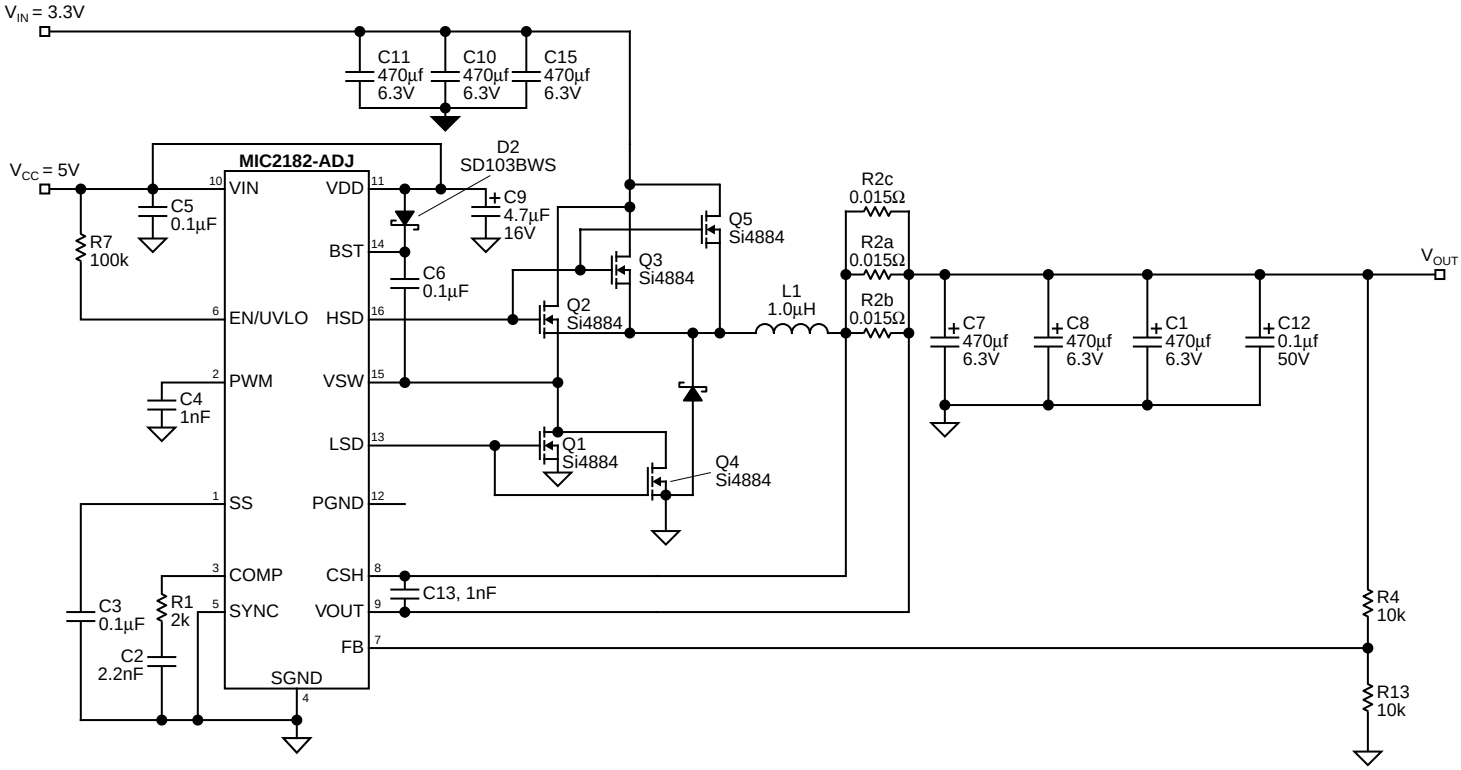


Figure 4. 3.3 to 2.5 Volt conversion

Switchmode Solution

Efficient 10 Amp SSTL Switching Regulator Using the MIC2182

The MIC2182 is versatile synchronous buck (step down) switching regulator controller. With N-channel synchronous output drivers, it has an output current capability of up to 20 Amps. The synchronous output architecture inherently gives it the ability to source or sink load current, lending it for use as a regulator for the termination voltage for SSTL, HSTL, PECL, GTL+, LV-TTL, LV-CMOS, VME, CMOS, Rambus(tm) and other bus interface standards.

Example

An example of the application of the MIC2182 for an SSTL or HSTL application is shown in Figure 5.

Control

Due to the characteristics of the internal current error amplifier it is disabled for this application and operation in confined to PWM voltage mode control by use of the internal PWM ramp already available. The current amplifier is disabled by connecting V_{OUT} and CSH together and tying them both to the input voltage.

Vcc

5 Volts is required for the Vcc to the MIC2182. If it is not readily available, it can be generated from Vddq (2.5 Volts min) by use of the MIC2141/2.

Feedback

For SSTL the output voltage (V_{TT}) of the regulator is forced to track one half the input voltage (V_{DDQ}). Since the reference to the error amplifier is connected internally, it is bypassed and an external error amplifer is used. The MIC2182 error amplifier is a transconductance amplifier with a high output impedance and low output current. Because of this, the input to the amplifier can be shorted, forcing the output of the error amplifier high. The output of the external, low output impedance, high output current feedback error amplifier is then tied directly to pin 3 (COMP).

The reference to the error amplifier is developed from a resistive divider off of the Vddq input voltage.

Bias

For proper bias of the MIC2182 an additional supply rail is required. A 5 Volt 5% regulated supply can be tied directly to pin 11 (VDD). Higher voltages up to 28 Volts should be connected to pin 10 (VIN).

Input Capacitor

An additional high ESR capacitor was added at the input to dampen oscillations due to the high Q nature of the tantalum capacitors at the input.

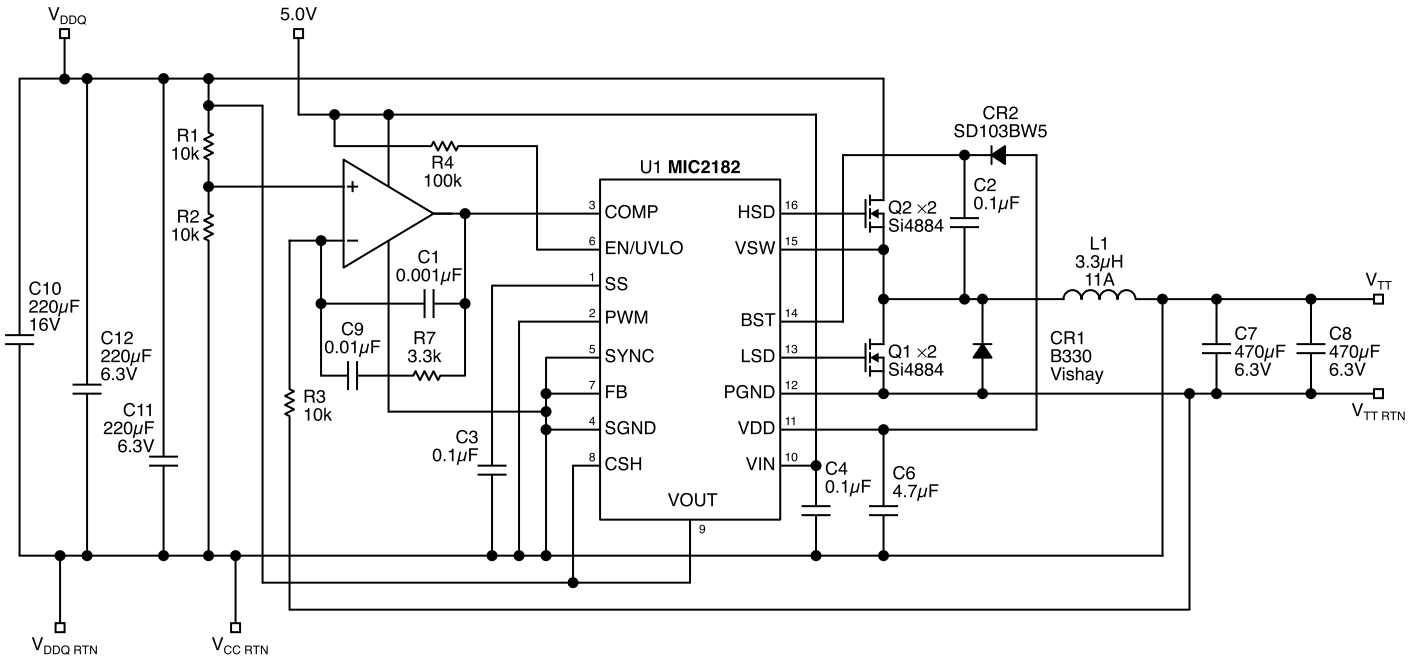
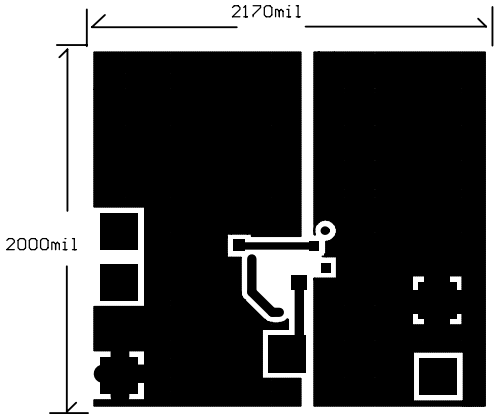
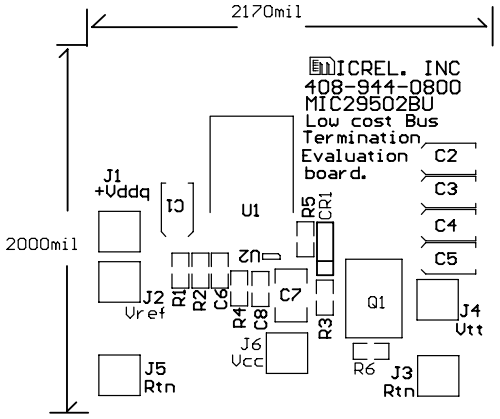


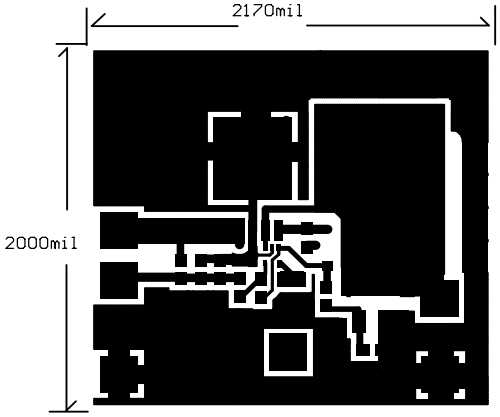
Figure 5. SSTL Bus Terminator



Bottom-Side Copper



Top-Side Silk Screen



Top-Side Copper

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