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Routing Checklist for the LAN9500A, 56-pin QFN Package

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Routing Checklist for LAN9500A

Information Particular for the 56-pin QFN Package

LAN9500A QFN Phy Interface:

1. The traces connecting the transmit outputs (TXP, pin 3) & (TXN, pin 2) to the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

2. The traces connecting the receive inputs (RXP, pin 6) & (RXN, pin 5) from the magnetics must be run as differential pairs. The differential impedance should be 100 ohms.

3. For differential traces running from the LAN controller to the magnetics, SMSC recommends routing these traces on the component side of the PCB with a contiguous digital ground plane on the next layer. This will minimize the use of vias and avoid impedance mismatches by switching PCB layers.

4. The VDD33A power supply should be routed as a mini-plane and can be routed on an internal power plane layer.

LAN9500A QFN Magnetics:

1. The traces connecting the transmit outputs from the magnetics to pins 1 & 2 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

2. The traces connecting the receive inputs on the magnetics from pins 3 & 6 on the RJ45 connector must be run as differential pairs. Again, the differential impedance should be 100 ohms.

3. For differential traces running from the magnetics to the RJ45 connector, SMSC recommends routing these traces on the component side of the PCB with all power planes (including chassis ground) cleared out from under these traces. This will minimize the use of vias and minimize any unwanted noise from coupling into the differential pairs. The plane clear out boundary is usually halfway through the magnetics.

RJ45 Connector:

1. Try to keep all other signals out of the Ethernet front end (RJ45 through the magnetics to the LAN chip). Any noise from other traces may couple into the Ethernet section and cause EMC problems.

2. Also recommended, is the construction of a separate chassis ground that can be easily connected to digital ground at one point. This plane provides the lowest impedance path to earth ground.

+3.3V Power Supply Connections:

1. Route the (5) VDD33IO pins of the LAN9500A QFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

2. In addition, route the (5) VDD33IO decoupling capacitors for the LAN9500A QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

3. Route the (3) VDD33A pins of the LAN9500A QFN directly into a solid, +3.3V power plane. The pin-to-plane trace should be as short as possible and as wide as possible.

4. In addition, route the (3) VDD33A decoupling capacitors for the LAN9500A QFN power pins as short as possible to each separate power pin. There should be a short, direct copper connection as well as a connection to each power plane (+3.3V & digital ground plane) for each cap.

VDDCORE:

1. The VDDCORE pin 21 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap associated with it.

2. The VDDCORE pin 50 must be routed with a heavy, wide trace with multiple vias to the single decoupling cap and the single bulk capacitor associated with it.

3. The two VDDCORE pins 21 & 50 must then be connected together with a short, heavy, wide trace on the PCB. Be sure to use multiple vias as necessary.

4. The VDDPLL pin 10 must be routed with a heavy, wide trace with multiple vias through the ferrite bead to the single decoupling cap and the single bulk capacitor associated with it. The ferrite bead should be supplied through a VDDCORE voltage power plane.

5. The VDDUSBPLL pin 17 must be routed with a heavy, wide trace with multiple vias through the ferrite bead to the single decoupling cap and the single bulk capacitor associated with it. The ferrite bead should be supplied through a VDDCORE voltage power plane.

Ground Connections:

1. The single digital ground pin (pin 57, EDP) on the LAN9500A QFN should be connected directly into a solid, contiguous, internal ground plane. The EDP pad on the component side of the PCB should be connected to the internal digital ground plane with 16 power vias in a 4x4 grid.

2. We recommend that all Ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. The routing for the crystal or clock circuitry should be kept as small as possible and as short as possible.

2. A small ground flood routed under the crystal package on the component layer of PCB may improve the emissions signature. Stitch the flood with multiple vias into the digital ground plane directly below it.

EEPROM Interface:

1. There are no critical routing instructions for the EEPROM interface. Since it is a relatively slow interface, normal board routing measures should suffice.

EXRES Resistor:

1. The EXRES resistor (pin 8) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the EXRES resistor.

USBRBIAS Resistor:

1. The USBRBIAS resistor (pin 16) should be routed with a short, wide trace. Any noise induced onto this trace may cause system failures. Do not run any traces under the USBRBIAS resistor.

Required External Pull-ups/Pull-downs:

1. There are no critical routing instructions for the Required External Pull-ups/Pull-down connections.

MII Interface:

1. The MII interface on the LAN9500A should be constructed using 68-ohm traces.

USB Interface:

1. The USB 2.0 specification requires the USBDP/USBDM (pins 12 & 11) traces to maintain 90 ohm differential trace impedance.
2. The USBDP/USBDM traces should be run over a solid, contiguous ground plane serving as a reference plane.
3. Avoid the use of vias in the USBDP/USBDM traces.
4. Avoid the use of stubs on the USBDP/USBDM traces.
5. Keep all other signals away from the USBDP/USBDM traces.
6. The USBDP/USBDM traces should be matched in length to within 150 mils.
7. The overall USBDP/USBDM trace length should be kept under 6.0”.

Configuration Straps:

1. There are no critical routing instructions for the Configuration Straps of the LAN9500A.

Miscellaneous:

1. SMSC recommends utilizing at least a four-layer design for boards for the LAN9500A QFN device. The design engineer should be aware, however, as tighter EMC standards are applied to his product and as faster signal rates are utilized by his design, the product design may benefit by utilizing up to eight layers for the PCB construction.

2. As with any high-speed design, the use of series resistors and AC terminations is very application dependant. Buffer impedances should be anticipated and series resistors added to ensure that the board impedance matches the driver. Any critical clock lines should be evaluated for the need for AC terminations. Prototype validation will confirm the optimum value for any series and/or AC terminations.

3. Bulk capacitors for each power plane should be routed immediately into power planes with traces as short as possible and as wide as possible.

4. Following these guidelines and other general design rules in PCB construction should ensure a clean operating system.

5. Trace impedance depends upon many variables (PCB construction, trace width, trace spacing, etc.). The electrical engineer needs to work with the PCB designer to determine all these variables.