
Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ8041MLL. These checklist items should be followed when utilizing the KSZ8041MLL in a new design. A summary of these items is provided in [Section 9.0, "Hardware Checklist Summary," on page 10](#). Detailed information on these subjects can be found in the corresponding section:

- [General Considerations on page 1](#)
- [Power on page 1](#)
- [Ethernet Signals on page 3](#)
- [Clock Circuit on page 6](#)
- [Digital Interfaces on page 7](#)
- [Startup on page 8](#)
- [Miscellaneous on page 9](#)

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

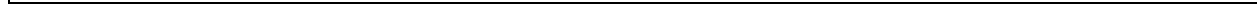
Check the pinout of the part against the data sheet. Ensure all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The GND pins should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

3.0 POWER

- The analog supply, **VDDA_3.3**, requires a connection to **VDDA** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220Ω (at 100 MHz) ferrite bead is used.
- The **VDDA_3.3** pins should include one set of 0.1 μF and 22 μF capacitors to decouple the device. The 22 μF is the bulk capacitor, and the 0.1 μF is the decoupling capacitor for the second **VDDA_3.3** pin. The capacitor size should be SMD_0603 or smaller.
- **VDDIO_3.3** should be connected to the board's +3.3V supply. The **VDDIO_3.3** pin should include one set of capacitors: 22 μF as the bulk capacitor, and the 0.1 μF as the decoupling capacitor for the second **VDDIO_3.3** pin.
- **V1.8_OUT** is used to provide bypassing for the on-chip +1.8V core regulator. This pin requires a 0.1 μF bypass capacitor. This capacitor should be located as close as possible to the pin without using vias. In addition, pin 6 requires a bulk capacitor placed as close as possible to the pin. The bulk capacitor should have a value from 1.0 μF to 2.2 μF, and have an Equivalent Series Resistance (ESR) of no more than 1.0Ω. Microchip recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances, and characteristics are not recommended.
- **V1.8_OUT** should be connected to the **VDD_1.8** pin through a ferrite bead and a 0.1 μF bypass capacitor. **V1.8_OUT** also should be connected to the two **VDDA_1.8** pins through a ferrite bead and a 0.1 μF bypass capacitor.



4.0 ETHERNET SIGNALS

4.1 PHY Interface

- **TX+** (pin 12): This pin is the transmit twisted pair output positive connection from the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 μF capacitor is required on this pin.
- **TX-** (pin 11): This pin is the transmit twisted pair output negative connection from the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 μF capacitor is required on this pin.
- For transmit channel connection and termination details, refer to [Figure 4-1](#).
- **RX+** (pin 10): This pin is the receive twisted pair input positive connection to the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 μF capacitor is required on this pin.
- **RX-** (pin 9): This pin is the receive twisted pair input negative connection to the internal PHY. A 49.9Ω (1.0%) termination resistor AC coupled to the digital ground through a 0.1 μF capacitor is required on this pin.
- For receive channel connection and termination details, refer to [Figure 4-2](#).

FIGURE 4-1: TRANSMIT CHANNEL CONNECTIONS AND TERMINATIONS

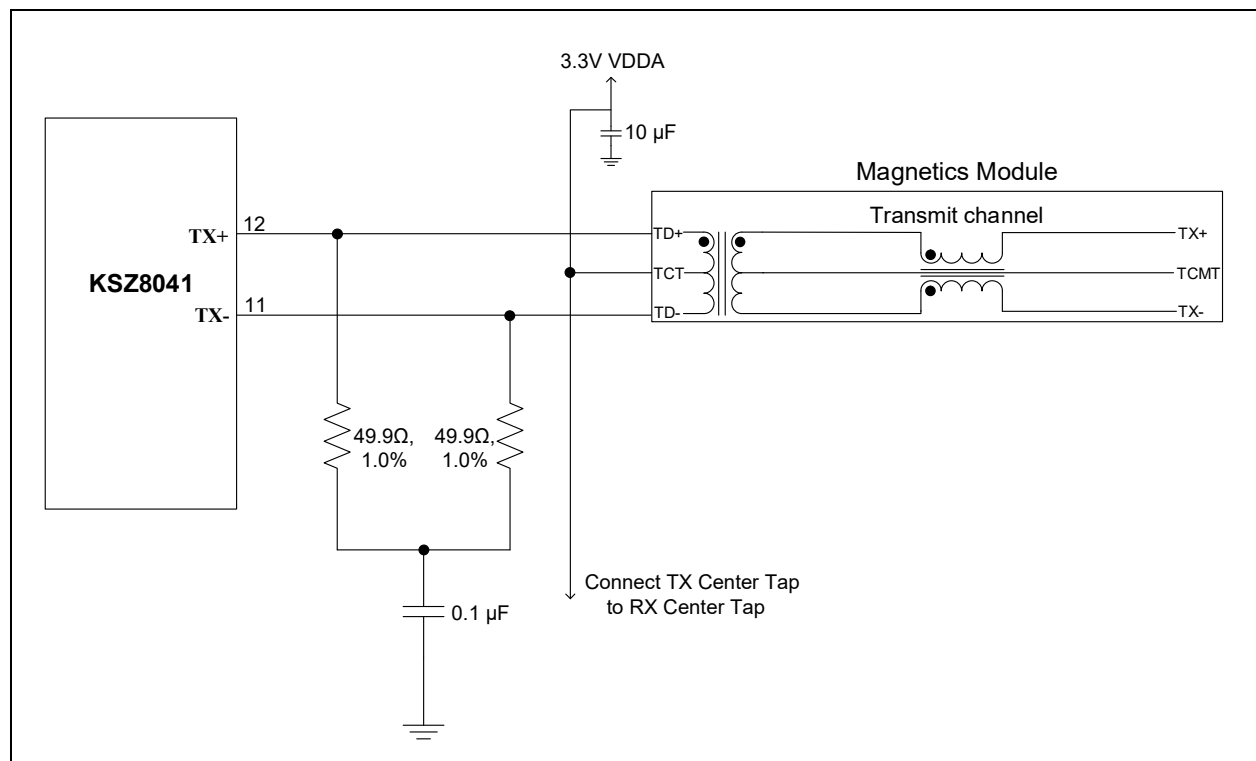
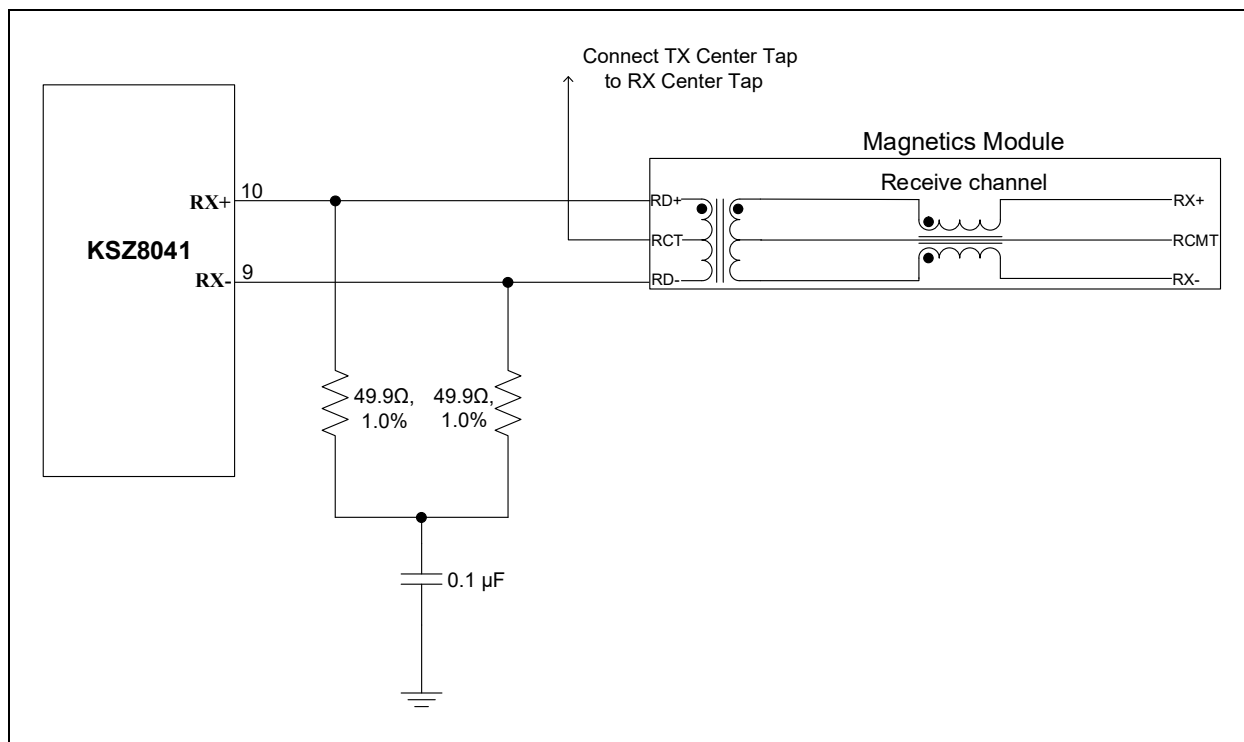


FIGURE 4-2: RECEIVE CHANNEL CONNECTIONS AND TERMINATIONS



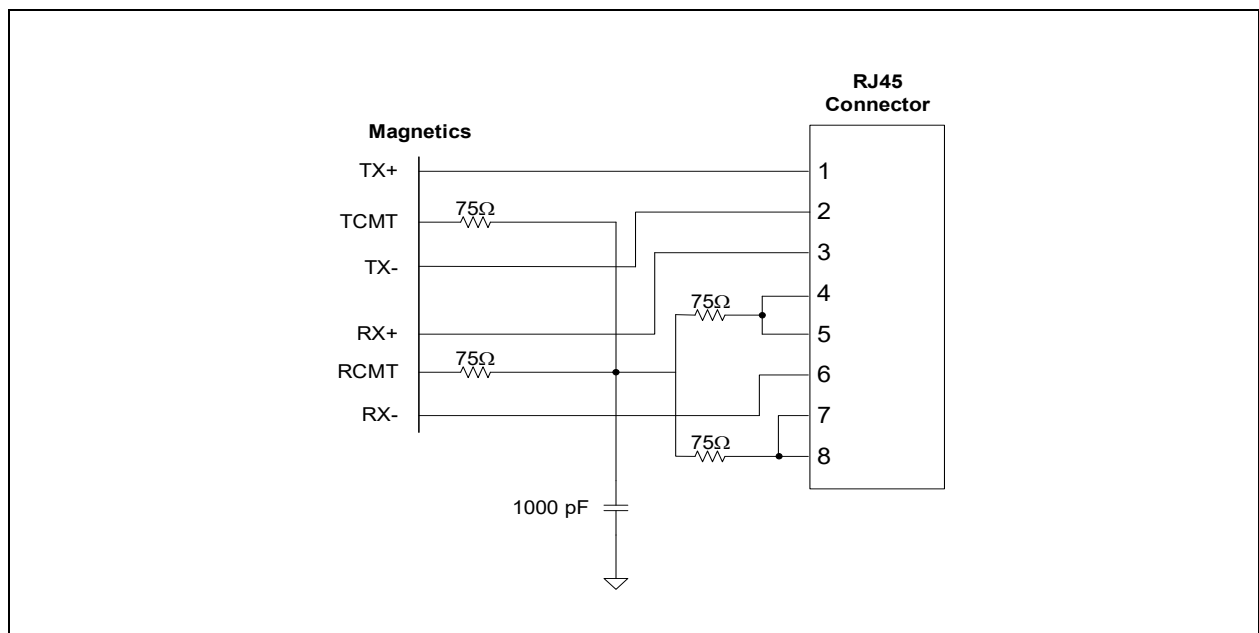
4.2 Magnetics Connection

- The center tap connection on the KSZ8041MLL side for the transmit channel must be connected to **VDDA** (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics. In addition, a 10 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.
- The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both TX and RX center taps.
- Assuming the design of an end-point device (NIC):
 - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to TX+ (pin 12) of the KSZ8041MLL.
 - Pin 2 of the RJ45 is TX- and should trace through the magnetics to TX- (pin 11) of the KSZ8041MLL.
 - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to RX+ (pin 10) of the KSZ8041MLL.
 - Pin 6 of the RJ45 is RX- and should trace through the magnetics to RX- (pin 9) of the KSZ8041MLL.
- When using the device in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module (TX channels and RX channels are symmetrical with each other) is required.

4.3 RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
 - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
 - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
 - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
 - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground.

FIGURE 4-3: RJ45 CONNECTIONS

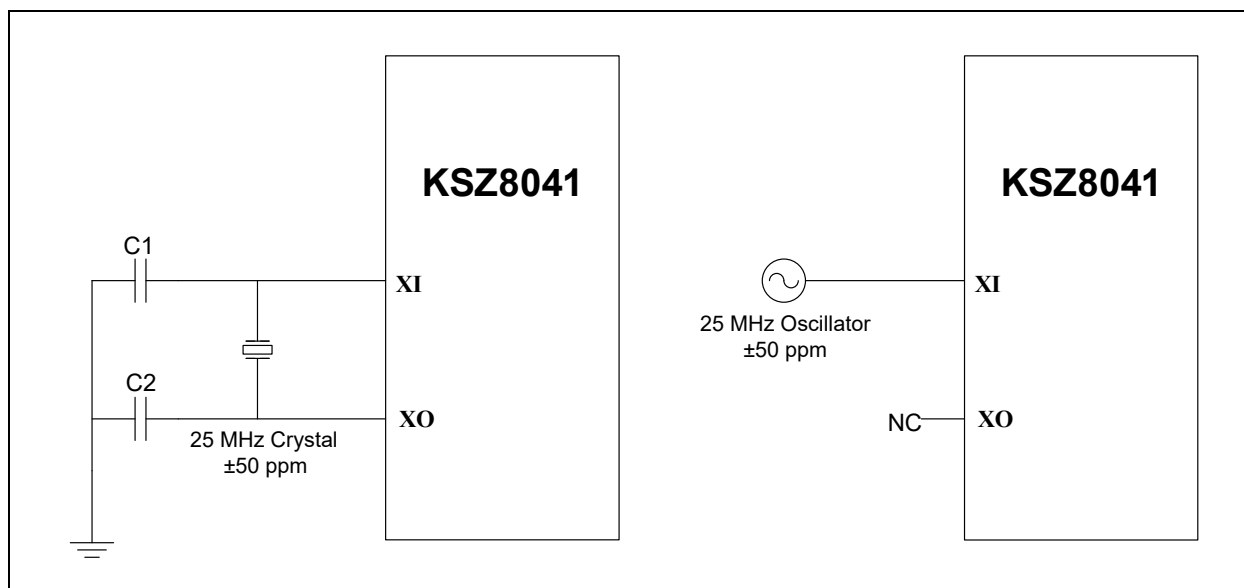


5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections for MII Mode

- When using the KSZ8041MLL in MII mode, a 25.000 MHz (± 50 ppm) crystal should be used to provide the clock source. For exact specifications and tolerances, refer to the latest revision of the *KSZ8041MLL Data Sheet*.
- Alternatively, a 25.000 MHz 3.3V clock oscillator may be used to provide the clock source for the KSZ8041MLL. When using a single-ended clock source, **XO** (pin 14) should be left floating as a No Connect (NC).
- **XI/REFCLK** (pin 15) is the clock circuit input for the KSZ8041MLL device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 14) is the clock circuit output for the KSZ8041MLL device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system-dependent, based on the CL specification of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS FOR MII MODE



6.0 DIGITAL INTERFACES

6.1 MII Interface

- When utilizing either an external MII MAC interface or an MII connector, [Table 6-1](#) indicates the proper connections for the 17 signals, including two management pins (MDC, MDIO).

TABLE 6-1: MII CONNECTIONS

From:	Connects to:
KSZ8041MLL	MII MAC Device
RXD0 (pin 23)	RXD<0>
RXD1 (pin 22)	RXD<1>
RXD2 (pin 21)	RXD<2>
RXD3 (pin 20)	RXD<3>
RXDV (pin 27)	RX_DV
RXER (pin 29)	RX_ER
RXC (pin 28)	RX_CLK
TXD0 (pin 35)	TXD<0>
TXD1 (pin 36)	TXD<1>
TXD2 (pin 38)	TXD<2>
TXD3 (pin 39)	TXD<3>
TXEN (pin 34)	TX_EN
TXC (pin 33)	TX_CLK
CRS (pin 41)	CRS
COL (pin 40)	COL
MDIO (pin 18)	MDIO
MDC (pin 19)	MDC

- The KSZ8041MLL does not provide a TX_ER pin (Transmit error functionality on MII bus). Therefore, the TX_ER contact on the MII connector should be a No Connect (NC). Please visit the MAC interface's data sheet for details on the TX_ER connection.
- Provisions should be made for series terminations for all outputs on the MII interface. Series resistors will enable the designer to closely match the output driver impedance of the KSZ8041MLL and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.
- The series terminations on the TXD0, TXD1, TXD2, TXD3, and TX_EN lines should be placed close to the MAC.
- The series terminations on the TXC, RXC, RXD0, RXD1, RXD2, RXD3, RXDV, RXER, CRS, and COL lines should be placed close to the KSZ8041MLL.

6.2 Required External Pull-Ups

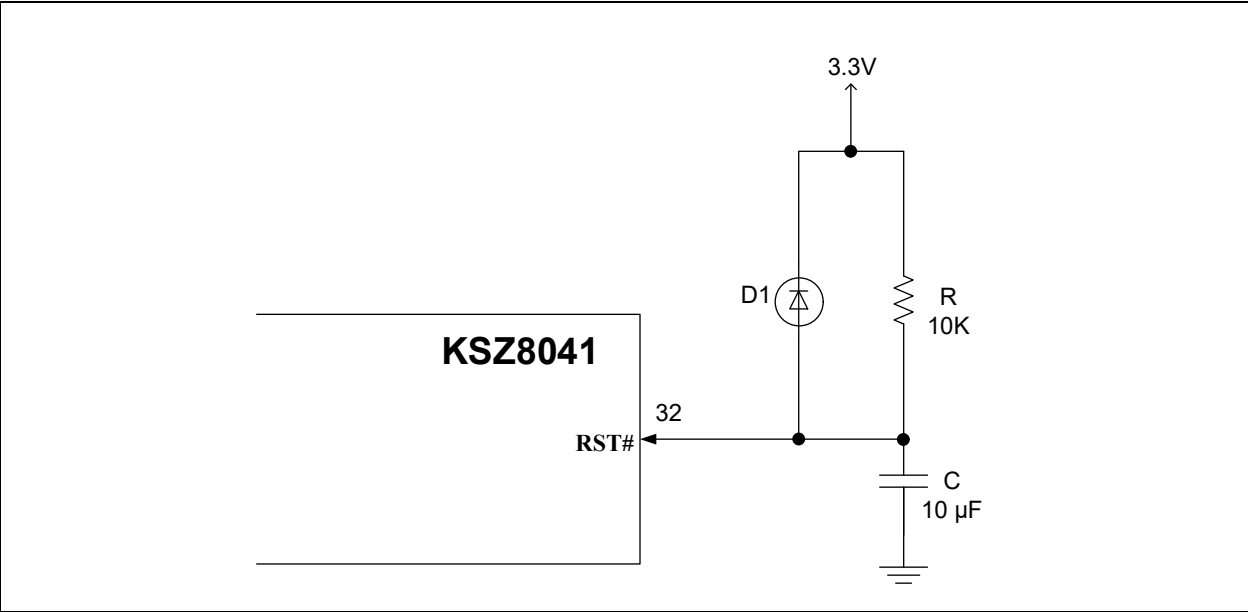
- When using the KSZ8041MLL MDC/MDIO management pins, a pull-up resistor of 4.7 kΩ on the **MDIO** signal (pin 18) is required.
- If used, the **INTRP** (pin 21) requires a 4.7 kΩ external pull-up resistor since this output is an open drain.

7.0 STARTUP

7.1 Reset Circuit

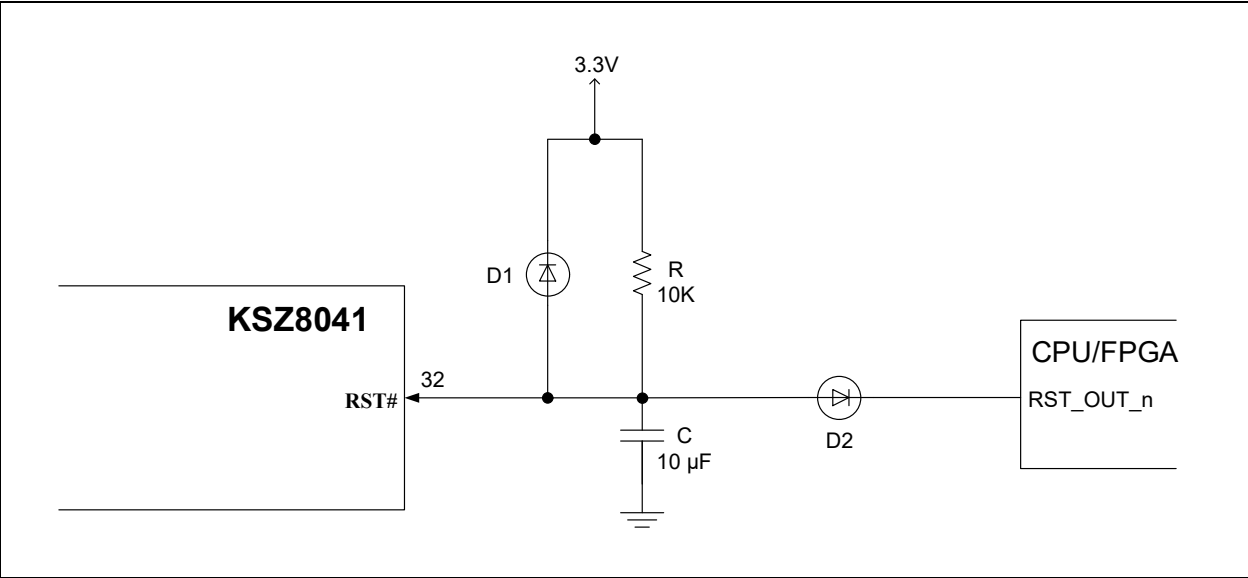
RST# (pin 47) is an active-low reset input. This signal resets all logic and registers within the KSZ8041MLL. A hardware reset (RST# assertion) is required following power-up. Please refer to the latest copy of the *KSZ8041MLL Data Sheet* for reset timing requirements. [Figure 7-1](#) shows a recommended reset circuit for powering up the KSZ8041MLL when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY



[Figure 7-2](#) details the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin (RST_OUT_n) from the CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be directly connected.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



7.2 Strapping Pins

The strapping pins control the configuration, speed, duplex, auto-negotiation, power-down functionality, and PHY address of the KSZ8041MLL. The value of these strapping pins are latched upon power-up and reset. In some systems, the MAC receive input pins may drive high during power-up or reset and consequently cause the PHY strap in pins on the MII/RMII signals to be latched high. In this case (with the exception of speed, duplex, and PHY address bit 0 strapping options), it is recommended to add 1K pull-downs on these PHY strap-in pins to ensure the PHY does not strap in to ISOLATE mode or is not configured with an incorrect PHY address. Refer to the *KSZ8041MLL Data Sheet* for complete details for the operation of these pins.

7.3 LED Pins

- The KSZ8041MLL provides two LED signals. These indicators display speed, link, and activity information about the current state of the PHY. The LED pins drive low to light up the LED indicators, which should have their anode ends tied to 3.3V and their cathode ends tied through a series resistor (typically 220Ω - 470Ω). Refer to the *KSZ8041MLL Data Sheet* for further details on how to connect each pin for correct operation.
- The LED functionality signal pins are shared with the following pin strapping functions:
 - LED0 is shared with **NWAYEN** on pin 42.
 - LED1 is shared with **SPEED** on pin 43.

8.0 MISCELLANEOUS

8.1 REXT Resistor

The **REXT** pin on the KSZ8041MLL should connect to digital ground through a 6.49 kΩ resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the embedded 10/100 Ethernet physical device.

8.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a zero ohm resistor connects them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7-22 μF) for each power plane.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	v	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify pins match the data sheet.		
	Section 2.2, "Ground"	Verify grounds should be tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	- Ensure VDDA_3.3 and VDDIO_3.3 is in the range 3.135V to 3.465V and a 22 μF capacitor is on each pin. - No external 1.8V supply is used, and V1.8_OUT must be wired to VDD_1.8 and VDDA_1.8 with a ferrite bead and caps on each. V1.8_OUT requires a 1.0 μF capacitor.		
Section 4.0, "Ethernet Signals"	Section 4.1, "PHY Interface"	Verify the termination resistors (49.9 Ω , 1.0%) and capacitors (0.1 μ F) on the TX and RX pins.		
	Section 4.2, "Magnetics Connection"	Verify the center taps are connected to the VDDA_3.3 supply on the KSZ8041MLL device side, and are terminated with 75 Ω resistors through a 1000 pF, 2 kV capacitor to chassis ground on the RJ45 line side.		
	Section 4.3, "RJ45 Connector"	Verify pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2 kV capacitor.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections for MII Mode"	Verify usage of 25 MHz $\pm$ 50 ppm crystal.		
Section 6.0, "Digital Interfaces"	Section 6.1, "MII Interface", Section 6.2, "Required External Pull-Ups"	Confirm proper MII signals between MAC and PHY interface with correct termination resistors (33 Ω) and external pull-up for MDIO signal.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 7.2, "Strapping Pins"	In systems where the MAC receive input pins are driven high after reset, it is recommended to add 1 k Ω pull-downs on the PHY strap pins.		
	Section 7.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
Section 8.0, "Miscellaneous"	Section 8.1, "REXT Resistor"	Confirm proper REXT resistor (6.49 k Ω , 1.0%) with a 100 μ F capacitor in parallel.		
	Section 8.2, "Other Considerations"	- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. - Incorporate sufficient power plane bulk capacitors (4.7-22 μF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002856A (11-15-18)	All	Initial release.

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