# ATA6570

## ATA6570 Silicon Errata and Data Sheet Clarification

The functionality of the ATA6570 device that you have received (Revision A1) is described in the current Device Data Sheet, except for the anomalies described in this document.

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|---|---|
| **Note:** | This document summarizes all silicon errata issues from all revisions of silicon with date code 812 or older. In all revisions of silicon with date code 813 or newer, the described errata issue has been fixed. |

### 1. Module: CAN Bus Wake-Up Detection System Initialization

The device does not wake up via the CAN bus (WUP) under the following conditions:

1. The Supply Voltage (VS) rises slowly (dV/dt <~ 1.6V/s) from undervoltage condition ($V_{VS}$ <~ 4.3V) to CAN operation condition ($V_{VS}$ >~ 4.8V).
2. During this rise, $V_{VCC}$ or $V_{VIO}$ are missing.

**The root cause of this behavior is the missing initialization of the CAN bus wake-up detection system**.

1. The device reaches the internal operation supply voltage range at $V_{VS}$ = 4.3V (typical).
2. At this point, the supply voltage for the CAN IP is not yet reached ($V_{VS}$ ≥ 4.8V, typical) and hence, the wake-up detection system is not yet initialized.
3. Due to the missing VIO voltage (and/or VCC voltage), the device is set to Sleep mode after $t_{UV2Sleep}$ (300 ms typical).
4. If $V_{VS}$ rises above 4.8V (typical), the CAN wake-up detection system is enabled and the initialization timer needs to elapse. But the clock for the timer is switched off, because the device is in Sleep mode; hence, no WUP is detected from the control logic. After the Power-on Reset, the clock is initially on and the main FSM is in Standby mode. Due to VIO undervoltage, the device enters Sleep mode and the clock is switched off. Afterwards, the clock is switched on to enable the TX FSM transit from off to standby. After the TX FSM has reached the Standby mode, the clock is switched off again, although the CAN wake-up detection system initialization has not been completed.
5. The local wake-up (pin WAKE) detection system is initialized after the internal operation supply range is reached, therefore this wake-up is functioning correctly.

### 2. Module: CAN Bus Wake-Up Detection System Reinitialization

The device does not wake up via the CAN bus under the following conditions:

1. The VS drops below the CAN operation condition ($V_{VS}$ ~ 4.8V) but not below the undervoltage level ($V_{VS}$ ~ 3V), while the ATA6570 is in Sleep mode and $V_{VS}$ rises again above 4.8V.

**The root cause of this behavior is the missing reinitialization of the CAN bus wake-up detection system**.

1. The device falls below the CAN operation threshold while in Sleep mode.
2. At this point, the CAN wake-up system is disabled to prevent false wake-ups.
3. If $V_{VS}$ rises above 4.8V (typical), the CAN wake-up detection system is enabled and the initialization timer needs to elapse. But the clock for the timer is switched off, because the device is in Sleep mode; hence, no WUP is detected from the control logic. When the VS voltage is high enough, the CAN TRX control state machine switches from off to standby. In this mode, the CAN wake-up detection system is also enabled. As this system requires some time to work properly (several microseconds), a timer is started to blank out any signals from the system until the initialization phase is complete. The issue in the current implementation is that the CAN TRX control state machine does not assert the internal clock request signal long enough.
4. The local wake-up (pin WAKE) detection system is initialized after the internal operation supply range is reached, therefore this wake up is functioning correctly.

## Summary

The mode of failure is that the INH line is not driven high on the CAN message reception and does not go high on the power cycle. The issue can appear on any slow ramping supply voltage ($V_{VS}$), whether it is decreasing or increasing. If the battery voltage drops between 3V and 4.8V and an undervoltage event occurs on VIO or VCC (6-54 µs), the device goes to Sleep mode without configuring the CAN wake-up.

For recovery, a POR has to occur. This requires $V_{VS}$ to go below 2.5V approximately. With a high capacitance at the VS pin, several power cycles can occur and the VS voltage never falls below 2.5V.

# APPENDIX A: DOCUMENT REVISION HISTORY

## Rev. A Document (04/2018)

- Initial release of this document.

## Rev. B Document (04/2018)

- Corrected typographical and format errors.

**NOTES:**

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