Maxim DS1338 → MCP7940N Migration

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INTRODUCTION

This migration document describes how to replace the DS1338 RTCC with the MCP7940N RTCC.

Note: The MCP7940N has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in manufacturing this device, this device may have different performance characteristics than its earlier version. These differences may cause the device to perform differently in your application than the earlier version.

Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

The MCP7940N is an I²C™ RTCC device, similar to the DS1338. The MCP7940N and DS1338 are available in the standard 8-lead SOIC package.

Table 1 shows considerations that must be taken into account when migrating from DS1338 to the MCP7940N.

TABLE 1: DS1338 – MCP7940N MIGRATION REQUIRED MODIFICATIONS

No.	Required changes	HW	SW	Section Reference
1	External load capacitors required	✓	—	**Crystal Circuit**
2	MCP7940N recommends additional components for the battery backup circuit	✓	—	**Battery Backup**
3	The MCP7940N battery backup function is enabled by setting the VBATEN bit	—	✓	**Battery Backup**
4	MCP7940N and DS1338 have different I²C™ control bytes	—	✓	**Device Addressing**
5	The MCP7940N MFP pin (SQW/OUT on DS1338) has more functions: square-wave, alarms and firmware-controlled output	—	✓	**SQW/OUT vs. MFP Functionality**
6	The MCP7940N oscillator is enabled by a control bit with inverse polarity	—	✓	**Starting the Oscillator**
7	Additional control and Status bits in the Date and Time registers. SRAM address range changes	—	✓	**Accessing the RTCC and SRAM Registers**

TABLE 2: MCP7940N ADDITIONAL FEATURES

No.	Feature
1	64 bytes of battery-backed SRAM; DS1338 has only 56 bytes.
2	On-chip digital trimming/calibration.
3	Two programmable alarms.
4	More package options: 8-lead SOIC, TSSOP, MSOP and 2x3 TDFN.
5	Power-Up/Down Time-Stamp registers.
6	Leap year indication bit.
7	MCP7940N is available in Extended (-40°C to +125°C) Temperature range.

DS1338 and MCP7940N are electrically compatible. Although there are some differences between the two devices (shown in Table 3), these do not influence the migration process.

TABLE 3: ELECTRICAL DIFFERENCES BETWEEN MCP7940 AND DS1338

No.	Description	Symbol	Differences	
			MCP7940N	DS1338
1	Supply Voltage	V_{CC}	Industrial (I): 1.8V-5.5V	Typ. DS1338-18: 1.71-5.5V DS1338-3: 2.7-5.5V DS1338-33: 3-5.5V
2	V_{BAT} Battery Voltage	V_{BAT}	1.3-5.5V	1.3-3.7V
3	V_{BAT} Change Over	V_{TRIP} (V_{PF} on DS1338)	Typ. 1.5V	Typ. DS1338-18: 1.62V DS1338-3: 2.59V DS1338-33: 2.82V
4	V_{BAT} Current	I_{BAT}	Typ. 700 nA (V_{BAT}=3.0V)	Typ. 800 nA (V_{BAT}=3.7V)
5	Standby Current	I_{CCS}	Max. 5 µA (V_{CC}=5.5V)	100 uA for DS1338-18 (V_{CC}=1.89V) 200 uA for DS1338-33 (V_{CC}=5.5V)
6	Active supply current	I_{CCA}	Read: Max. 300 µA (400 kHz) Write: Max. 400 uA (400 kHz)	325 uA (400 kHz)
7	Crystal Selection	—	6-9pF (external capacitors required)	12.5pF (include internal capacitors)

SCHEMATIC RECOMMENDATIONS

The differences between the schematics of MCP7940N and DS1338 are the load capacitors (CX1 and CX2) and the battery backup circuit.

The recommended connections for the MCP7940N and DS1338 devices are shown in Figure 1 and Figure 2.

FIGURE 1: RECOMMENDED CONNECTIONS FOR DS1338 DEVICES

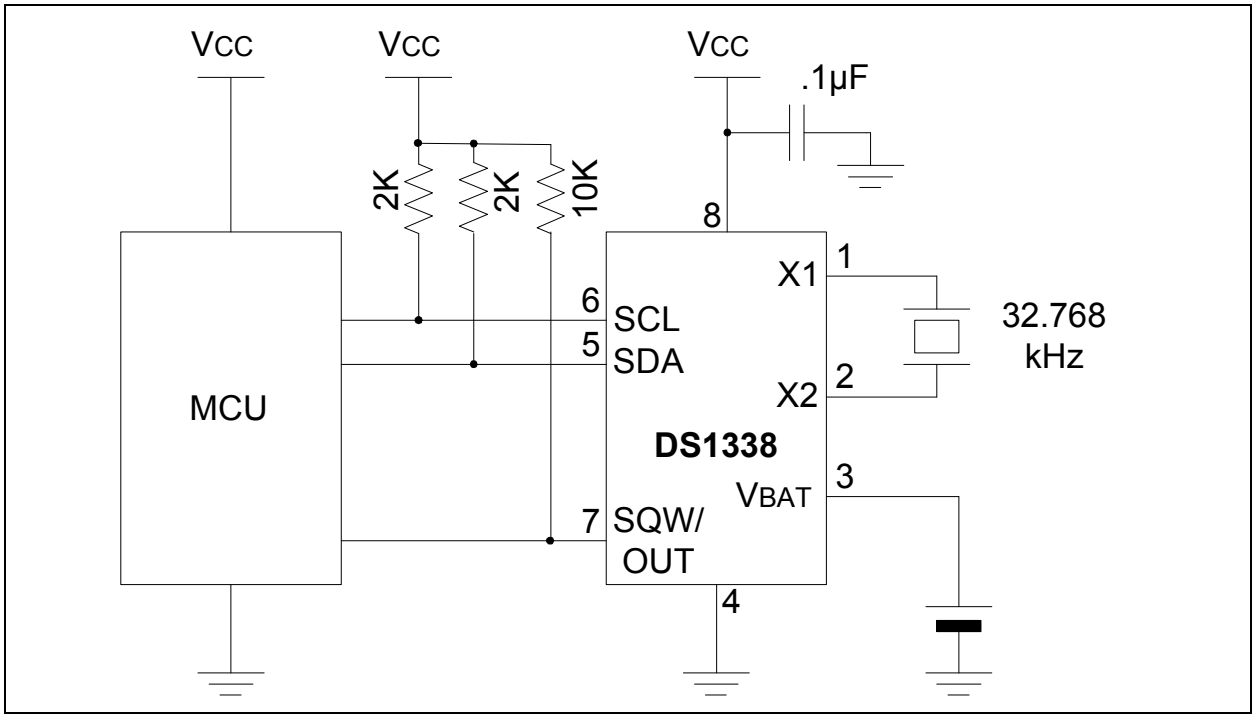
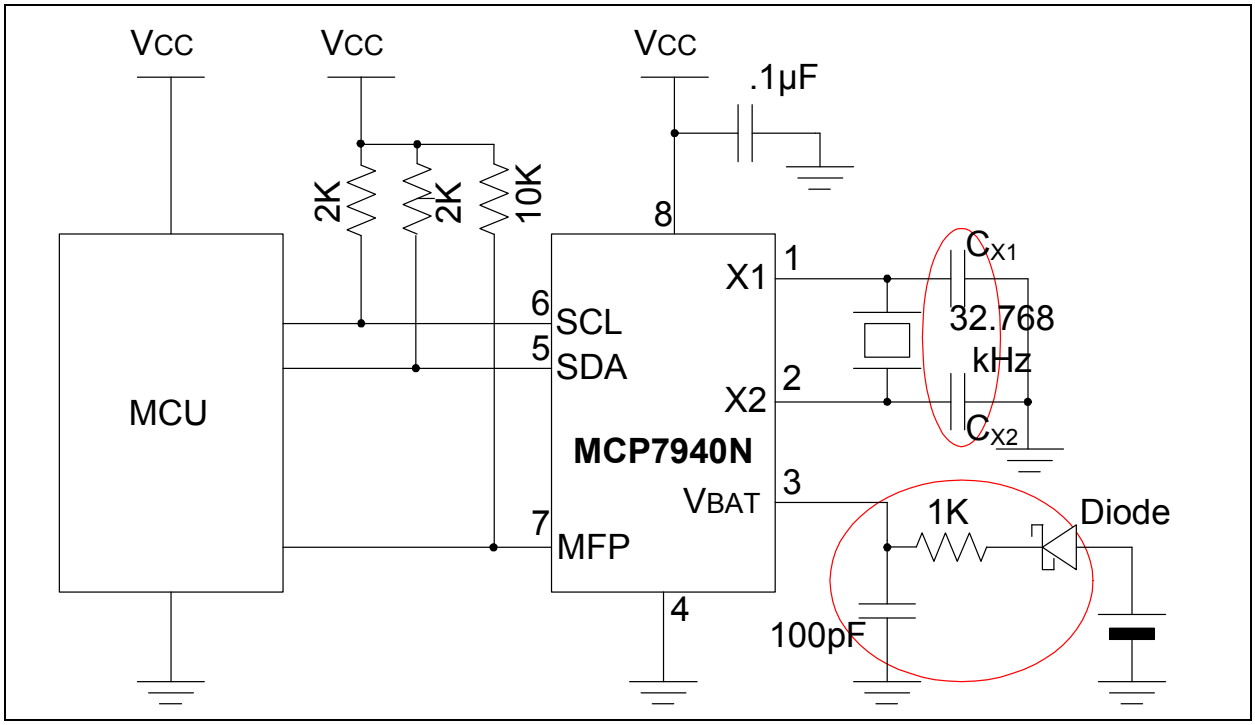


FIGURE 2: RECOMMENDED CONNECTIONS FOR MCP7940N DEVICES



CRYSTAL CIRCUIT

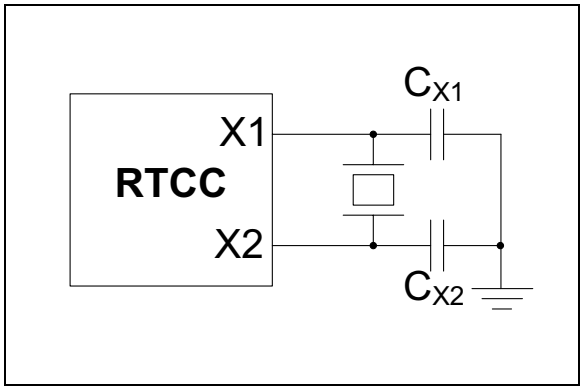
DS1338 is designed to use 32.768 kHz crystals with 12.5pF load capacitance. The CX1 and CX2 capacitors are internal.

Figure 3 shows the MCP7940N schematic for the oscillator circuit (this device does not have internal load capacitors, which must be included on the PCB). It has been designed to operate with a standard 32.768 kHz tuning fork crystal with a load capacitance of between 6-9pF.

Microchip recommends several crystals for which MCP7940N works reliably. For more information please consult the following documents:

- AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"* (DS01365)
- MCP7940N Data Sheet (DS25010)

FIGURE 3: OSCILLATOR DIAGRAM



BATTERY BACKUP

MCP7940N and DS1338 devices both have an automatic VCC switchover to VBAT, backup supply, to maintain the RTCC and SRAM during a VCC power fail.

The DS1338 battery backup feature is always enabled in hardware. On the MCP7940N, the battery backup feature is controlled by the VBATEN bit (bit 3) in the Day register (0x03). The VBATEN bit should be set to '1' to match the functionality of the DS1338. This bit is cleared by default on power-up.

Note: If the battery backup function is not enabled, the SRAM content will be lost and RTCC will be reset when VCC drops to VTRIP. If the device is operating in Battery Backup mode and the VBAT drops to the minimum voltage (see Table 3, VBAT parameter), the entire SRAM and RTCC data will no longer be preserved during power loss.

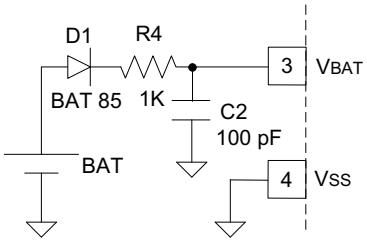
The MCP7940N and DS1338 are fully accessible through the serial interface while VCC is higher than VTRIP/VSO. These devices have different operating modes when VCC drops to VTRIP/VPF and when the backup supply voltage is higher than the supply voltage, VCC.

TABLE 4: VBAT VS. VCC

Device	Supply Condition	Serial Access	Powered By
DS1338	VCC > VPF, VCC > VBAT	Yes	VCC
	VCC > VPF, VCC < VBAT	Yes	VBAT
	VCC < VPF, VCC > VBAT	No	VCC
	VCC < VPF, VCC < VBAT	No	VBAT
MCP7940N	VCC > VTRIP	Yes	VCC
	VCC < VTRIP	No	VBAT

Note: The VTRIP parameter on MCP7940N is typically 1.5V. On DS1338, the VTRIP parameter is named VPF and is typically 2.82V (DS1338-33 device, see Table 3).

FIGURE 4: BATTERY BACKUP



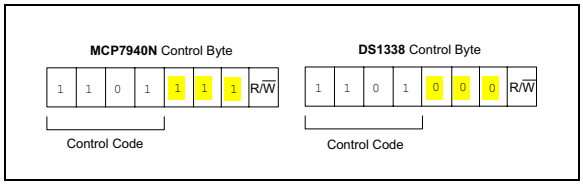
When using any supply, it is recommended to include a 1K series resistor, R4 and a 100pF capacitor, C2, between the supply and the VBAT pin (as seen in Figure 4). This is required to remove the spikes that can occur when switching from VCC to VBAT.

Additionally, a series diode, D1, is recommended when using a battery to eliminate any current flowing into the cell during a catastrophic failure of the RTCC device. For more information, see AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"* (DS01365).

DEVICE ADDRESSING

The MCP7940N and DS1338 control byte are shown in Figure 5.

FIGURE 5: ADDRESS SEQUENCE BIT ASSIGNMENTS



The MCP740N control byte for accessing the SRAM and RTCC registers is set to '1101111x' (0xDF for a read, 0xDE for a write). The RTCC registers and the SRAM share the same address space.

The control byte for DS1338 is different, '1101000x' (0xD0 for a write, 0xD1 for a read operation).

The Read/Write operations are identical for DS1338 and MCP7940N, only the control byte is different.

SQW/OUT vs. MFP FUNCTIONALITY

The SQW/OUT pin from the DS1338 is called MFP on the MCP7940N. It has compatible functionality and is still Pin 7 of the package.

SQW/OUT and MFP pins can be used to output a squarewave signal with a programmable frequency (1 Hz, 4 kHz, 8 kHz and 32 kHz) or toggled via the control bit, OUT. Additionally, the MFP pin from MCP7940N is asserted when the alarm is triggered.

On power-up, the SQW/OUT and MFP pins have the same default state polarity.

Device	Pin No.	Pin Name	Power-Up State
DS1338	7	SQW/OUT	High
MCP7940N	7	MFP	High

Note: SQW/OUT is enabled even if DS1338 is powered by V_{CC} or V_{BAT}. MFP is not enabled when MCP7940N is powered by V_{BAT}.

The MFP pin functionality is controlled by the Control register, same as SQW/OUT on DS1338.

TABLE 5: DS1338 AND MCP7940N CONTROL REGISTER

Device	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset State
DS1338	07h	OUT	0	**OSF**	**SQWE**	0	0	RS1	RS0	B2h
MCP7940N	07h	OUT	**SQWE**	**ALM1**	**ALM0**	**EXTOSC**	**RS2**	RS1	RS0	80h

Note: OSF is the Oscillator Stop Flag. This bit is set by hardware when the oscillator has been stopped. It remains 1 logic until cleared by the user.

Note: When migrating from DS1338 to MCP7940N, the EXTOSC and RS2 bits will be '0'.

Note: By default, the OSF and SQWE bits are set by hardware. The user must clear these bits if no alarm is used (ALM1:0).

The Control register is mapped at the same address, 07h, for MCP7940N and DS1338. Below is a description of each bit from the Control register:

- Bit 7 is the OUT bit: sets the logic level on the MFP when not using this as a square-wave output (MFP = 1 if OUT = 1 and MFP = 0 if OUT = 0)
- Bit 6 is the SQWE bit (bit 4 on DS1338): setting this bit enables the divided output from the crystal oscillator
- Bit 5:4 are ALM1:ALM0 bits: determine which alarms are active
- Bit 3 is the EXTOSC bit: setting this bit will allow an external 32.768 kHz signal to drive the RTCC registers, eliminating the need for an external crystal
- Bit 2:0 are RS2:RS0 bits: sets the internal divider for the 32.768 kHz oscillator to be driven to the MFP (1 Hz, 4 kHz, 8 kHz and 32 kHz for RS2 = 0, 64 Hz for RS2 = 1)

When migrating from DS1338 to MCP7940N, the Control register can be set, as shown in Example 1.

EXAMPLE 1:

```
DS1338_Control_Register = DS1338_SQWE | SQW_OUT_1Hz; // Control Register = 0x10
                                                    // (DS1338_SQWE = 0x10), (SQW_OUT_1Hz = 0x00)
MCP7940N_Control register = MCP7940N_SQWE | MFP_1Hz; // Control Register = 0x40
                                                    // (MCP7940N_SQWE = 0x40, MFP_1Hz = 0x00)

// SQWE bit = 1: enable square-wave function on MFP pin
// RS2:RS0 bits = 0: the frequency for the square-wave signal is 1 Hz
```

For more information, please refer to the MCP7940N Data Sheet (DS25010).

STARTING THE OSCILLATOR

The oscillator in both the RTCC's is enabled by a control bit, but the polarity varies between the devices. The enable is bit 7 in the Seconds register (0x00).

Device	Bit Name	State	Reset State
DS1338	CH	1 = disable oscillator 0 = enable oscillator	1
MCP7940N	ST	1 = enable oscillator 0 = disable oscillator	0

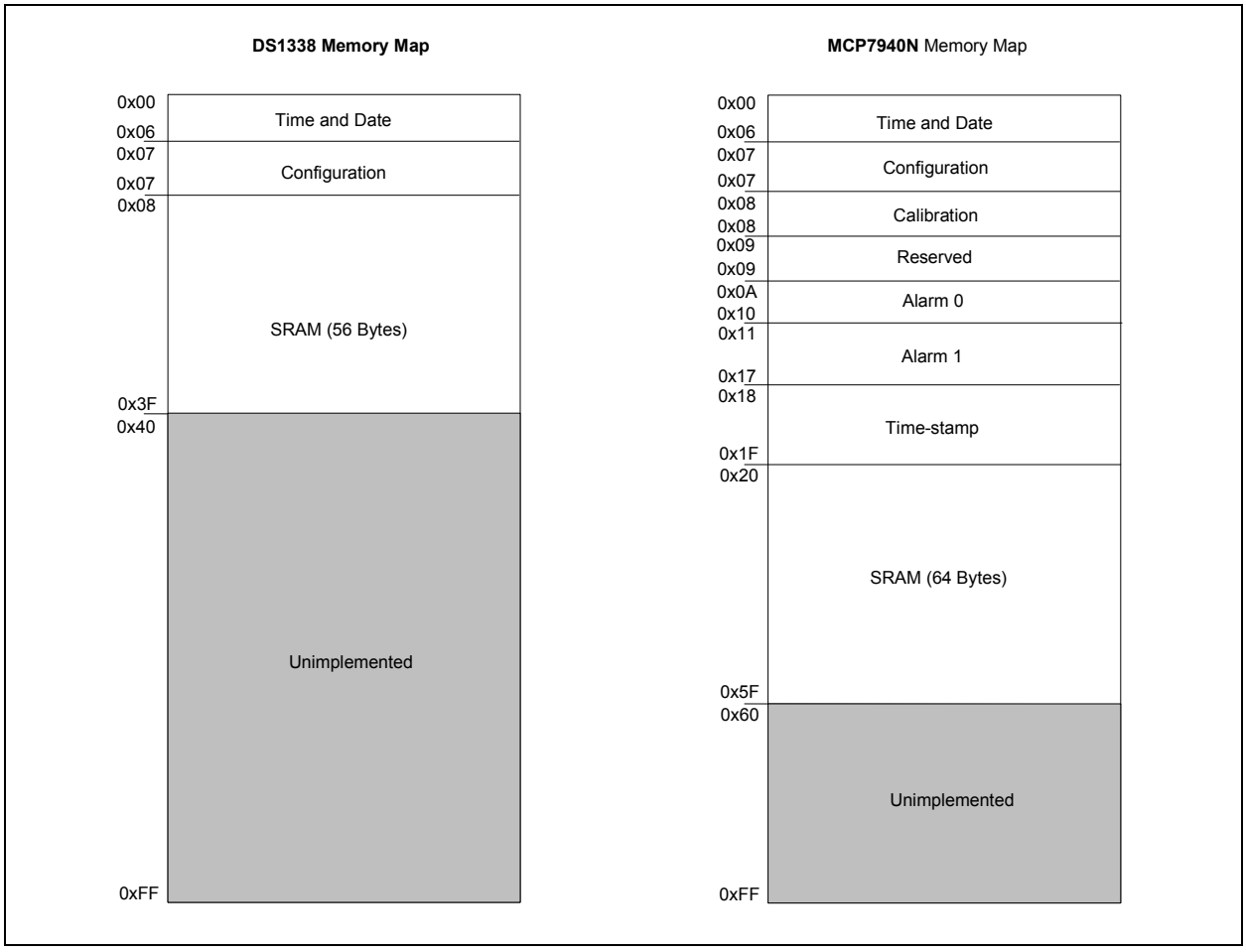
ACCESSING THE RTCC AND SRAM REGISTERS

On DS1338, the 56 bytes of RAM are located in address locations from 08h to 3Fh. These memory locations are used on MCP7940N by the calibration alarms and time-stamp registers.

On MCP7940N, the 64 bytes of RAM are located in address locations 20h to 5Fh.

Differences between the DS1338 and MCP7940N memory maps are shown in Figure 6.

FIGURE 6: DS1338 AND MCP7940N MEMORY MAP



The Date and Time registers are mapped on MCP7940N the same as DS1338 (from 00h to 07h address) with several differences that will be described below.

The SECONDS, MINUTES, HOUR, DATE and YEAR registers are mapped identically on the MCP7940N and DS1338.

The DAY register on MCP7940N contains the BCD day and additional bits for configuration and status (not present in the DS1338). The VBATEN bit (bit 3) is used to enable/disable the battery backup. The VBAT bit (bit 4) is set by hardware when the VCC falls and is cleared by firmware. The OSCON bit (bit 5) is set and cleared by hardware, indicating if the oscillator is currently running or not. This is a read-only bit.

The MONTH register has an additional bit, LP (bit 5), which indicates if the current year is a leap one. This is a read-only bit.

Care should be taken when the Date and Time registers are read or written. A number of the unimplemented "don't care" bits on DS1338, which read as '0', are used on MCP7940N as control and status bits (they are highlighted in Table 6).

EXAMPLE 2: READ THE DAY FROM MCP7940N

```
DAY_REGISTER & 0x07   =  Day  // Mask of
                         control and status bits
```

EXAMPLE 3: READ THE MONTH FROM MCP7940N

```
(MONTH_REGISTER & 0x10) * 10 +
(MONTH_REGISTER & 0x0F)          =  Month
```

TABLE 6: DATE AND TIME REGISTER MAP

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range	Reset State
Time Registers											
00h	ST	10 Seconds			Seconds				Seconds	00-59	00h
01h		10 Minutes			Minutes				Minutes	00-59	00h
02h		12/24	10 Hour AM/PM	10 Hour	Hour				Hours	1-12 + AM/PM 00 - 23	00h
03h			**OSCON**(Note)	**VBAT**(Note)	**VBATEN**	Day			Day	1-7	01h
04h			10 Date		Date				Date	01-31	01h
05h			**LP**(Note)	10 Month	Month				Month	01-12	01h
06h	10 Year				Year				Year	00-99	01h

Note: The OSCON, VBAT and LP bits are read-only.

Note: The shaded areas are not implemented and read as '0'.

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ISBN: 9781620771273

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