

Product Overview

Description

The SG1842/43 family of control IC's provides all the necessary features to implement off-line fixed frequency, current-mode switching power supplies with a minimum number of external components.

Current-mode architecture demonstrates improved line regulation, improved load regulation, pulse-by-pulse current limiting and inherent protection of the power supply output switch. The bandgap reference is trimmed to $\pm 1\%$ over temperature.

Oscillator discharge current is trimmed to less than $\pm 10\%$. The SG1842/43 has under-voltage lockout, current limiting circuitry and start-up current of less than 1 mA. The totem-pole output is optimized to drive the gate of a power MOSFET. The output is low in the off state to provide direct interface to an N-channel device. The SG1842/43 is specified for operation over the full military ambient temperature range of -55°C to 125°C . The SG2843 is specified for the industrial range of -25°C to 85°C .

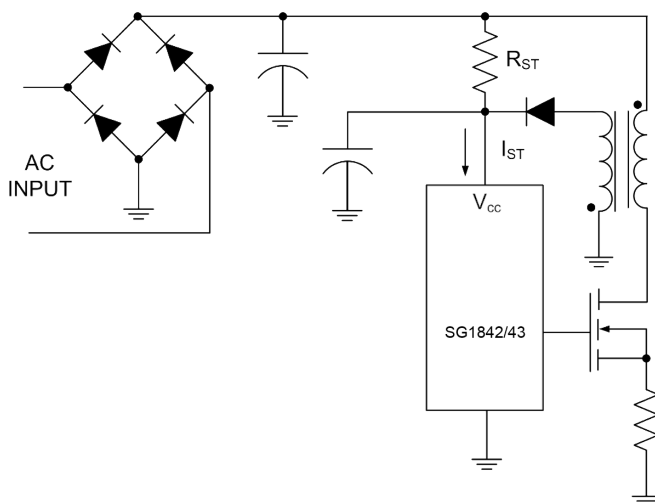
Features

- Optimized for off-line control
- Low start-up current ($< 1\text{ mA}$)
- Automatic feed forward compensation
- Trimmed oscillator discharge current
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with 6V hysteresis (SG1842 only)
- Double-pulse suppression
- High-current totem-pole output (1A peak)
- Internally trimmed bandgap reference
- 500 kHz operation
- Undervoltage lockout
 - SG1842 - 16 volts
 - SG1843 - 8.4 volts
- Low shoot-through current $< 75\text{ mA}$ over temperature

Application

- Available to MIL-STD-883 – 883
- Available to DLA
 - Standard Microcircuit Drawing (SMD)
- Microchip® level "S" processing available

Figure 1. Product Highlight



1. Connection Diagrams and Ordering Information¹⁻³

Ambient Temperature	Type	Package	Part Number	Packaging Type	Connection Diagram
0 °C to 70 °C	Y	8-Pin Ceramic Dual Inline Package	—	CERDIP	Y PACKAGE (Top View) PbSn Tin Lead Finish
-25 °C to 85 °C			—		
-55 °C to 125 °C			SG1842Y SG1843Y		
MIL-STD/883			SG1842Y-883B SG1843Y-883B		
DESC			SG1842Y-DESC SG1843Y-DESC		
0 °C to 70 °C	DM	8-Pin Small Outline Integrated Circuit	—	SOIC	DM PACKAGE (Top View) RoHS / Pb-free 100% Matte Tin Lead Finish
-25 °C to 85 °C			SG2843DM		
0 °C to 70 °C	D	14-Pin Small Outline Integrated Circuit	—	SOIC	D PACKAGE (Top View) RoHS / Pb-free 100% Matte Tin Lead Finish
-25 °C to 85 °C			SG2843D		
-55 °C to 125 °C	F	10-Pin Ceramic Flat Pack Package	SG1843F	Flat Pack	F PACKAGE (Top View) PbSn Lead Finish
MIL-STD/883			—		
DESC			—		
-55 °C to 125 °C	L	20-Pin Ceramic	SG1843L	Ceramic Leadless Chip Carrier (LCC)	L PACKAGE (Top View) PbSn Lead Finish
MIL-STD/883			SG1843L-883B		
DESC			SG1843L-DESC		

Notes:

- Contact factory for JAN and DESC part availability.
- All parts are viewed from the top.
- Available in tape and reel. Append the letters "TR" to the part number.

2. Absolute Maximum Ratings¹⁻²

Parameter	Value	Units
Supply voltage ($I_{CC} < 30 \text{ mA}$)	Self-limiting	V
Supply voltage (low impedance source)	30	V
Output current (peak)	± 1	A
Output current (continuous)	350	mA
Output energy (capacitive load)	5	μJ
Analog inputs (V_{FB} , I_{SENSE})	-0.3 to +6.3	V
Error amplifier output sink current	10	mA
Power dissipation at $T_A = 25^\circ\text{C}$ (DIL-8)	1	W
Operating Junction Temperature		
Hermetic (Y, F, L packages)	150	$^\circ\text{C}$
Plastic (D, DM packages)	150	$^\circ\text{C}$
Storage temperature range	-65 to +150	$^\circ\text{C}$
Lead temperature (soldering, 10 seconds)	300	$^\circ\text{C}$
RoHS / Pb-free peak package solder reflow temp. (40 second max. exposure)	260 (+0, -5)	$^\circ\text{C}$
Notes:		
1. Exceeding these ratings could cause damage to the device.		
2. All voltages are with respect to pin 5. All currents are positive into the specified terminal.		

3. Thermal Data¹⁻²

Parameter	Value	Units
DM Package		
Thermal resistance-junction to ambient, θ_{JA}	165	°C/W
D Package		
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W
Y Package		
Thermal resistance-junction to ambient, θ_{JA}	130	°C/W
F Package		
Thermal resistance-junction to case, θ_{JC}	80	°C/W
Thermal resistance-junction to ambient, θ_{JA}	145	°C/W
L Package		
Thermal resistance-junction to case, θ_{JC}	35	°C/W
Thermal resistance-junction to ambient, θ_{JA}	120	°C/W
Notes:		
1. Junction temperature calculation: $T_J = T_A + (P_D \times \theta_{JA})$.		
2. The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.		

4. Recommended Operating Conditions

Symbol	Parameter	Recommended Operating Conditions			Units
		Min	Typ	Max	
V_S	Supply voltage range	—	30	—	V
I_{PK}	Output current (peak)	—	± 1	—	A
I_{OUT}	Output current (continuous)	—	200	—	mA
	Analog inputs (V_{FB} , I_{SENSE})	0	—	2.6	V
EA_{SINK}	Error amp output sink current	—	5	—	mA
OSC_{FR}	Oscillator frequency range	0.1	—	500	kHz
R_T	Oscillator timing resistor	0.52	—	150	k Ω
C_T	Oscillator timing capacitor	0.001	—	1.0	μ F
Operating Ambient Temperature Range¹					
	SG1842/43	-55	—	125	$^{\circ}$ C
	SG2843	-25	—	85	$^{\circ}$ C
Note:					
1. Range over which the device is functional.					

5. Electrical Characteristics

Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1842/SG1843 with $-55\text{ }^{\circ}\text{C} \leq T_A \leq 125\text{ }^{\circ}\text{C}$, SG2843 with $-25\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $V_{CC} = 15\text{V}$, $R_T = 10\text{ k}\Omega$, and $C_T = 3.3\text{ nF}$. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

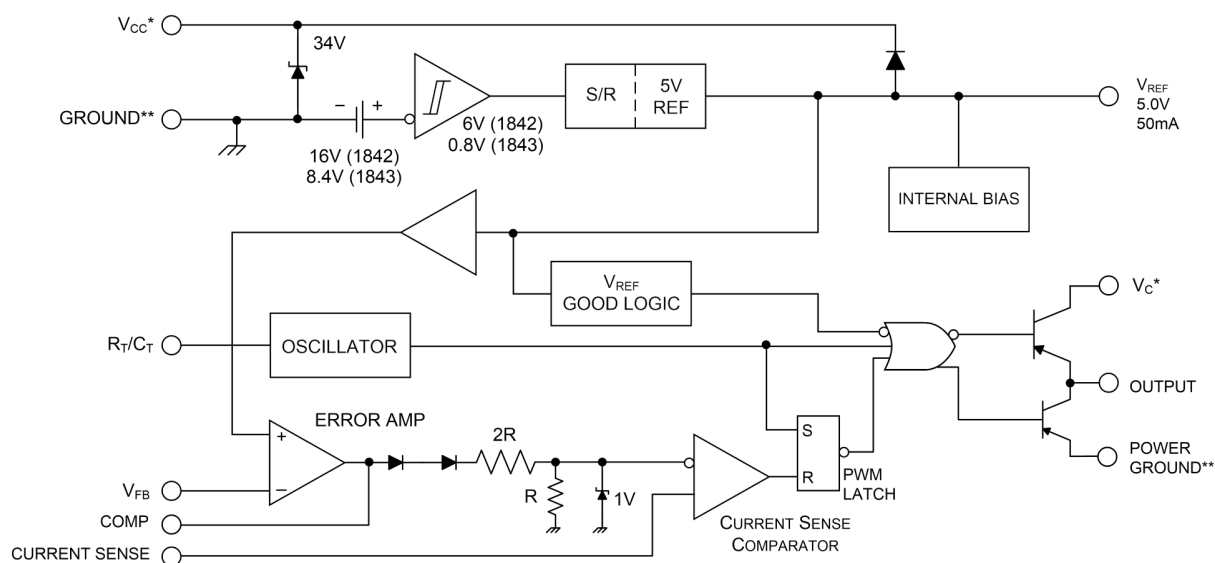
Symbol	Parameter	Test Conditions	SG1842/43			SG2843			Units
			Min	Typ	Max	Min	Typ	Max	
Reference Section									
V _{REF}	Output voltage	T _J = 25 °C, I _O = 1 mA	4.95	5.00	5.05	4.95	5.00	5.05	V
V _{REG}	Line regulation	12V ≤ V _{IN} ≤ 25V	—	6	20	—	6	20	mV
I _{REG}	Load regulation	1 ≤ I _O ≤ 20 mA	—	6	25	—	6	25	mV
	Temperature stability ¹		—	0.2	0.4	—	0.2	0.4	mV/°C
	Total output variation ¹	Line, load, temperature	4.90	—	5.10	4.90	—	5.10	V
V _N	Output noise voltage ¹	10 Hz ≤ f ≤ 10 kHz, T _J = 25 °C	—	50	—	—	50	—	μV
	Long term stability ¹	T _A = 125 °C, 1000 hrs	—	5	25	—	5	25	mV
V _{REFOSC}	Output short circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section ³									
f	Initial accuracy	T _J = 25 °C	47	52	57	47	52	57	kHz
f _{REG}	Voltage stability	12V ≤ V _{CC} ≤ 25V	—	0.2	1	—	0.2	1	%
	Temperature stability ¹	T _{MIN} ≤ T _A ≤ T _{MAX}	—	5	—	—	5	—	%
OSC _{PP}	Amplitude	V _{RT/CT} (peak to peak)	—	1.7	—	—	1.7	—	V
I _{DSG}	Discharge current	T _J = 25 °C	7.8	8.3	8.8	7.5	8.4	9.3	mA
		T _{MIN} ≤ T _A ≤ T _{MAX}	7.0	—	9.0	7.2	—	9.5	mA
Error Amp Section									
EA _{IN}	Input voltage	V _{COMP} = 2.5V	2.45	2.50	2.55	2.45	2.50	2.55	V
EA _{IB}	Input bias current		—	-0.3	-1	—	-0.3	1	μA
A _{VOL}	Open loop gain	2V ≤ V _O ≤ 4V	65	90	—	65	90	—	dB
EA _{BW}	Unity gain bandwidth ¹	T _J = 25 °C	0.7	1	—	0.7	1	—	MHz
PSRR	Power supply rejection ratio	12V ≤ V _{CC} ≤ 25V	60	70	—	60	70	—	dB
EA _{SINK}	Output sink current	V _{VFB} = 2.7V, V _{COMP} = 1.1V	2	6	—	2	6	—	mA
EA _{SRC}	Output source current	V _{VFB} = 2.3V, V _{COMP} = 5V	-0.5	-0.8	—	-0.5	-0.8	—	mA
EA _{VOH}	V _{OUT} High	V _{VFB} = 2.3V, R _L = 15k to GND	5	6	—	5	6	—	V
EA _{VOL}	V _{OUT} Low	V _{VFB} = 2.7V, R _L = 15k to V _{REF}	—	0.7	1.1	—	0.7	1.1	V
Current Sense Section									
CS _{AVOL}	Gain ^{2,3}		2.85	3	3.15	2.85	3	3.15	V/V
	Maximum input signal ²	V _{COMP} = 5V	0.9	1	1.1	0.9	1	1.1	V
PSRR	Power supply rejection ratio ²	12V ≤ V _{CC} ≤ 25V	—	70	—	—	70	—	dB
CS _{IB}	Input bias current		—	-2	-10	—	-2	-10	μA
CS _{DELAY}	Delay to output ¹		—	150	300	—	150	300	ns

.....continued

Symbol	Parameter	Test Conditions	SG1842/43			SG2843			Units
			Min	Typ	Max	Min	Typ	Max	
Output Section									
V _{OL}	Output low level	I _{SINK} = 20 mA	—	0.1	0.4	—	0.1	0.4	V
		I _{SINK} = 200 mA	—	1.5	2.2	—	1.5	2.2	V
V _{OH}	Output high level	I _{SOURCE} = 20 mA	13	13.5	—	13	13.5	—	V
		I _{SOURCE} = 200 mA	12	13.5	—	12	13.5	—	V
R _S	Rise time	T _J = 25 °C, C _L = 1 nF	—	50	150	—	50	150	ns
F _T	Fall time	T _J = 25 °C, C _L = 1 nF	—	50	150	—	50	150	ns
Under-Voltage Lockout Section									
UVLO	Start threshold	1842	15	16	17	15	16	17	V
		1843/2843	7.8	8.4	9.0	7.8	8.4	9.0	V
V _{SMIN}	Min. operation voltage after turn-on	1842	9	10	11	9	10	11	V
		1843/2843	7.0	7.6	8.3	7.0	7.6	8.2	V
PWM Section									
DC _{MAX}	Maximum duty cycle		93	95	100	90	95	100	%
DC _{MIN}	Minimum cuty cycle		—	—	0	—	—	0	%
Power Consumption Section									
I _S	Start-up current		—	0.5	1	—	0.5	1	mA
I	Operating supply current	V _{FB} = V _{ISENSE} = 0V	—	11	17	—	11	17	mA
Z	V _{CC} Zener voltage	I _{CC} = 25 mA	—	34		—	34	—	V
Notes:									
1. These parameters, although guaranteed, are not 100% tested in production.									
2. Parameter measured at trip point of latch with V _{VFB} = 0.									
3. Gain defined as: A = ΔV _{COMP} / ΔV _{ISENSE} ; 0 ≤ V _{ISENSE} ≤ 0.8V									
4. Adjust V _{CC} above the start threshold before setting at 15V.									

6. Block Diagram

Figure 6-1. Block Diagram



* - V_{CC} and V_C are internally connected for 8-pin packages.

** - **POWER GROUND** and **GROUND** are internally connected for 8-pin packages.

7. Characteristic Curves

Figure 7-1. Dropout Voltage Vs. Temperature

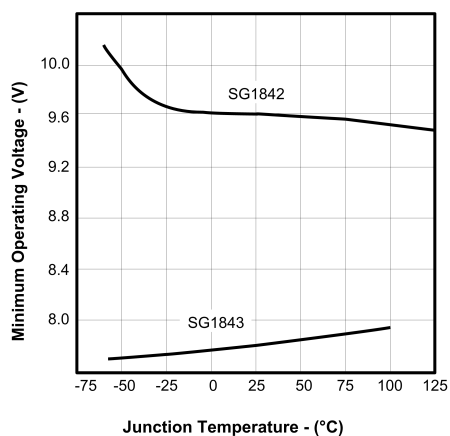


Figure 7-2. Oscillator Temperature Stability

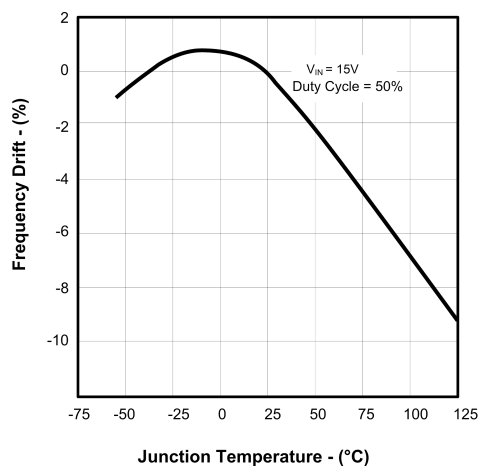


Figure 7-3. Current Sense to Output Delay Vs. Temperature

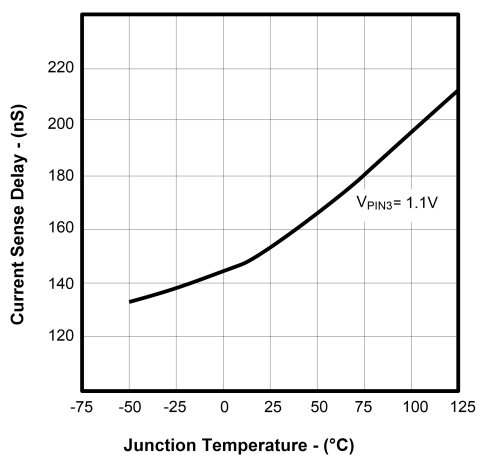


Figure 7-4. Output Duty Cycle Vs. Temperature

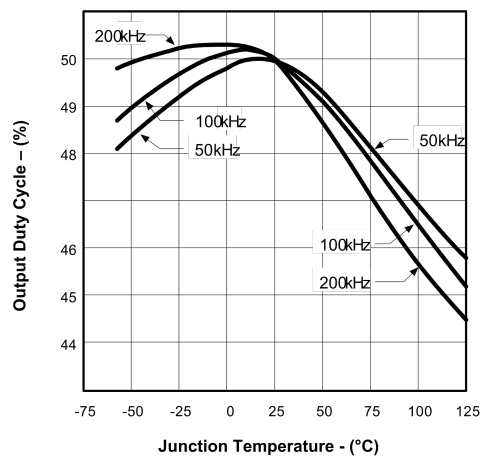


Figure 7-5. Start-Up Current Vs. Temperature

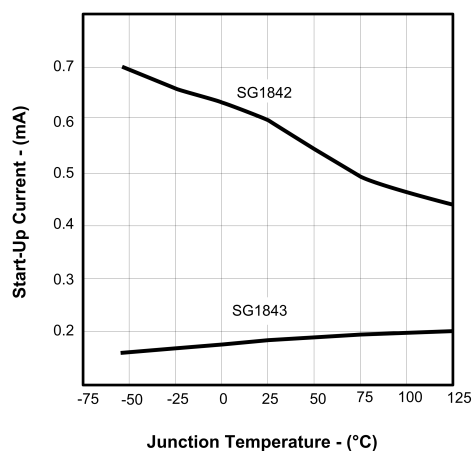


Figure 7-6. Reference Voltage Vs. Temperature

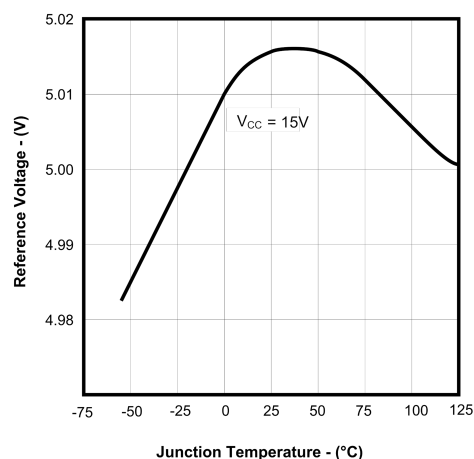


Figure 7-7. Start-Up Voltage Threshold Vs. Temperature

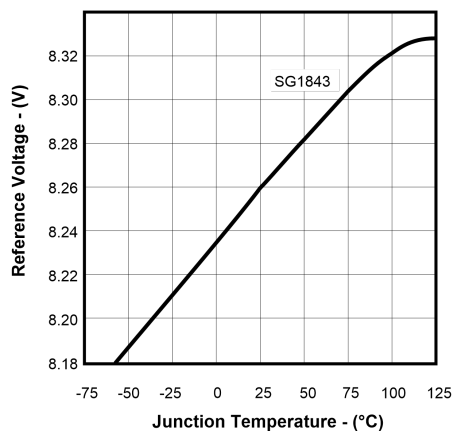


Figure 7-8. Start-Up Voltage Threshold Vs. Temperature

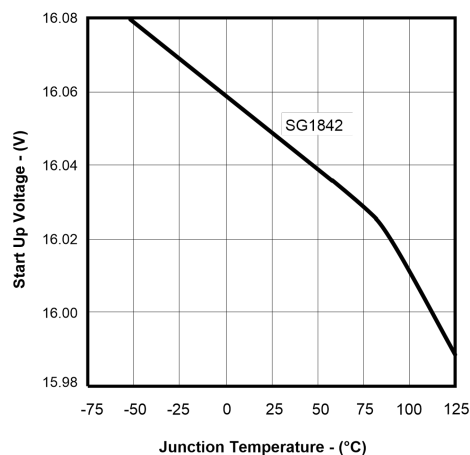


Figure 7-9. Oscillator Discharge Current Vs. Temperature

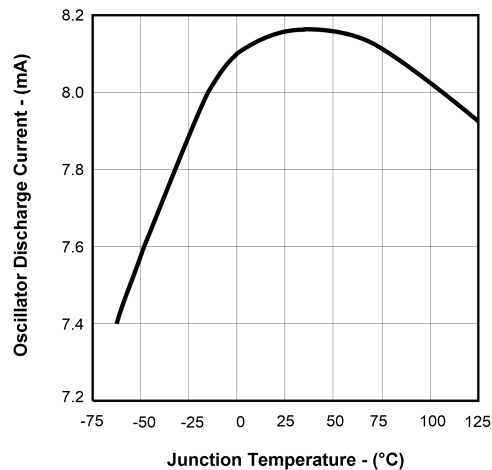


Figure 7-10. Output Saturation Voltage Vs. Output Current and Temperature (Sink Transistor)

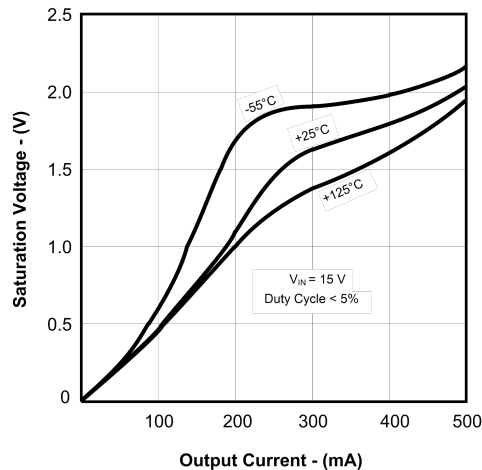


Figure 7-11. Current Sense Threshold Vs. Error Amplifier Output

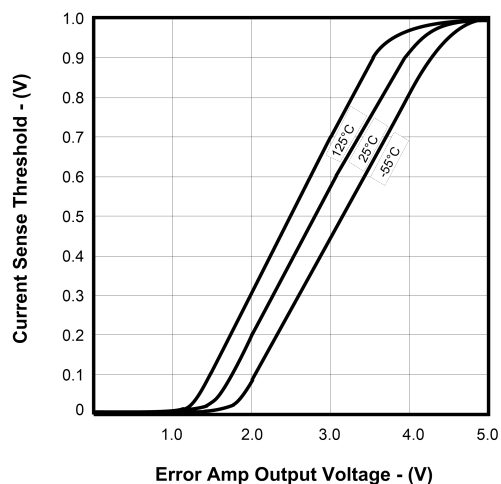
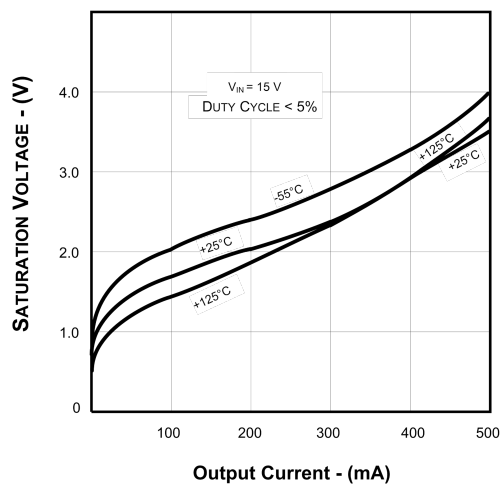


Figure 7-12. Output Saturation Voltage Vs. Output Current and Temperature



8. Application Information

The oscillator of the 1842/43 family of PWM's is designed such that many values of R_T and C_T will give the same oscillator frequency, but only one combination will yield a specific duty cycle at a given frequency.

Given:

Frequency $\equiv f$

Maximum Duty Cycle $\equiv D_m$

Calculate:

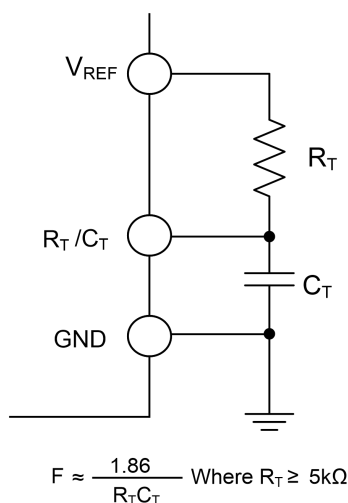
$$R_T = 267 \left[\frac{(1.76)^{1/D_m} - 1}{(1.76)^{(1-D_m)/D_m} - 1} \right] (\Omega)$$

where $0.3 < D_m < 0.95$

$$C_T = \frac{1.86 * D_m}{f * R_T} (\mu F)$$

For Duty-Cycles above 95% use:

Figure 8-1. Oscillator Timing Circuit



A set of formulas are given to determine the values of R_T and C_T for a given frequency and maximum duty cycle. (Note: These formulas are less accurate for smaller duty cycles or higher frequencies. This will require trimming of R_T or C_T to correct for this error.)

Example:

A Flyback power supply requires a maximum of 45% duty cycle at a switching frequency of 50 kHz. What are the values of R_T and C_T ?

Given:

$f = 50 \text{ kHz}$

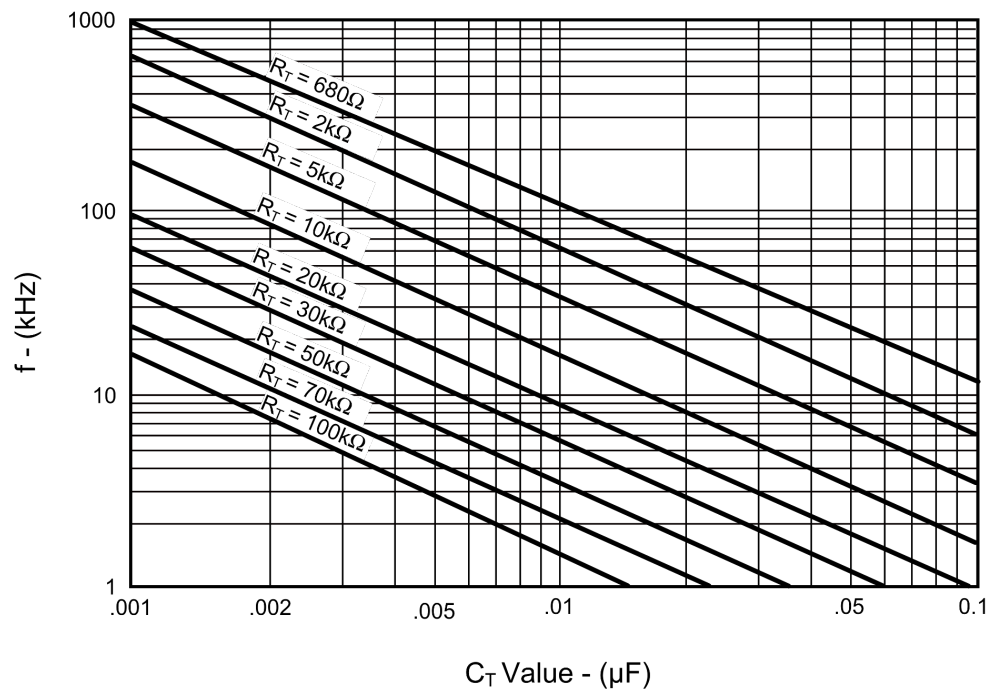
$D_m = 0.45$

Calculate:

$$R_T = 267 \left[\frac{(1.76)^{\frac{1}{.45}} - 1}{(1.76)^{\frac{.55}{.45}} - 1} \right] = 674 \Omega$$

$$C_T = \frac{1.86 * 0.45}{50000 * 674} = .025 (\mu F)$$

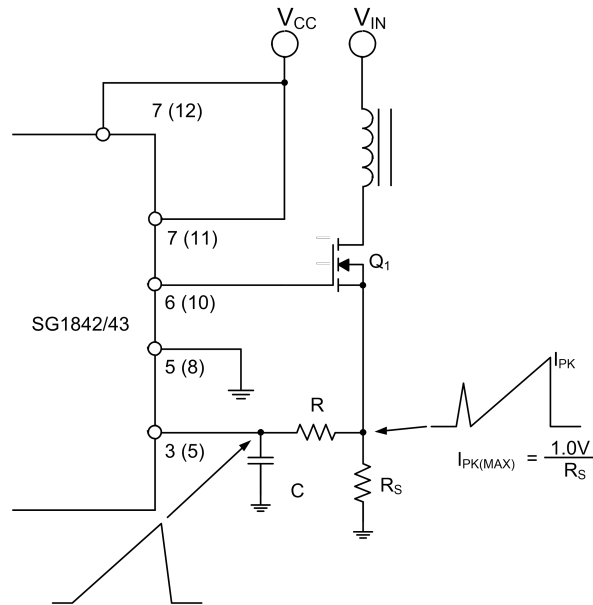
Figure 8-2. Oscillator Frequency Vs. R_T For Various C_T



9. Typical Application Circuits

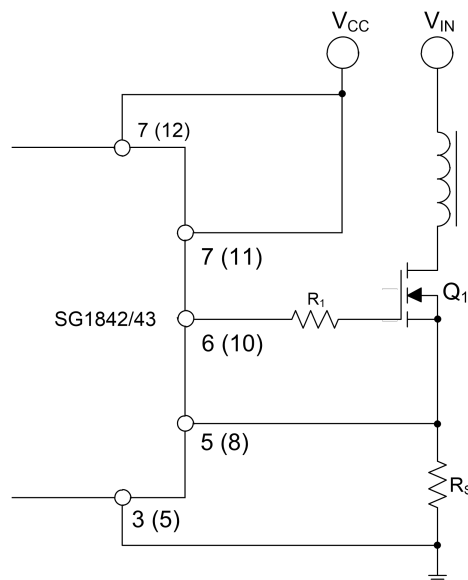
Pin numbers referenced are for 8-pin package and pin numbers in parenthesis are for 14-pin package.

Figure 9-1. Current Sense Spike Suppression



The RC low-pass filter eliminates the leading edge current spike caused by parasitic of Power MOSFET.

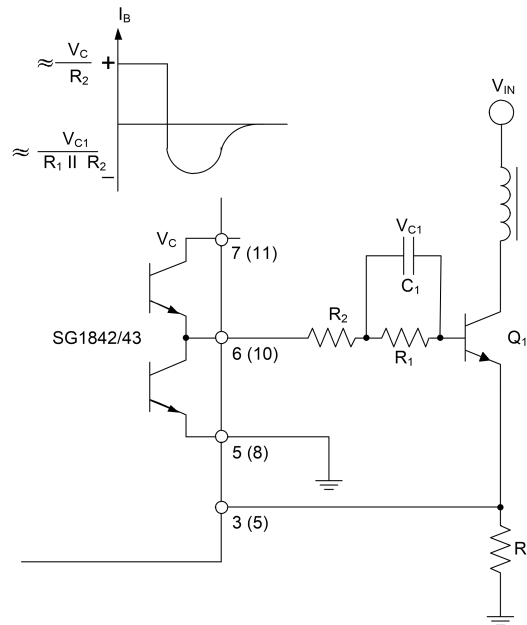
Figure 9-2. MOSFET Parasitic Oscillations



A resistor (R1) in series with the MOSFET gate reduce overshoot and ringing caused by the MOSFET input capacitance and any inductance in series with the gate drive. (Note: It is very important to have

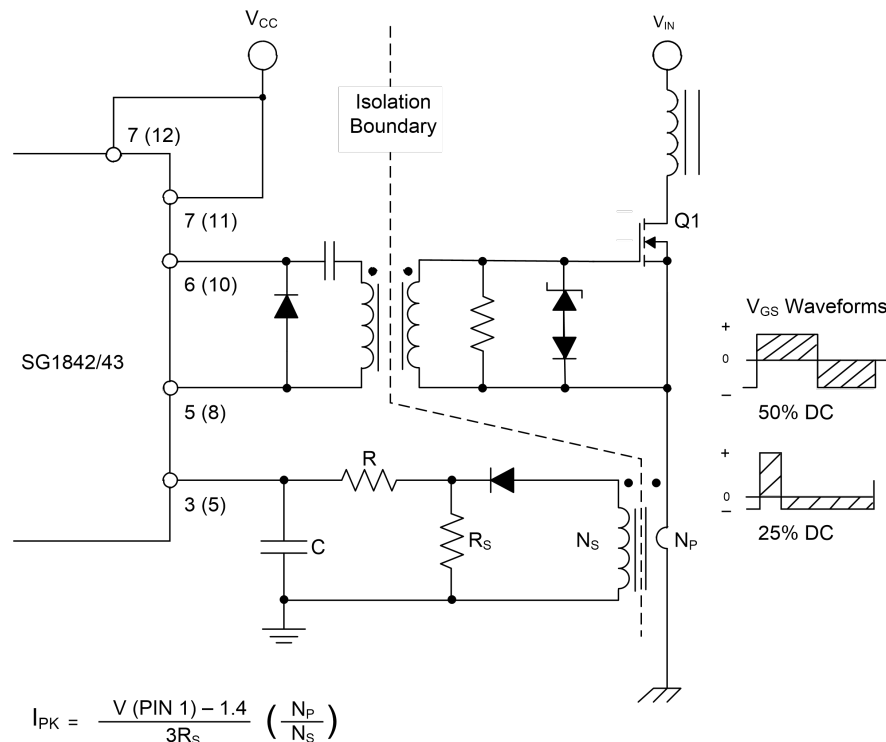
a low inductance ground path to insure correct operation of the I.C. This can be done by making the ground paths as short and as wide as possible.)

Figure 9-3. Bipolar Transistor Drive



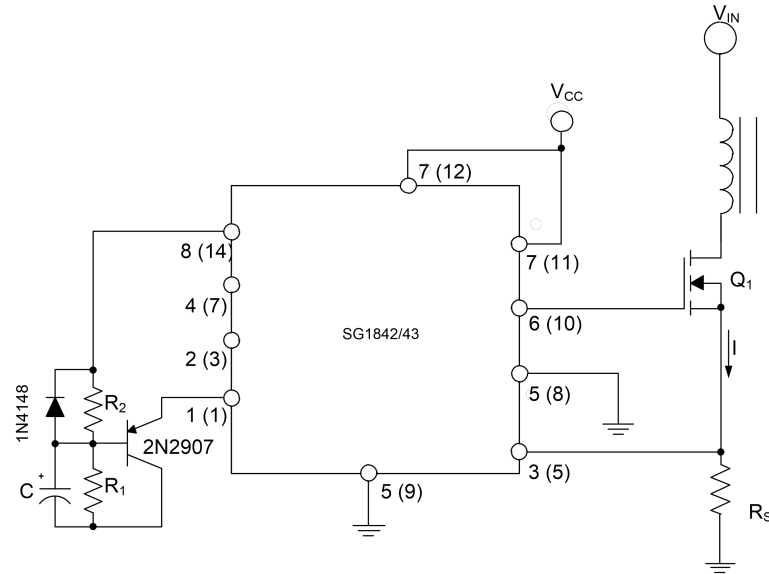
The 1842/43 output stage can provide negative base current to remove base charge of power transistor (Q_1) for faster turn off. This is accomplished by adding a capacitor (C_1) in parallel with a resistor (R_1). The resistor (R_1) is to limit the base current during turn on.

Figure 9-4. Isolated MOSFET Drive



Current transformers can be used where isolation is required between PWM and Primary ground. A drive transformer is then necessary to interface the PWM output with the MOSFET.

Figure 9-5. Adjustable Buffered Reduction of Clamp Level with Softstart



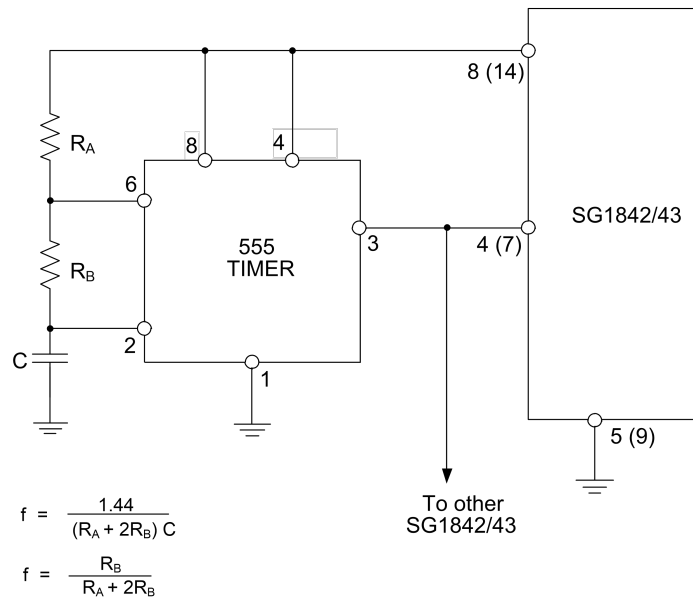
$$I_{PK} = \frac{V_{CS}}{R_S}$$

Where, $V_{CS} = 1.67 \left(\frac{R_1}{R_1 + R_2} \right)$ and $V_{CS,MAX} = 1V$ (Typ.)

$$t_{SOFTSTART} = -\ln \left[1 - \frac{V_{EAO} - 1.3}{5 \left(\frac{R_1}{R_1 + R_2} \right)} \right] \left(\frac{R_1 R_2}{R_1 + R_2} \right) C$$

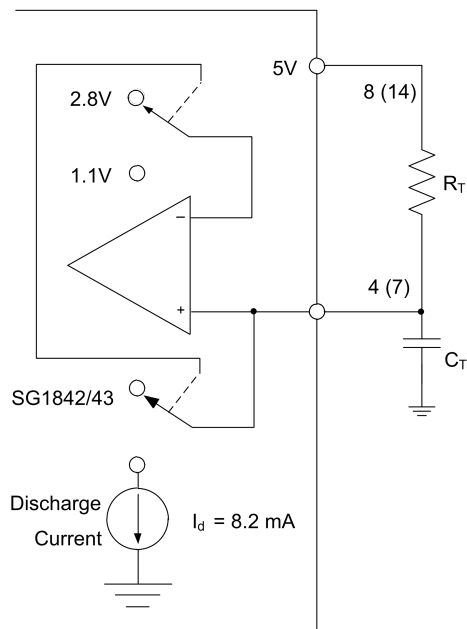
Where, $V_{EAO} \equiv$ voltage at the Error Amp Output under minimum line and maximum load conditions
Softstart and adjustable peak current can be done with the external circuitry shown in [Figure 9-5](#).

Figure 9-6. External Duty Cycle Clamp and Multi-Unit Synchronization



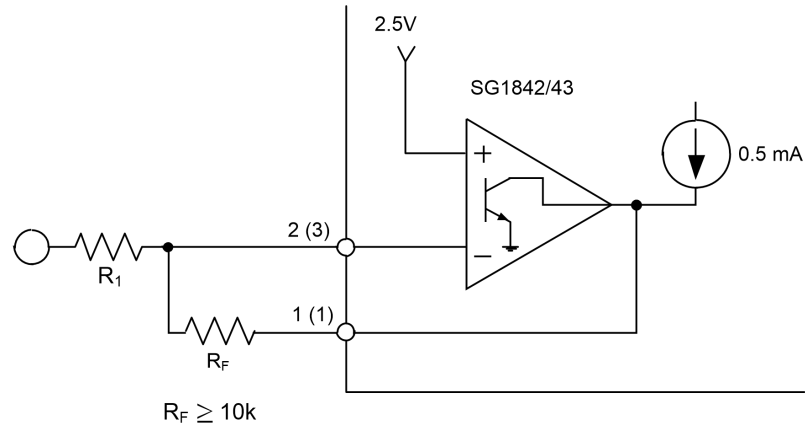
Precision duty cycle limiting as well as synchronizing several 1842/1843's is possible with circuitry shown in [Figure 9-6](#).

Figure 9-7. Oscillator Connection



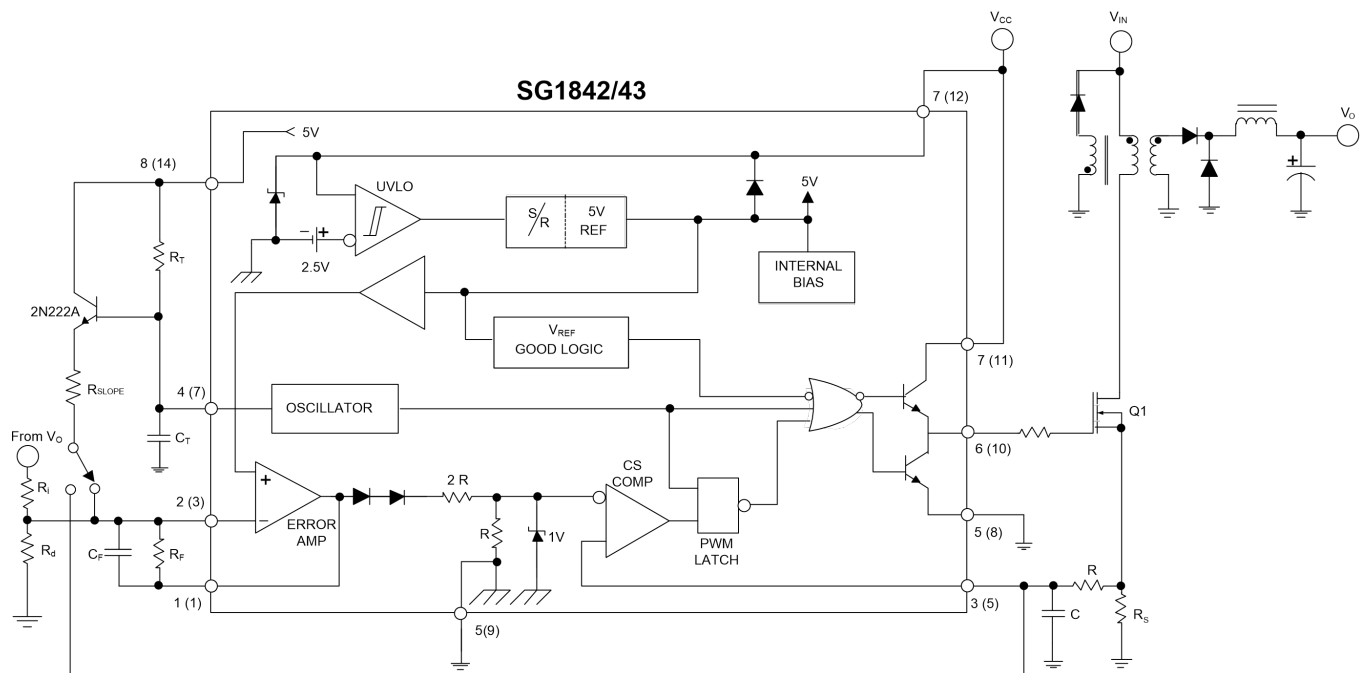
The oscillator is programmed by the values selected for the timing components R_T and C_T . Refer to application information for calculation of the component values.

Figure 9-8. Error Amplifier Connection



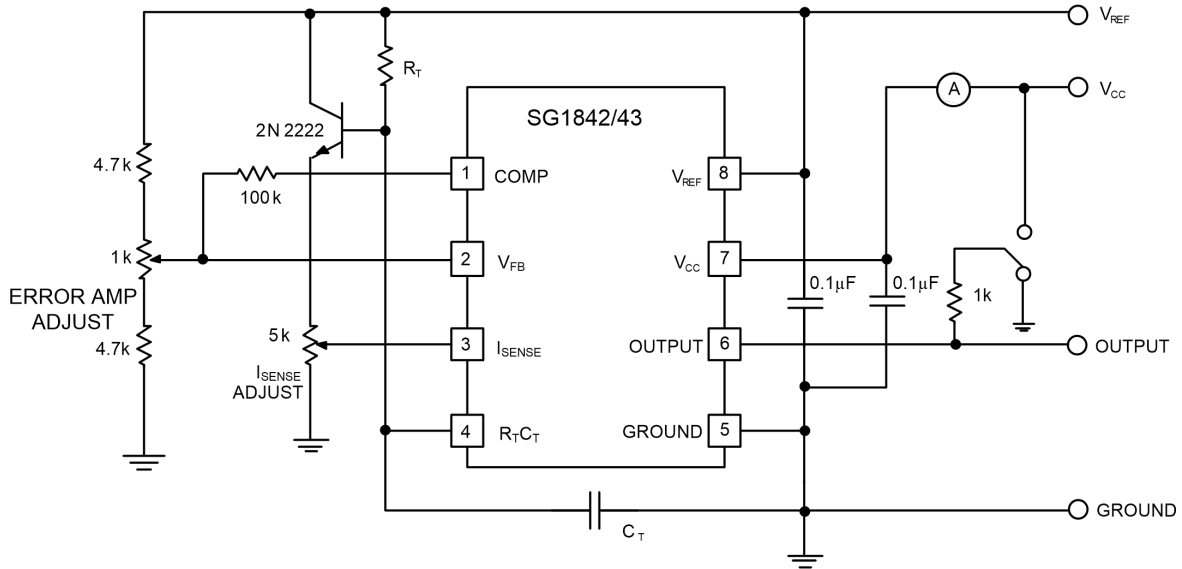
Error amplifier is capable of sourcing and sinking current up to 0.5 mA.

Figure 9-9. Slope Compensation



Due to inherent instability of current mode converters running above 50% duty cycle, slope compensation should be added to either current sense pin or the error amplifier. [Figure 9-9](#) shows a typical slope compensation technique.

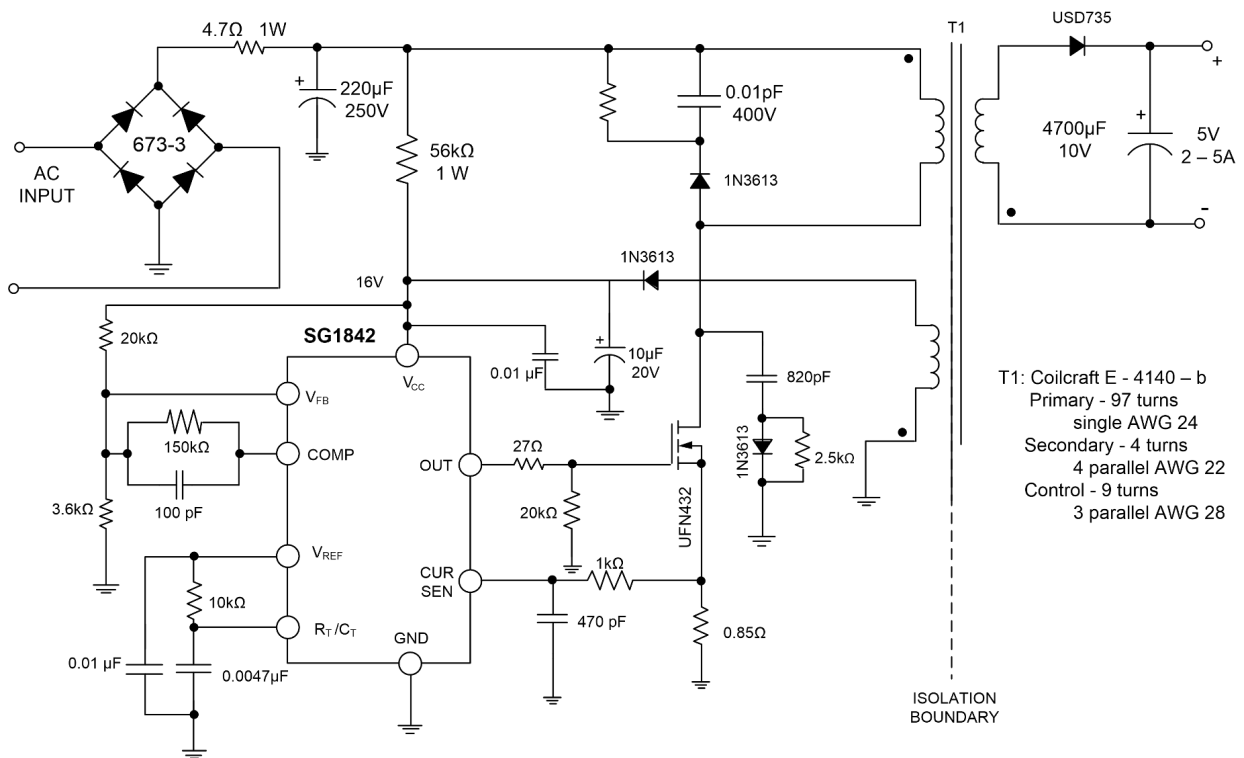
Figure 9-10. Open Loop Laboratory Fixture



High-peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected to pin 5 in a single point ground.

The transistor and 5 k Ω potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

Figure 9-11. Off-line Flyback Regulator



Specifications

Input line voltage: 90 VAC to 130 VAC

Input frequency:	50 or 60 Hz
Switching frequency:	40 kHz $\pm$ 10%
Output power:	25W maximum
Output voltage:	5V $\pm$ 5%
Output current:	2 to 5A
Line regulation:	0.01 %/V
Load regulation:	8 %/A ¹
Efficiency at 25 Watt:	$V_{IN} = 90$ VAC: 70% $V_{IN} = 130$ VAC: 65%
Output short-circuit current:	2.5 A average

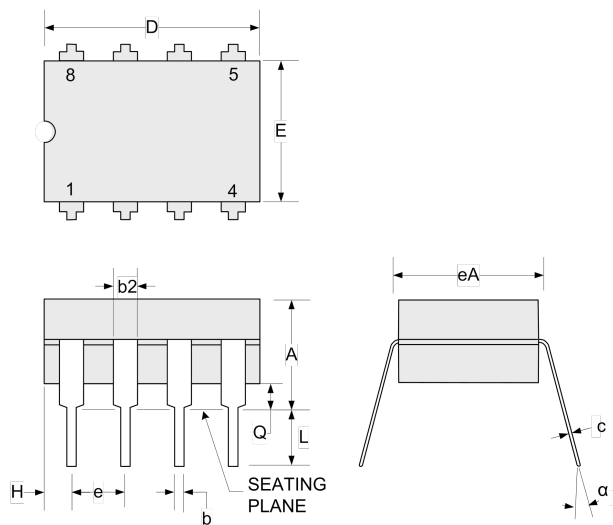
Note:

1. This circuit uses a low-cost feedback scheme in which the DC voltage developed from the primary-side control winding is sensed by the SG1842 error amplifier. Load regulation is therefore dependent on the coupling between secondary and control windings and on transformer leakage inductance.

10. Package Outline Dimensions

Controlling dimensions are in inches. Metric equivalents are shown for general information.

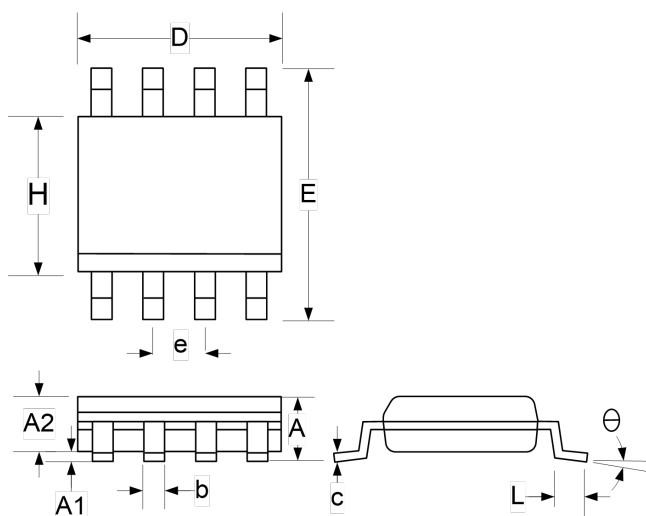
Figure 10-1. Y 8-Pin CERDIP Package Dimensions



Dim ¹	Millimeters		Inches	
	Min	Max	Min	Max
A	4.32	5.08	0.170	0.200
b	0.38	0.51	0.015	0.020
b2	1.04	1.65	0.045	0.065
c	0.20	0.38	0.008	0.015
D	9.52	10.29	0.375	0.405
E	5.59	7.11	0.220	0.280
e	2.54 BSC		0.100 BSC	
eA	7.37	7.87	0.290	0.310
H	0.63	1.78	0.025	0.070
L	3.18	4.06	0.125	0.160
α	—	15°	—	15°
Q	0.51	1.02	0.020	0.040

Note:

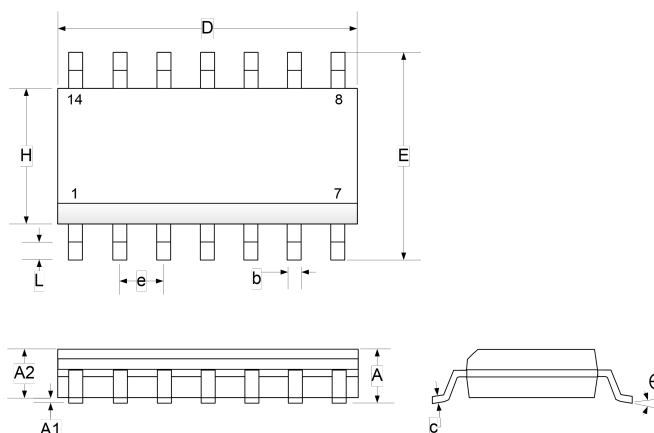
1. Dimensions do not include protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.

Figure 10-2. DM 8-Pin SOIC Package Dimensions


Dim ¹	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	4.83	5.21	0.189	0.205
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
LC ²	—	.010	—	0.004

Notes:

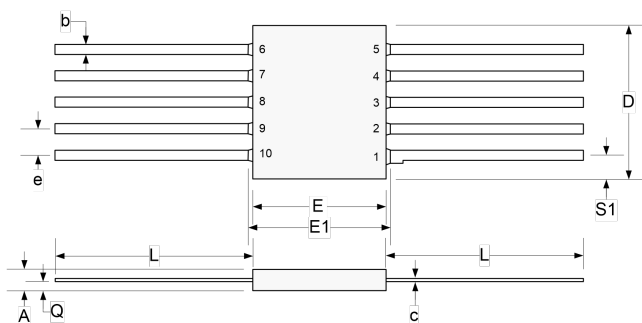
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Lead co-planarity

Figure 10-3. D 14-Pin SOIC Package Dimensions


Dim ¹	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.007	0.010
D	8.54	8.74	0.336	0.344
E	5.79	6.20	0.228	0.244
e	1.27 BSC		0.050 BSC	
H	3.81	4.01	0.150	0.158
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
LC ²	—	.010	—	0.004

Notes:

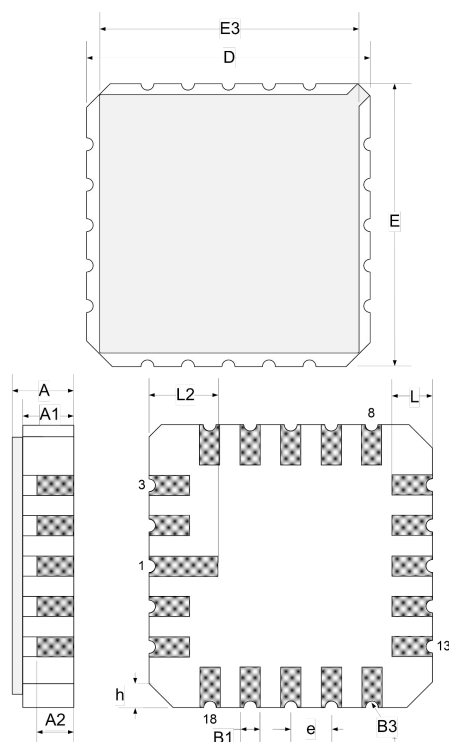
1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155 mm (.006") on any side. Lead dimension shall not include solder coverage.
2. Lead co-planarity

Figure 10-4. F 10-Pin Ceramic Flatpack Package Dimensions


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.45	1.90	0.057	0.075
b	0.25	0.483	0.010	0.019
c	0.102	0.152	0.004	0.006
D	—	7.37	—	0.290
E	6.04	6.40	0.238	0.252
E1	—	6.91	—	0.272
e	1.27 BSC		0.050 BSC	
L	6.35	9.40	0.250	0.370
Q	0.51	1.02	0.020	0.040
S1	0.20	0.38	0.008	0.015

Notes:

- Lead No. 1 is identified by tab on lead or dot on cover.
- Leads are within 0.13 mm (.0005") radius of the true position (TP) at maximum material condition.
- Dimension "e" determines a zone within which all body and lead irregularities lie.

Figure 10-5. L 20-Pin Leadless Chip Carrier Package Dimensions


Dim	Millimeters		Inches	
	Min	Max	Min	Max
D/E	8.64	9.14	0.340	0.360
E3	—	8.128	—	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	—	1.168	—	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note:

- All exposed metalized area shall be gold plated 60 micro-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

11. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	09/2023	Initial revision.

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