
MCP3918 Rev. A Silicon Errata and Data Sheet Clarification

The MCP3918 parts you have received conform functionally to the Device Data Sheet (DS20005287A), except for the anomalies described in this document.

All of the issues listed here will be addressed in future revisions of the MCP3918 silicon.

Contact Microchip Technology Inc. for the latest Silicon fix.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS20005287A):

None to report at this time.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

1. Module: ADC Conversion

The converter internal phases can be erroneously generated if there is a simultaneous occurrence of a master clock edge and a reset event (a $\overline{\text{RESET}}$ pin rising edge, the last SCK rising edge of a write communication that generates an ADC reset and restart as defined in [Section 6.6 “Situations that Reset and Restart Active ADCs”](#) or a Power-on Reset). This perturbation in the internal clock phase generation can cause modulator instability and generate erroneous results, so it is highly recommended to avoid these events becoming synchronized.

Work around

A possible work around of this issue is to freeze the master clock during all the above detailed events (a $\overline{\text{RESET}}$ pin rising edge, the last SCK rising edge of a write communication that generates an ADC reset and restart as defined in [Section 6.6 “Situations that Reset and Restart Active ADCs”](#) or a Power-on Reset). In this case, the part will not exhibit any issue.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev. A Document (7/2015)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

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