KSZ8051 to KSZ8081/KSZ8091 (32-QFN) -- Hardware Differences

Hardware Pin Differences: Tabulated are only pin differences between parts (pins common to all parts are not shown)
Internal pull-up/pull-down values for the strapping pins are indicated after table

Rev 1.0 Created

Pin #	KSZ8051MNL (0.13um) Name	Type	Function	KSZ8081MNX (0.11um) Name	Type	Function	KSZ8091MNX (0.11um) Name	Type	Function
21	INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.	INTRP / NAND_Tree#	Ipu/Opu	**Sames as KSZ8051MNL (0.13um)**	INTRP / PME_N2 / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output PME_N Output: Programmable PME_N Output (pin option 2) This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.
22	TXC	I/O	MII Mode: MII Transmit Clock Output MII Back-to-Back Mode: MII Transmit Clock Input	TXC (pin 22)	I/O	**MII mode: MII Transmit Clock output** **Note:** **At the de-assertion of reset, this pin needs to latch in a pull-down value for normal operation. If MAC side pulls this pin high, PHY will goes to factory test mode, see Register 16h, set Bit [15]=0' for solution. Or an external pull-down resistor is recommended.**	TXC / PME_EN	Ipd/O	MII Mode: MII Transmit Clock Output MII Back-to-Back Mode: MII Transmit Clock Input Config Mode: The pull-up/pull-down value is latched as PME_EN at the de-assertion of reset.
30	LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset.	LED0 / NWAYEN	Ipu/O	**Sames as KSZ8051MNL (0.13um)**	LED0 / PME_N1 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / PME_N Output: Programmable PME_N Output (pin option 1) In this mode, this pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset.
31	LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset.	LED1 / SPEED	Ipu/O	**Sames as KSZ8051MNL (0.13um)**	TXER	Ipd	MII Mode: MII Transmit Error Input

KSZ8051MNL (0.13um) Name	Type	Function	KSZ8051RNL (0.13um) Name	Type	Function	KSZ8081RNB (0.11um) Name	Type	Function	KSZ8091RNB (0.11um) Name	Type	Function
INTRP / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.	INTRP / NAND_Tree#	Ipu/Opu	**Sames as KSZ8051RNL (0.13um)**	INTRP / NAND_Tree#	Ipu/Opu	**Sames as KSZ8051RNL (0.13um)**	INTRP / PME_N2 / NAND_Tree#	Ipu/Opu	Interrupt Output: Programmable Interrupt Output PME_N Output: Programmable PME_N Output (pin option 2) This pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: The pull-up/pull-down value is latched as NAND Tree# at the de-assertion of reset.
NC	O	No connect- It is recommended to tie this unused pin directly to ground.	NC	O	**Sames as KSZ8051RNL (0.13um)**	NC	O	**Sames as KSZ8051RNL (0.13um)**	PME_EN	Ipd/O	Config Mode: The pull-up/pull-down value is latched as PME_EN at the de-assertion of reset.
LED0 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during power-up / reset.	LED0 / NWAYEN	Ipu/O	**Sames as KSZ8051RNL (0.13um)**	LED0 / NWAYEN	Ipu/O	**Sames as KSZ8051RNL (0.13um)**	LED0 / PME_N1 / NWAYEN	Ipu/O	LED Output: Programmable LED0 Output / PME_N Output: Programmable PME_N Output (pin option 1) In this mode, this pin has a weak pull-up, is open drain like, and requires an external 1.0KΩ pull-up resistor. Config Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) at the de-assertion of reset.
LED1 / SPEED	Ipu/O	LED Output: Programmable LED1 Output / Config Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset.	LED1 / SPEED	Ipu/O	**Sames as KSZ8051RNL (0.13um)**	LED1 / SPEED	Ipu/O	**Sames as KSZ8051RNL (0.13um)**	LED1 / SPEED	Ipu/O	**Sames as KSZ8051RNL (0.13um) and KSZ8081RNB (0.11um)**

Symbol	Parameter	Condition	Min	Typ	Max	Units
KSZ8051MNL All Pull-Up / Pull-Down Pins (including Strapping Pins)						
ipu	Internal Pull-up Resistance	V_{DDIO} = 3.3V	29	43	76	KΩ
		V_{DDIO} = 2.5V	37	59	102	KΩ
		V_{DDIO} = 1.8V	57	100	187	KΩ
ipd	Internal Pull-down Resistance	V_{DDIO} = 3.3V	27	43	76	KΩ
		V_{DDIO} = 2.5V	35	60	110	KΩ
		V_{DDIO} = 1.8V	55	100	190	KΩ

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KSZ8081MNX All Pull-Up/Pull-Down Pins (including Strapping Pins)						
ipu	Internal Pull-Up Resistance	V_{DDIO} = 3.3V	30	45	73	kΩ
		V_{DDIO} = 2.5V	39	61	102	kΩ
		V_{DDIO} = 1.8V	48	99	178	kΩ
pd	Internal Pull-Down Resistance	V_{DDIO} = 3.3V	26	43	79	kΩ
		V_{DDIO} = 2.5V	34	59	113	kΩ
		V_{DDIO} = 1.8V	53	99	200	kΩ

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KSZ8081RNB All Pull-Up/Pull-Down Pins (including Strapping Pins)						
ipu	Internal Pull-Up Resistance	V_{DDIO} = 3.3V	30	45	73	kΩ
		V_{DDIO} = 2.5V	39	61	102	kΩ
		V_{DDIO} = 1.8V	48	99	178	kΩ
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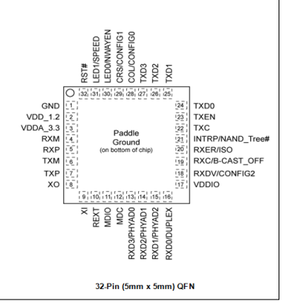
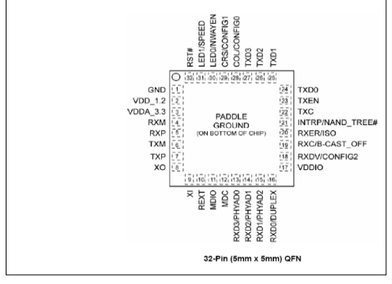
		V_{DDIO} = 1.8V	53	99	200	kΩ

Pin Configuration – KSZ8051MNL



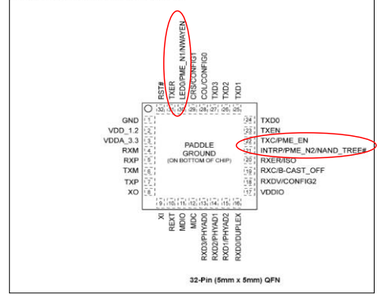
32-Pin (5mm x 5mm) QFN

Pin Configuration– KSZ8081MNX



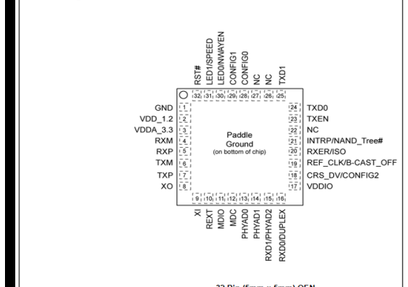
32-Pin (5mm x 5mm) QFN

Pin Configuration – KSZ8091MNX



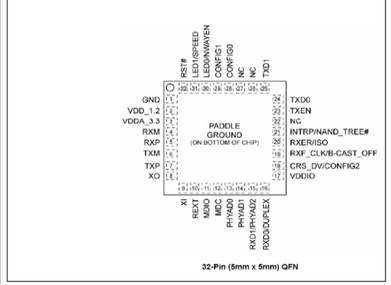
32-Pin (5mm x 5mm) QFN

Pin Configuration – KSZ8051RNL



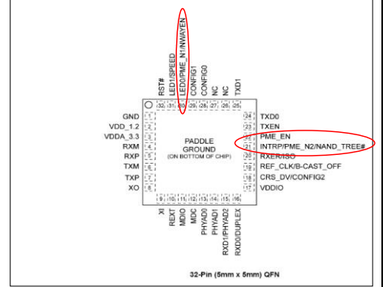
32-Pin (5mm x 5mm) QFN

Pin Configuration – KSZ8081RNB



32-Pin (5mm x 5mm) QFN

Pin Configuration – KSZ8091RNB



32-Pin (5mm x 5mm) QFN