KSZ8051 to KSZ8081/KSZ8091 (32-QFN) -- Hardware Differences

Hardware Pin Differences: Tabulated are only pin differences between parts (pins common to all parts are not shown) Internal pull-up/pull-down values for the strapping pins are indicated after table

Rev 1.0 Created

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	KSZ8051MNL (0.13um)				KSZ8081MNX (0.11um)			KSZ8091MNX (0.11um)		KSZ8051RNL (0.13um)		KSZ8081RNB (0.11um)		KSZ8091RNB (0.11um)	
Pin #	Name	Туре	Function	Name	Туре	Function	Name	Type Function	Name	Type Function	Name Type	Function	Name	Type Function	
21	INTRP / NAND_Tree#	lpu/Opu	Interrupt Culput. Programmable Interrupt Culput. This pin has a weak pul-up, is open drain like, and requires an external 1.0KD pull-up resistor. Corfig Mode: The pull-uppull-down value is intched as NAMD Trees at the de-assertion of reset.	INTRP / NAND_Tree#	lpulOpu	Sames as KS28051MNL (0.13um)	INTRP / PME_N2 / NAND_Tree#	interrupt Cutput: Programmable Interrupt Cutput PME, IV Cutput: Programmable PME, IV Cutput (pin option 2) PME, IV Cutput: Programmable PME, IV Cutput (pin option 2) Cutput (pin be as weak) puture, open of pain like, and requires an external 1 CMD put-up resistor. Curflig Mode: This put-upplut-down value is latched as NANIO Tread at the de-assertion of reset.	INTRP /	Interrugt Output Programmable Interrugt Output This pin thas a week pulsus, is open drain like, and requires an external 1.0KD pulsup resistor. Corflig Mode: The pulsupplud-down value is bished as NAND Tirest at the de-assertion of reset. NAND	/ Ipu∕Opu Tree#	Sames as KS23051RNL (0.13um)	INTRP / PME_N2 / NAND_Tres#	purOpu Pide Andre Programmable Heler (A) Output (pin option 2) Pide (A) Output Programmable Heler (A) Output (pin option 2) The pin has a weak play, in open dan like and requires an external 1.0KΩ pulsup resistor. Curling Mode: The pull-opplut-down value in bitched as NAND Tread at the dis-assertion of resot.	
22	TXC	I/O	Mil Mode: Mil Transmit Clock Output Mil Back-to-Back Mode: Mil Transmit Clock Input	TXC (pin 22)	Ю	Mil mode: Mil Transmit Clock output Note: All the descention of react, this pin needs to latch in a pail-down value for normal At the one TMAN (do plats this pin help, RPY will gone to factory rest mode, see Register 16h, set Bit (15)-V for solution. Or an external pull-down resistor is recommended.	TXC / PME_EN	Mill Moder Mill Transent Clock Output (bd) Mill Black de Black Moder. Mill Transent Clock Input Config Moder. The pulk-upplut-down value is batched as PME_EN at the de-assertion of reset.	NC	O No connect- it is recommended to lie this unused pin directly to ground. NC	0	Sames as KS23051RNL (0.13um)	PME_EN	(xdO Corfig Mode: The pull-opjoul-down value is batched as PME_EN at the .de-assertion of roset.	
30	LEDO / NWAYEN	lpu/O	LED Output: Programmable LEDO Cutput / Config Mode: Latched as Auto-Negotiation Enable (register 0%, bit 12) during _power-up / reset.	LED0 / NWAYEN	lpu/O	Samus as KSZ8051MNL (0.12um)	LEDO/ PME_N1/ NWAYEN	LED Output: Programmable LED Output / PME_IN Output (Programmable PME_IN Output (pin option 1) PME_IN Output (Programmable PME_IN Output (pin option 1) In the mode, this just has a week jud-in, is open option (PME_IN Output option) Confra Medica Listender als, Amely Reposition Finale Reposition (Finale Reposition Finale Reposition	LEDO / NWAYEN	puriO LED Output: Programmable LEDO Output / Cortig Mode: Latched as Auto-Negotiation Enable (register 0h, bit 12) during: power-up / reset. NWAY	Ipu/O EN	Sames as KS2001PNL (0.13um)	LEDO / PME_N1 / NWAYEN	bud EED Cutput: Programmable EED Cutput / pud PME_IN Cutput: Programmable PME_IN Cutput (pin option 1) In the mobil, this pin has a week place, in open draw file, and requires an external 1.000 puls-op resistor. Conf	
31	LED1/ SPEED	O'uql	LED Output: Programmable LED1 Output / Conflig Mode: Latched as SPEED (register 0h, bit 13) during power-up / reset.	LED1 / SPEED	lpu/O	Sames as KSZ8051MNL (0.13um)	TXER	lpd MII Mode: MII Transmit Error Input	LED1 / SPEED	LED Output: Programmable LED1 Output / LED1 / LPD1 / Conflig Mode: Latched as SPEED (register 0h, bit 13) at the de-assertion of reset. SPEEL	lpu/O	Sames as KSZ8051RNL (0.13um)	LED1 / SPEED	lpuO Sames as KSZ8051RNL (0.13um) and KSZ8081RNB (0.11um)	
	KS COI	Internal Pu	Vector Condition Vector		su Internal i	er Condition Min 7pm Max. Units Min 1pm Max. Units Units Min 1pm Max. Units Units Min 1pm Max. Units Min 1pm	DM pd	Parameter Condition Min. 1 Typ. Max. Wins		both Parameter Condition Min Type Max Units Infermal Pul-seg Resistance Voces 2 3V 29 43 76 KZ Voces 1 3V 29 43 76 KZ Voces 1 3V 27 59 162 XZ Voces 1 3V 57 150 187 KZ Infernal Pul-down Resistance Voces 2 3V 27 43 76 KZ Voce 2 3V 35 60 110 KZ Vcces 1 3V SS 55 100 160 KZ	Du Internal F	Lipshi4D come Fee Seculating Stargage Prival	в В	Symbol Parameter Condition Min. Typ. Mar. Usits K5209118881 AP Ltd Light Housen Pleas Chemider Seagning Pleas To 200 AP Ltd Light Housen Pleas Chemider Seagning Pleas 30 45 72 12 </th	
	Pin Confis	guration -	- KSZ8051MNL - MSZ8051MNL -	Pin Co	onfiguration	TXM ECONOMICS CONTROL OF CHIPPER	Pin Config	Substitution – KSZ8091MNX Substitution Substit	Pin Config	P P P P P P P P P	in Configuration	SECOND STATE OF STATE	Pin C	TXDD AND AND AND AND AND AND AND	

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