



8-bit **AVR**[®]
Microcontrollers

Application Note

AVR083: Replacing ATmega163 by ATmega16

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1 Introduction

This application note is a guide to assist current ATmega163 users in converting existing designs to the ATmega16. In addition to the functional changes, the electrical characteristics of the ATmega16 are different including an increase in operating frequency because of a change in process technology. Check the data sheet for detailed information.

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2 ATmega163 Errata Corrected in ATmega16

The following items from the Errata Sheets of the ATmega163 do not apply to the ATmega16. Refer to the ATmega163 Errata Sheet for a more detailed description of the Errata.

Note: Some of these errata entries were corrected in the last revision of ATmega163. They are still referred, to ease converting from any ATmega163 design.

2.1 Increased Interrupt Latency

In ATmega16, all instructions are interruptible, and no dead-lock situation exists if a loop is followed by a two-word instruction for the purpose of looping until an interrupt goes active.

2.2 Interrupts Abort TWI Power-down

The TWI Power-down operation is no longer interrupted by other interrupts, and the TWI does not return to its idle state when interrupts occur during Power-down.

2.3 TWI Master Does not Accept Spikes on Bus Lines

In ATmega16, a digital filter eliminates problems with spikes triggering a false start condition. In addition, if a start condition is incorrectly received it will now generate the status code Bus Error and set TWINT when the SDA line goes to the idle state. Hence, the previous dead-lock situation has been eliminated.

2.4 TWCR Write Operation Ignored when Immediately Repeated

In ATmega16 consecutive write operations to the TWCR Register work as expected, and there is no need to insert a NOP in between.

2.5 PWM not Phase Correct

All Timers in ATmega16 have been redesigned to generate phase correct PWM

2.6 TWI is Speed Limited in Slave Mode

The speed limit in Slave mode does not apply to ATmega16. In ATmega16, the CPU clock frequency in the slave must be at least 16 times higher than the SCL frequency, as described in the data sheet.

3 Changes to Names

The following control bits have changed names, but have the same functionality and placement when accessed as in ATmega163:

Table 3-1. Changed Bit Names

Bit Name in ATmega163	Bit Name in ATmega16	I/O Register (ATmega163)	Comments
PWMn(0)	WGMn0	TCCRn(A)	"A" and "0" in 16-bit timer only
PWMn1	WGMn1	TCCRnA	
CTCn	WGMn2	TCCRn(B)	"B" in 16-bit timer only
CHR9	UCSZ2	USCRB	
OR	DOR	UCSRA	
ASB	RWWSB	SPMCR	
ASRE	RWWSRE	SPMCR	
ADFR	ADATE	ADCSR	

The following I/O Registers have changed names, but include the same functionality and placement when accessed as in ATmega163:

Table 3-2. Changed Register Names

Register Name in ATmega163	Register Name in ATmega16	Comments
GIMSK	GICR	
MCUSR	MCUCSR	
UBRRHI	UBRRH	I/O location gives access to two registers. See "Improvements to UART" on page 4
UBRR	UBRRL	
ADCSR	ADCSRA	

4 Improvements to Timer/Counters

For details about the improved and additional features, please refer to the data sheet. The following features have been added:

- Variable top value in PWM mode.
- Timer/Counter0 extended with compare function and PWM.
- For Timer/Counter1, Phase and Frequency Correct PWM mode in addition to the Phase Correct PWM mode.

4.1 Updating of OCR in PWM mode (Applies to all Timer/Counters)

In PWM mode, the value written to the Output Compare Register is not physically used as compare value until the Timer/Counter reaches the value TOP. The interpretation of this point of time differs between ATmega163 and ATmega16. In ATmega163, the new OCR value is used in the cycle where the Timer/Counter has the value TOP. In ATmega16, the counter value TOP is used to update the compare value, i.e., it is first active in the cycle where the Timer/Counter has the value TOP-1 down-counting.





5 Improvements to ADC

The ADC in ATmega16 supports differential and amplified measurements.

6 Improvements to UART

The UART in ATmega163 has been replaced by a USART in ATmega16. The ATmega16 USART is compatible with the ATmega163 UART with one exception: The two-level Receive Register acts as a FIFO. The following must be kept in mind:

- A second buffer register has been added. The two buffer registers operate as a circular FIFO buffer. Therefore the UDR must only be read once for each incoming data. More important is the fact that the Error Flags (FE and DOR) and the ninth data bit (RXB8) are buffered with the data in the receive buffer. Therefore the status bits must always be read before the UDR Register is read. Otherwise the error status will be lost since the buffer state is lost.
- The Receiver Shift Register can now act as a third buffer level. This is done by allowing the received data to remain in the Serial Shift Register if the buffer registers are full, until a new start bit is detected. The USART is therefore more resistant to Data OverRun (DOR) error conditions.

The UBRRHI Register is placed at the same address on both devices. However, the address is shared by the UCSRC Register in ATmega16. The URSEL bit selects between accessing the UBRRH or the UCSRC Register at this address. Since writing the URSEL bit to zero selects the UBRRH register, this behavior is backward compatible to the ATmega163.

Another minor difference is the initial value of RXB8, which is "1" in the UART in ATmega163 and "0" in the USART in ATmega16.

7 Changes to Electrical Characteristics

The ATmega16 is produced in a different process than the ATmega163 and electrical characteristics will thus differ between these devices. Please consult the data sheets for further details on electrical characteristics.

8 Changes to EEPROM Write Timing

In ATmega163, the EEPROM write time takes 2,048 cycles of the calibrated RC Oscillator. In ATmega16, the EEPROM write time takes 8,448 cycles of the calibrated RC Oscillator. This is in both devices regardless of the clock source and frequency of the system clock. The calibrated RC Oscillator is assumed to be calibrated to 1.0 MHz in both devices.

Note: Changing the value in the OSCCAL Register affects the frequency of the calibrated RC Oscillator and hence the EEPROM write time.

9 Programming Interface

The Parallel Programming algorithm is changed. In Parallel mode, the ATmega16 supports page programming of the EEPROM. The timing requirements for Parallel Programming have been changed. See the ATmega16 data sheet for details.

The STK500 supports both In-System Programming and Parallel Programming of the ATmega16.

10 Fuse Settings

ATmega16 contains more fuses than ATmega163. Table 3 shows the ATmega163 compatible Fuse settings. Some of the fuses are described further in the following sections.

Table 10-1. Comparing Fuses in ATmega163 and ATmega16⁽¹⁾

Fuse	Default ATmega163 Setting	Default ATmega16 Setting	ATmega163 Compatible Setting
OCDEN	–	1	1
JTAGEN	–	0	1 ⁽²⁾
SPIEN	0	0	0
CKOPT	–	1	0 ⁽³⁾
EESAVE	1	1	1
BOOTSZ1	1	0	1
BOOTSZ0	1	0	1
BOOTRST	1	1	1
BODLEVEL	1	1	1
BODEN	1	1	1
SUT1	–	1	See note ⁽⁴⁾
SUT0	–	0	See note ⁽⁴⁾
CKSEL3	0	0	See note ⁽⁴⁾
CKSEL2	0	0	See note ⁽⁴⁾
CKSEL1	1	0	See note ⁽⁴⁾
CKSEL0	0	1	See note ⁽⁴⁾

- Notes:
1. A dash indicates that the Fuse is not present in ATmega163
 2. See “JTAG Interface” on page 6
 3. See “Oscillators and Selecting Start-up Delays” on page 6
 4. The CKSEL Fuses are available in both ATmega163 and ATmega16. However, the SUT and CKSEL setting should be reconsidered when moving to ATmega16. See “Oscillators and Selecting Start-up Delays” on page 6



11 Oscillators and Selecting Start-up Delays

In ATmega163, the CKSEL Fuses selects both which Oscillator is active, and the duration of the Start-up delay. In ATmega16, the active Oscillator and its frequency range is selected by the CKSEL Fuses, while the SUT Fuses selects Start-up delay for the given Oscillator. Hence, the CKSEL Fuse setting from ATmega163 must be reconsidered when moving to ATmega16. Follow the guidelines from the section "System Clock and Clock Options" in the ATmega16 data sheet to find appropriate start-up values.

The crystal Oscillator in ATmega163 is capable of driving an addition clock buffer from the XTAL2 output. In ATmega16, this is only possible when the CKOPT Fuse is programmed. In this mode the Oscillator has a rail-to-rail swing at the output, but at the expense of higher power consumption. Hence, do only program this fuse when rail-to-rail swing is required.

12 Changes to Watchdog Timer

The frequency of the Watchdog Oscillator in ATmega16 is close to 1.0 MHz for all supply voltages. The typical frequency of the Watchdog Oscillator in ATmega163 is close to 1.0 MHz at 5V, but the Time-out period increases with decreasing VCC. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATmega16. Refer to the data sheet for ATmega16 for further information.

13 JTAG Interface

The ATmega16 provides a JTAG interface, which can be used for programming, boundary-scan, and On-chip debug. Refer to data sheet for details. The device is shipped with the JTAGEN Fuse programmed in order to allow programming through the JTAG interface. This fuse must be erased to be ATmega163 compatible (If not, four pins are dedicated to the Test Access Port – TAP instead of being I/O pins).

Note that if the On-chip Debug System is enabled, the main clock will continue running in all sleep modes. This will contribute significantly to the total current consumption. Therefore the OCDEN fuse should be disabled if not needed.

14 Self-Programming

Both ATmega16 and ATmega163 supports Self-Programming. In ATmega163 the CPU is halted both during Page Erase and during Page Write. In ATmega16, the CPU is only halted when programming the No-Read-While-Write – NRWW – section of the Flash memory. The SPMEN bit in the SPMCR Register will be auto-cleared in both devices. This means that a Boot Loader for ATmega163 can be written without polling for completion of the erase or the write operation. If this is the case, porting the code to ATmega16 requires rewriting the code to poll for SPMEN to go low before starting a new page erase, page write or writing the Lock bits command.

When the Read-While-Write – RWW – section in the ATmega16 has been erased or written to, it has to be re-enabled before reading it. A similar recommendation is specified for the ATmega163, though this is only needed for compatibility with future devices. The ATmega163 can actually read from the RWW section though it has not been enabled (since this happens automatically). This is not the case for the ATmega16: The RWW section must be enabled to be able to read from it after SPM access. An ATmega163 code may therefore execute differently, most likely incorrectly, on an ATmega16 if recommendations regarding enabling of the RWW section in the ATmega163 data sheet have not been followed. Refer to the data sheet regarding enabling of the RWW section. Further, note the changes to the bit-names in the SPMCR Register (see Table 3-1, “Changed Bit Names” on page 3).

However, the data sheet for ATmega163 recommends this polling operation for compatibility with future devices, so as long as this recommendation is followed, the Boot Loader can be used in ATmega16 without modification.

15 Other Concerns

The ATmega16 has a signature byte different from the one used in ATmega163. Make sure you are using the signature byte of ATmega16 when porting the design.

Be aware that EEPROM write access must be completed before entering power-down sleep mode. Otherwise the system oscillator will continue to run, drawing additional current.



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