MCP2518FD

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Silicon Errata and Data Sheet Clarification

The functionality of the MCP2518FD devices is described in the Device Data Sheet (DS20006027), except for the anomalies described below.

1. Module: SPI Module

Incorrect data for certain READ/READ_CRC commands:

There is a possibility that the transmitted data on a READ/READ_CRC is wrong when reading from the chip. A glitch on the SDO line shorter than 1 bit in length occurs and creates wrong data.

Fix/Work Around

Only use the READ_CRC command and if a CRC mismatch occurs, re-issue the READ_CRC command.

The following registers may be affected:

CiTXIF

CiRXIF

CiCON

CiTBC

CiINT

CiRXOVIF

CiTXATIF

CiTXREQ

CiTREC

CiBDIAG0

CiBDIAG1

CiTXQSTA

CiFIFOSTAm

The occurrence can be minimized by not using FIFOs 7/15/23/31.

Bit 31 of RAM reads may also be affected. This can be avoided by reading from a receive FIFO only after the message has been loaded into the FIFO, indicated by the receive flags. This is the recommended procedure independent of the issue described here.

2. Module: ECC Module

ECC Single Error Correction does not work in all cases.

Fix/Work Around:

Enable Single Error Correction (SEC) and Double Error Detection (DED) interrupts by setting SECIE and DEDIE. Handle SECIF as a detection interrupt and do not rely on the error correction. Instead, handle both interrupts as a notification that the RAM word at ERRADDR was corrupted.

3. Module: SPI Module

SFR address rollover does not work:

The SFR address rollover, from 0x3FF to 0x000 and from 0xFFF to 0xE00, does not work. Instead, the address changes from 0x3FF to 0x400 and from 0xFFF to 0x000.

The address rollover for the RAM works as described.

Fix/Work Around:

None.

4. Module: SPI/RAM Module

The SPI may write corrupted data to the RAM at fast SPI speeds:

Simultaneous activity on the CAN bus while writing data to RAM via the SPI interface, with high SCK frequency, may lead to corrupted data being written to RAM.

Fix/Work Around:

Ensure that FSCK is less than or equal to 0.85 * (FSYSCLK/2).

5. Module: SPI/GPIO Module

Writing multiple bytes to the IOCON register using one SPI `WRITE` instruction may overwrite LAT0 and LAT1:

Writing Byte 2 and Byte 3 of the IOCON register using one SPI `WRITE` instruction clears LAT0 and LAT1.

Fix/Work Around:

When setting LAT0 or LAT1, do not use a multi-data byte SPI `WRITE` instruction.

Instead, write the bit fields in the IOCON register using single data byte SFR `WRITE` instructions.

6. Module: SPI Module

The reading of the FIFOCI bits in the FIFOSTA register may be corrupted:

The reading of the FIFOCI bits in the FIFOSTA register for an RX FIFO may be corrupted if a certain timing is met with regards to a frame on the CAN bus. The generated CRC matches the false data. A subsequent `READ` will return the correct FIFOCI.

Fix/Work Around:

Perform multiple read-outs to detect unexpected data.

7. Module: SPI/Device

Failed wake up when clearing OSCDIS:

When waking up the device by clearing the OSCDIS bit, it is possible to hit a timing window where the wake up will fail. The device will wake up briefly and go back to sleep again.

Fix/Work Around:

1. Prolong the TSCK2NCS/Byte2Byte timing to at least 50 TSYSCLK cycles depending on whether regular Write commands or CRC/Write-safe commands are used. The delay needs to be after the byte containing the OSCDIS bit.
2. When polling OSCRDY to determine whether the device woke up already, ensure that two back-to-back reads of the bit show it as '`1`' to qualify for a successful wake up. If the second read returns a '`0`', repeat the wake up sequence by writing OSCDIS to '`0`' again.

Clarifications/Corrections to the Data Sheet

In the MCP2518FD Data Sheet (DS20006027**B**), the following clarifications and corrections should be noted:

1. Register 3-3: CRC - CRC Register

The bit `FERRIF` (bit 17) may be set on illegal SPI transactions if the last successful transfer was one of the following commands: `READ_CRC`, `WRITE_CRC` or `WRITE_SAFE`. One example is the CS line going low, and going up again without any activity on the SCK line.

This will generate a Format error and needs to be handled by clearing the error bit in the CRC Register.

APPENDIX A: REVISION HISTORY

Revision F (January 2025)

- Added **SPI/Device** (entry no. 7).

Revision E (November 2023)

- Clarification of Register 3-3: CRC - CRC Register was added to **Section "Clarifications/Corrections to the Data Sheet"**.
- Added **SPI Module** (entry no. 6).

Revision D (July 2022)

- Corrections added to **SPI Module**.

Revision C (October 2020)

- Corrections added to **SPI Module**.

Revision B (September 2020)

- Added **ECC Module**, **SPI Module**, **SPI/RAM Module** and **SPI/GPIO Module**.

Revision A (May 2018)

- Initial Release of this Document.

NOTES:

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ISBN: 979-8-3371-0448-5

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