3.2Gbps Dual Channel CML Programmable Delay

SY89297U Evaluation Board

General Description

The SY89297U evaluation board is designed for convenient setup and quick evaluation. The board is optimized to interface directly to a 50Ω oscilloscope.

For best AC performance, the board is configured in AC-coupled configuration.

Datasheet and support documentation can be found on Micrel's web site at: www.micrel.com.

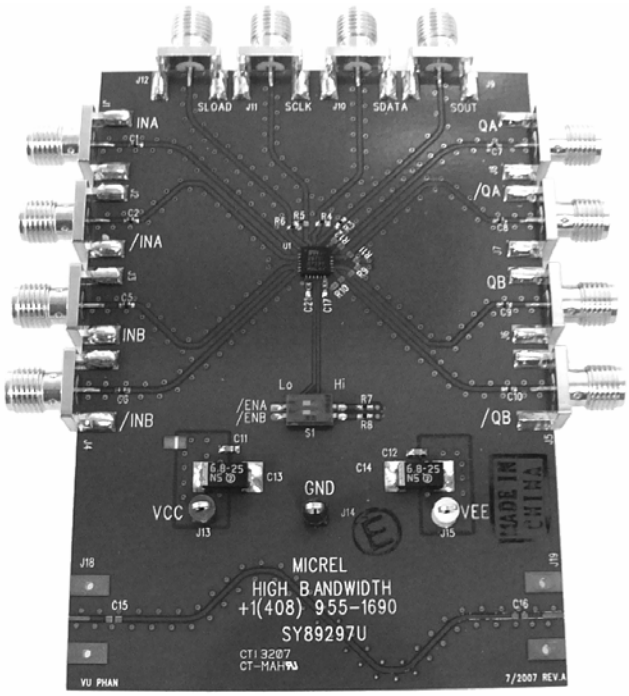
Features

- 5ps step delay
- +2.5V or +3.3V power supply
- AC-coupled configuration
- Serial control interface

Related Documentation

- SY89297U, 2.5/3.3V 3.2Gbps Dual-channel CML Programmable Delay Line Datasheet

Evaluation Board



Evaluation Board Description

The SY89297U evaluation board has a 3.2Gbps Dual-Channel CML delay line mounted on it. It comes with default AC-coupled configuration.

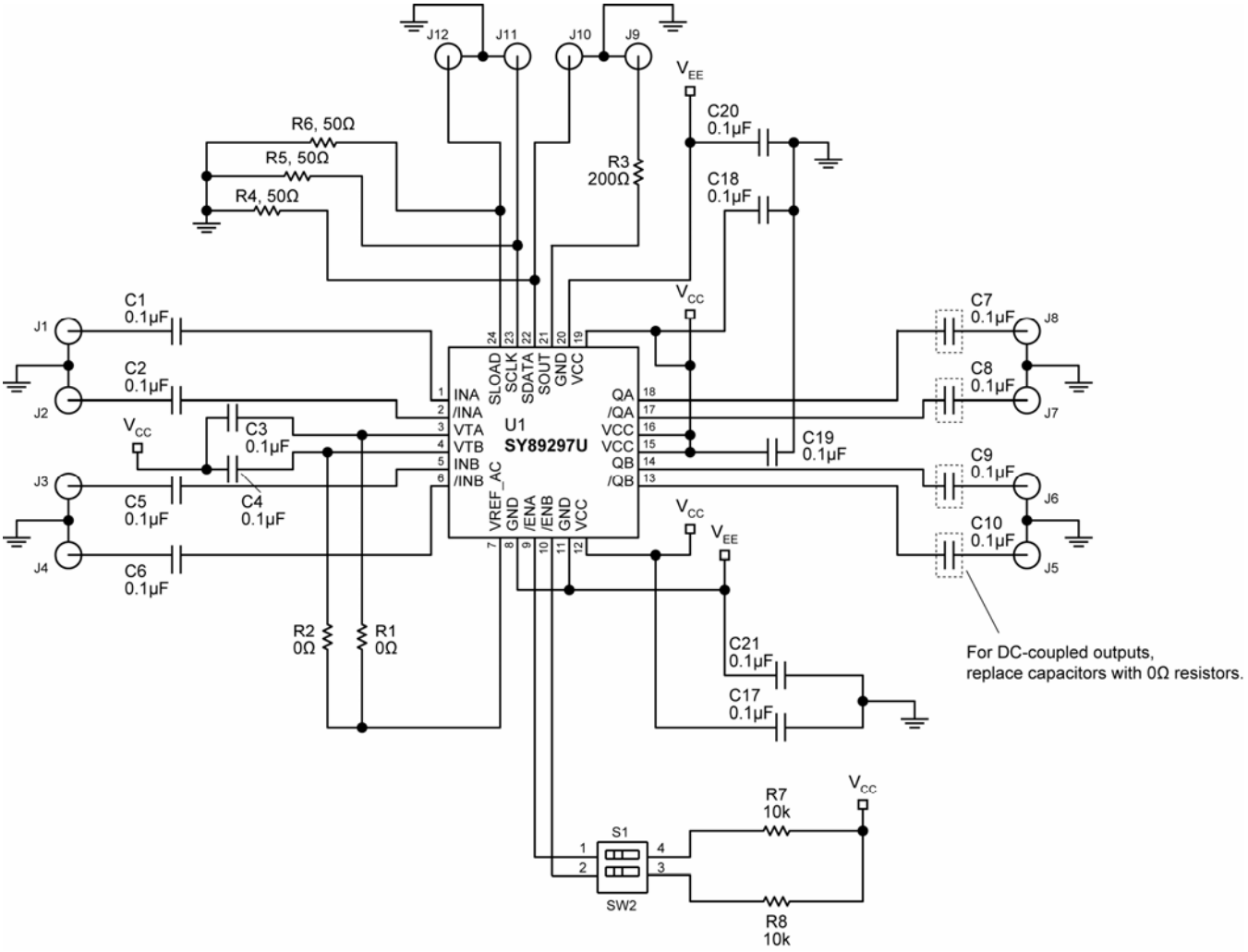
AC-Coupled Output

The AC-coupled configuration is suited to most customer applications and is preferred by the majority of users because of its ease-of-use. It requires only a single power supply and offers the most flexibility in interfacing to a variety of signal sources.

The DC-bias levels and AC-coupling capacitors are supplied on-board for each input, making it unnecessary to vary the offset voltage or change any components on the board as the power supply voltage varies over the +2.5V ±5% and +3.3V ±10% operating range. The user only needs to supply a minimum input voltage swing and the bias voltage will automatically adjust the input to the correct level as the power supply voltage varies.

Delay Control Programming: SCLK, SDATA, and SLOAD are CMOS/TTL compatible 3-pin serial programming control pins for both channels. To program the two channels, insert a 20-bit word into SDATA. Insert a reference 40MHz reference clock in SCLK pin. Data is loaded into the serial registers on the low-to-high transition of SCLK. SLOAD controls the latches that transfer scanned data to the delay line. These latches are transparent when SLOAD is high. Data is transferred from the latch to the delay line on a low-to-high transition of SLOAD. SLOAD has to transition high-to-low before new data is loaded in the scan chain. The latches are transparent when SLOAD is high and SCLK cannot switch at this time otherwise new data will immediately transfer to the scan chain. For more details, refer Pin Description and Timing Diagrams in the datasheet.

Evaluation Board Schematic



SY89297U AC-Coupled CML Evaluation Board

I/O	Power Supply	V_{CC}	GND	V_{EE}
AC-In/AC-Out	2.5V	+2.5V	0	0
AC-In/AC-Out	3.3V	+3.3V	0	0
AC-In/DC-Out	2.5V	+2.5V	+2.5V	0
AC-In/DC-Out	3.3V	+3.3V	+3.3V	0

Table 1. SY89297U Power Pin Configuration

Note: AC-In/DC-Out is the default configuration

AC-Coupled Evaluation Board Setup

The following steps describe the procedure for setting up the evaluation board:

1. Set the voltage setting for a DC supply to either 2.5V or 3.3V, depending upon your application.
2. Using a differential signal source, set the amplitude of each side of the differential pair to 400mV. The same holds true if you are planning to use both channels and independently delay different signals.
3. Using equal length 50Ω impedance coaxial cables, connect the signal generator to the input. Using equal length 50Ω impedance coaxial cables, connect the outputs of the evaluation board to a scope. To get a longer delay, you can feed the output from one channel to the input of another. For delay control, connect a signal source to SLOAD, SDATA, and SCLK using equal 50Ω cables. Unequal length cables are not recommended since they introduce duty cycle distortion and unwanted signal delays.

4a. For AC-coupled application, connect V_{CC} to positive power supply, and GND and V_{EE} to negative side of the supply.

4b. For DC-coupled applications, replace C7-C10 with 0Ω resistors. Connect V_{CC} and GND to positive power supply, and V_{EE} to the negative side.

5. Enable the signal source and monitor the outputs.

Evaluation Board Layout

PC Board Layout

The evaluation boards are constructed with Rogers 4003 material and are coplanar in design fabricated to minimize noise, achieve high bandwidth and minimize crosstalk.

Layer	SY89297U
Top	GND and Signal
L1	GND
L2	V_{CC}
L3	V_{EE}
L4	GND
Bottom	GND and Signal

Table 2. Layer Stack

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1-C12, C15-C21	VJ0402Y104KXXAT	Vishay[1]	0.1uF, 25V, 10% Ceramic Capacitor, Size 0402, X7R, Dielectric	17
R1-R3, C7-C12	CRCW040200R0F	Vishay[1]	0Ω, 1/16W Resistor SMD, Size 0402	9
C13, C14	293D106X0025C2T	Vishay[1]	10uF, 20V, Tantalum Electrolytic Capacitor, Size C	2
R4-R6, R9-R12	CRCW040249R9F	Vishay[1]	50Ω, 5%, 1/16W Resistor SMD, size 0402	7
R7, R8	CRCW04021002F	Vishay[1]	10kΩ, 1/16W, Resistor SMD, Size 0402	2
SMA1-SMA12	142-0701-851	Johnson Components[2]	Jack Assembly End Launch SMA	12
V_{CC}	5005K-ND	Keystone Electronics [3]	Red Test-point	1
GND	5006K-ND	Keystone Electronics [3]	Black Test-point	1
V_{EE}	5007K-ND	Keystone Electronics [3]	Yellow Test-point	1
SW	TDA-02	DigiKey[4]	2-Position Dip	2
U1	**SY89297U**	**Micrel, Inc.[5]**	**CML Programmable Delay**	1

Notes:

1. Vishay: www.vishay.com
2. Johnson Components: www.johnsoncomponents.com
3. Keystone Electronics: www.keyelco.com
4. DigiKey: www.digikey.com
5. **Micrel, Inc.: www.micrel.com**

HBW Support

Hotline: 408-955-1690

Email Support: HBWHelp@micrel.com

Application Hints and Notes

For application notes on high speed termination on PECL and LVPECL products, clock synthesizer products, SONET jitter measurement, and other High Bandwidth products go to Micrel's website at http://www.micrel.com/. Once in Micrel's website, follow the steps below:

1. Click on "Product Info".
2. In the Applications Information Box, choose "Application Hints and Application Notes."

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