AN2651

Configuration of Microchip USB47xx/USB49xx

Author: *Arnaldo Cruz and Mick Davis*
Microchip Technology Inc.

1.0 INTRODUCTION

The USB47xx/USB49xx can be configured:

- Via SMBus during start-up configuration stage (SOC_CFG)
- Via SMBus during hub operational stages (during runtime)
- Via One-Time Programmable (OTP) Memory
- Via a USB interface during hub operational stages (during runtime)
- Via an external SPI flash

SMBus Configuration: The hub may be configured via the SMBus Slave Interface during the hub's start-up configuration stage (called SOC_CFG). To hold the hub in the SOC_CFG stage, the CONFIG_STRAP pins must be set with the correct configuration mode (CONFIG4 or CONFIG6 for USB491x/USB492x, and CONFIG5 for USB47xx) and the SMBus slave clock and data pins must be sampled as 'high' (10k pull-up resistors to 3.3V recommended) at power-on or when RESET_N is deasserted. Once in the configuration stage, any of the registers may be reconfigured. The hub waits in SOC_CFG indefinitely until it receives the special Attach command.

After the hub has exited the SOC_CFG stage, the configuration registers may still be manipulated via SMBus. This may be useful for enabling an external SOC to control the hub's GPIOs or to check certain hub status registers.

OTP Memory: The hub's registers may be configured via the hub's internal OTP memory. Any register may be given a new default value. The OTP memory is 8 kB, and each byte within the OTP memory may be written only once. The OTP commands are loaded sequentially, so it is possible to overwrite a previously programmed register setting by programming that register subsequently with a new value. The OTP memory may be programmed via the USB interface or via SMBus.

USB Interface: All registers are accessible from the USB host using vendor-specific commands issued to the hub's internal Hub Feature Controller device.

External SPI Memory Device: If a custom firmware image is being used and executed from an attached SPI memory device, the configuration registers may also be configured within the SPI image. This method mimics the OTP configuration method and is referred to as "pseudo-OTP."

1.1 Sections

This document includes the following topics:

1.2 References

The following documents should be referenced when using this application note:

- *USB4712 Data Sheet*
- *USB4715 Data Sheet*
- *USB4912 Data Sheet*
- *USB4916/USB4914 Data Sheet*
- *USB4927/USB4925 Data Sheet*
- *MPLAB® Connect Configuration Tool*
- *System Management Bus Specification, Version 1.0*

2.0 HUB OPERATIONAL MODE

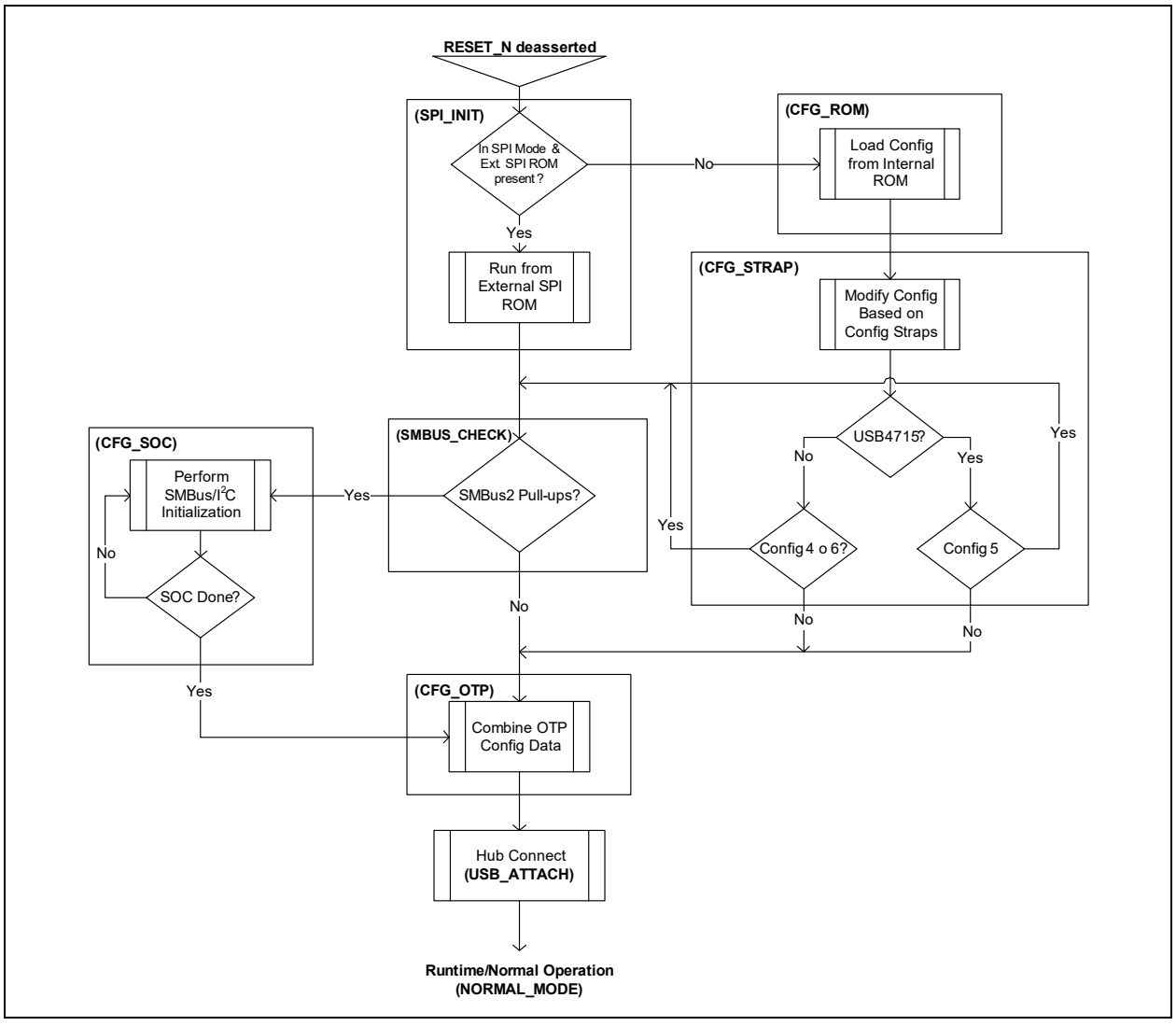
2.1 Hub Configuration Stages

The hub is configured in three stages. The SOC_CFG stage is only entered if the CONFIG_STRAP pins are set with the correct configuration mode (CONFIG4 or CONFIG6 for USB491x/USB492x and CONFIG5 for USB47xx) and the SMBus slave interface pins (data and clock) are both sampled as 'high' at start-up. During this stage, the hub allows an external SOC to configure the registers. The hub waits in SOC_CFG until it receives the special Attach command.

After SOC_CFG is complete (or if SOC_CFG is bypassed), the hub loads its OTP memory contents and manipulates the registers based on the OTP configuration. Note that in the event that SMBus manipulates a register in the SOC_CFG stage and within the OTP memory, the configuration value as set within the OTP memory takes priority.

Figure 1 explains the hub start-up flow.

FIGURE 1: HUB CONFIGURATION OPERATIONAL MODE FLOWCHART



Note:	Because the OTP Configuration registers are loaded after the SOC_CFG stage, it is possible for configuration registers modified in the SOC_CFG stage to be overwritten in the CFG_OTP stage. If a register is modified in both the SOC_CFG and OTP_CFG stages (that is, an OTP patch was programmed to the hub OTP), then the register value as written in the OTP_CFG stage takes effect.

2.2 SMBus Protocol

The SMBus protocol is a flexible 2-pin serial protocol used for low-speed communication between integrated circuits. The protocol consists of an SMBCLK pin generated by the SMBus Master and a bi-directional SMBDATA pin that can be driven by a Master or a Slave. The bus requires a pull-up resistor on both SMBCLK and SMBDATA to function. The hub configures the pins as Open/Drain buffers, where the driver either tristates the pin or drives the pin to GND. The input threshold for the high level ranges from 1.2V to 3.3V, allowing the hub to communicate with a large sample of SOCs on the market. Refer to the System Management Bus Specification for more details on the timing specifications of the bus.

3.0 REGISTER MAP

Note: It is recommended not to modify the current values of Reserved bits to avoid operation failure.

3.1 Configuration Registers (Base Address: BF80_0000h)

TABLE 1: CONFIGURATION REGISTERS MEMORY MAP

Configuration Registers			Base Address: BF80_0000h	
OFFSET	**R/W**	**Name**	**Function**	**Modification Stage**
0000h	R/W	DEV_REV	Device Revision Register	Configuration
0900h	R/W	PIO32_OEN	PIO[31:0] Output Enable Register	Runtime or Configuration
0904h	R/W	PIO64_OEN	PIO[63:32] Output Enable Register	Runtime or Configuration
0908h	R/W	PIO96_OEN	PIO[95:64] Output Enable Register	Runtime or Configuration
0910h	R/W	PIO32_IEN	PIO[31:0] Input Enable Register	Runtime or Configuration
0914h	R/W	PIO64_IEN	PIO[63:32] Input Enable Register	Runtime or Configuration
0918h	R/W	PIO96_IEN	PIO[95:64] Input Enable Register	Runtime or Configuration
0920h	R/W	PIO32_OUT	PIO[31:0] Output Register	Runtime or Configuration
0924h	R/W	PIO64_OUT	PIO[63:32] Output Register	Runtime or Configuration
0928h	R/W	PIO96_OUT	PIO[95:64] Output Register	Runtime or Configuration
0930h	R/W	PIO32_IN	PIO[31:0] Input Register	Runtime or Configuration
0934h	R/W	PIO64_IN	PIO[63:32] Input Register	Runtime or Configuration
0938h	R/W	PIO96_IN	PIO[95:64] Input Register	Runtime or Configuration
0940h	R/W	PIO32_PU	PIO[31:0] Pull-Up Resistor Register	Runtime or Configuration
0944h	R/W	PIO64_PU	PIO[63:32] Pull-Up Resistor Register	Runtime or Configuration
0948h	R/W	PIO96_PU	PIO[95:64] Pull-Up Resistor Register	Runtime or Configuration
0950h	R/W	PIO32_PD	PIO[31:0] Pull-Down Resistor Register	Runtime or Configuration

TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
OFFSET	**R/W**	**Name**	**Function**	**Modification Stage**
0954h	R/W	PIO64_PD	PIO[63:32] Pull-Down Resistor Register	Runtime or Configuration
0958h	R/W	PIO96_PD	PIO[95:64] Pull-Down Resistor Register	Runtime or Configuration
0960h	R/W	PIO32_OD	PIO[31:0] Open Drain Mode Register	Runtime or Configuration
0964h	R/W	PIO64_OD	PIO[63:32] Open Drain Mode Register	Runtime or Configuration
0968h	R/W	PIO96_OD	PIO[95:64] Open Drain Mode Register	Runtime or Configuration
09E0h	R/W	PIO32_DEB	PIO[31:0] Debounce Register	Runtime or Configuration
09E4h	R/W	PIO64_DEB	PIO[63:32] Debounce Register	Runtime or Configuration
09E8h	R/W	PIO96_DEB	PIO[95:64] Debounce Register	Runtime or Configuration
09F0h	R/W	GPIO_DEBOUNCE	GPIO[31:0] Debounce Register	Runtime or Configuration
3000h	R/W	VID_LSB	Vendor ID LSB	Configuration
3001h	R/W	VID_MSB	Vendor ID MSB	Configuration
3002h	R/W	PID_LSB	Product ID LSB	Configuration
3003h	R/W	PID_MSB	Product ID MSB	Configuration
3004h	R/W	DID_LSB	Device ID LSB	Configuration
3005h	R/W	DID_MSB	Device ID MSB	Configuration
3006h	R/W	HUB_CFG1	Hub Configuration Data Byte 1	Configuration
3007h	R/W	HUB_CFG2	Hub Configuration Data Byte 2	Configuration
3008h	R/W	HUB_CFG3	Hub Configuration Data Byte 3	Configuration
3009h	R/W	HUB_NRD	Hub Non-Removable Device	Configuration
300Ah	R/W	PORT_DIS_S	Port Disable – Self Powered	Configuration
300Bh	R/W	PORT_DIS_B	Port Disable – Bus Powered	Configuration
300Ch	R/W	H_MAXP_S	Hub Max Power – Self Powered	Configuration
300Dh	R/W	H_MAXP_B	Hub Maximum Power – Bus Powered	Configuration
300Eh	R/W	HC_MAXP_S	Hub Controller Maximum Current – Self Powered	Configuration
300Fh	R/W	HC_MAXP_B	Hub Controller Maximum Current – Bus Powered	Configuration
3010h	R/W	PWR_ON_TIME	Power-On Time Register	Configuration
3013h	R/W	MFR_STR_INDEX	Manufacturer String Index Register	Configuration
3014h	R/W	PRD_STR_INDEX	Product String Index Register	Configuration
3015h	R/W	SER_STR_INDEX	Serial String Index Register	Configuration
30D0h	R	BC_EN	Battery Charging Enable Status Register	Runtime (hub)
30E1h	R/W	OCS_LOCKOUT	Start OCS Lockout Timer Register	Configuration
30E5h	R	PORT_PWR_STAT	Port Power Status	Runtime (hub)
30EAh	R/W	OCS_MIN_WIDTH	OCS Minimum Width Register	Configuration
30EBh	R/W	OCS_INACTIVE_TIMER	OCS Inactive Timer	Configuration
30FAh	R/W	HUB_PRT_SWAP	Hub Port Swap Register	Configuration

TABLE 1: CONFIGURATION REGISTERS MEMORY MAP (CONTINUED)

Configuration Registers			Base Address: BF80_0000h	
OFFSET	**R/W**	**Name**	**Function**	**Modification Stage**
30FBh	R/W	HUB_PRT_REMAP_12	Hub Port Remap 12 Register	Configuration
30FCh	R/W	HUB_PRT_REMAP_34	Hub Port Remap 34 Register	Configuration
30FDh	R/W	HUB_PRT_REMAP_56	Hub Port Remap 56 Register	Configuration
30FEh	R/W	HUB_PRT_REMAP_7	Hub Port Remap 7 Register	Configuration
3100h	R	USB2_LINK_STATE1	USB 2 Link State 1	Runtime (hub)
3101h	R	USB2_LINK_STATE2	USB 2 Link State 2	Runtime (hub)
3104h	R/W	USB2_HUB_CTL	USB 2 Hub Control	Runtime
3108h	R/W	USB2_BCDUSB	USB 2 Version BCD[15:0]	Configuration
318Ch	R/W	CNTLP	Primary Hub Control Portable Test	Runtime
318Dh	R/W	EMBED_TEST_PORT_SEL	Embedded Primary Hub Test Port Select	Runtime
3194h	R	USB2_HUB_STAT	USB 2 Hub Status Register	Runtime (hub)
3195h	R	USB2_DN_SPEED14	USB 2 Downstream Device Speed [4-1]	Runtime (hub)
3196h	R	USB2_DN_SPEED5	USB 2 Downstream Device Speed [5]	Runtime (hub)
3197h	R	USB2_SUSP_IND	USB 2 Suspend Indicator	Runtime (hub)
398Ch	R/W	SCNTLP	Secondary Hub Control Portable Test (USB4925/USB4927)	Runtime
398D	R/W	EMBED_SEC_TEST_PORT_SEL	Embedded Secondary Hub Test Port Select	Runtime
3C00h	R/W	PORT_CFG_SEL_1	PORT 1 Port Power Select	Configuration
3C04h	R/W	PORT_CFG_SEL_2	PORT 2 Port Power Select	Configuration
3C08h	R/W	PORT_CFG_SEL_3	PORT 3 Port Power Select	Configuration
3C0Ch	R/W	PORT_CFG_SEL_4	PORT 4 Port Power Select	Configuration
3C1Ch	R/W	PORT_CFG_SEL_GANG	PORT Power Select Gang	Configuration
3C20h	R/W	USB_OCS_SEL_1	USB Port 1 OCS Source Select	Configuration
3C24h	R/W	USB_OCS_SEL_2	USB Port 2 OCS Source Select	Configuration
3C28h	R/W	USB_OCS_SEL_3	USB Port 3 OCS Source Select	Configuration
3C2Ch	R/W	USB_OCS_SEL_4	USB Port 4 OCS Source Select	Configuration
3C3Ch	R/W	GANG_OCS_SEL	Gang OCS Source Select	Configuration
60CAh	R/W	HS_P0_BOOST	USB Port 0 Boost Register	Configuration
60CCh	R/W	HS_P0_VSENSE	USB Port 0 VariSense Register	Configuration
64CAh	R/W	HS_P1_BOOST	USB Port 1 Boost Register	Configuration
64CCh	R/W	HS_P1_VSENSE	USB Port 1 VariSense Register	Configuration
68CAh	R/W	HS_P2_BOOST	USB Port 2 Boost Register	Configuration
68CCh	R/W	HS_P2_VSENSE	USB Port 2 VariSense Register	Configuration
6CCAh	R/W	HS_P3_BOOST	USB Port 3 Boost Register	Configuration
6CCCh	R/W	HS_P3_VSENSE	USB Port 3 VariSense Register	Configuration
70CAh	R/W	HS_P4_BOOST	USB Port 4 Boost Register	Configuration
70CCh	R/W	HS_P4_VSENSE	USB Port 4 VariSense Register	Configuration
74CAh	R/W	HS_P5_BOOST	USB Port 5 Boost Register	Configuration
74CCh	R/W	HS_P5_VSENSE	USB Port 5 VariSense Register	Configuration
78CAh	R/W	SEC_P1_BOOST	SEC Port 1 Boost Register	Configuration
78CCh	R/W	SEC_P1_VSENSE	SEC Port 1 Varisense Register	Configuration

3.2 Configuration Registers (Base Address: BFD2_0000h)

TABLE 2: CONFIGURATION REGISTERS MEMORY MAP

Configuration Registers			Base Address: BFD2_0000h	
OFFSET	**R/W**	**Name**	**Function**	**Recommended Modification Stage**
2856h	R/W	HFC_PID_LSB	HFC Product ID LSB	Configuration
2857h	R/W	HFC_PID_MSB	HFC Product ID MSB	Configuration
3202h	R/W	LANG_ID	LANG_ID [15:0] Language Identifier	Configuration
3204h	R/W	MFG_STR	Manufacturer String Descriptor	Configuration
3244h	R/W	PROD_STR	Product String Descriptor	Configuration
3412h	R/W	I2S_FEAT_SEL	I2S Feature Select Register	Configuration
3413h	R/W	I2S_HFEAT_SEL	I2S HID Feature Select Register	Configuration
3417h	R/W	SECH_PID_MSB	SEC Hub PID MSB	Configuration
3418h	R/W	SECH_PID_LSB	SEC Hub PID LSB	Configuration
3419h	R/W	SMBUS_OTP_RES	SMBUS OTP Result	Configuration
341Bh	R/W	OTP_UDC_ENABLE	OTP UDC Enumeration	Configuration
341Eh	R/W	HUB_DEF_PIDM	Primary Hub PID MSB	Configuration
341Fh	R/W	HUB_DEF_PIDL	Primary Hub PID LSB	Configuration
3433h	R/W	BC_LED_DIS	LED Disable	Configuration
343Ch	R/W	BC_CONFIG_P1	Port 1 Battery Charging Configuration	Configuration
343Dh	R/W	BC_CONFIG_P2	Port 2 Battery Charging Configuration	Configuration
343Eh	R/W	BC_CONFIG_P3	Port 3 Battery Charging Configuration	Configuration
343Fh	R/W	BC_CONFIG_P4	Port 4 Battery Charging Configuration	Configuration
3442h	R/W	FLEX_IN_PORT1	FLEX_IN_Port1	Configuration
3443h	R/W	FLEX_IN_PORT2	FLEX_IN_Port2	Configuration
3444h	R/W	FLEX_IN_PORT3	FLEX_IN_Port3	Configuration
3445h	R/W	FLEX_IN_PORT4	FLEX_IN_Port4	Configuration
3446h	R/W	FLEX_OUT_PORT1	FLEX_OUT_Port1	Configuration
3447h	R/W	FLEX_OUT_PORT2	FLEX_OUT_Port2	Configuration
3448h	R/W	FLEX_OUT_PORT3	FLEX_OUT_Port3	Configuration
3449h	R/W	FLEX_OUT_PORT4	FLEX_OUT_Port4	Configuration
344Ah	R/W	FLEX_PRTCTL_PORT1	FLEX_PRTCTL_Port1	Configuration
344Bh	R/W	FLEX_PRTCTL_PORT2	FLEX_PRTCTL_Port2	Configuration
344Ch	R/W	FLEX_PRTCTL_PORT3	FLEX_PRTCTL_Port3	Configuration
344Dh	R/W	FLEX_PRTCTL_PORT4	FLEX_PRTCTL_Port4	Configuration
344Eh	R/W	FLEX_VBUSDET	FLEX_VBUSDET	Configuration
344Fh	R/W	FLEX_ATTACH_DELAY	FLEX_ATTACHDELAY	Configuration
3450h	R/W	ROLE_SWITCH_DELAY	ROLESWITCHDELAY	Configuration
346Ah	R/W	MFG_STR_LEN	Manufacturer String Length	Configuration
3472h	R/W	PROD_STR_LEN	Product String Length	Configuration

Note: FLEX registers only apply to USB47xx.

3.3 PFx Function/Pin Number/PIO Register Mapping

TABLE 3: PFX TO PIN NUMBER AND PIO REGISTER MAPPING

PFx	USB4712	USB4715	USB4912	USB4914	USB4916	USB4925	USB4927	PIO	Register
	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #	Pin #		
PF1					49		49	PIO1	PIO32[1]
PF2			27	33	44	33	44	PIO2	PIO32[2]
PF3			26	32	43	32	43	PIO3	PIO32[3]
PF4	24	30	24	30	41	30	41	PIO6	PIO32[6]
PF5		29		29	40	29	40	PIO8	PIO32[8]
PF6		28		28	36	28	36	PIO10	PIO32[10]
PF7	6	11	6	11	15	11	15	PIO11	PIO32[11]
PF8					50		50	PIO64	PIO96[0]
PF9					13	10	13	PIO65	PIO96[1]
PF10				40	53		52	PIO66	PIO96[2]
PF11				41	54		53	PIO67	PIO96[3]
PF12					46		46	PIO68	PIO96[4]
PF13					45		45	PIO69	PIO96[5]
PF14					39		39	PIO70	PIO96[6]
PF15					38		38	PIO71	PIO96[7]
PF16					37		37	PIO72	PIO96[8]
PF17					26		26	PIO73	PIO96[9]
PF18					25		25	PIO74	PIO96[10]
PF19					21		21	PIO75	PIO96[11]
PF20					12		12	PIO76	PIO96[12]
PF21					52			PIO77	PIO96[13]
PF22					55			PIO78	PIO96[14]

3.3.1 REGISTER DEFINITIONS

TABLE 4: DEVICE REVISION REGISTER

DEV_REV OFFSET: 0000h RESET = B100_7804h			Device Revision Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:16	DEVID	R	Device ID: 0478h
15:8	Reserved	R	Always reads 0
7:0	REVID	R	Silicon Revision ID A0h = A0 silicon B0h = B0 silicon B1h = B1 silicon

Note: 0000h-[7:0], 0001h-[15:8], 0002h-[23:16], 0003h-[31:24]

TABLE 5: PIO[31:0] OUTPUT ENABLE REGISTER

PIO32_OEN OFFSET: 0900h RESET = 0000_0000h			PIO32 Output Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_OEN[31:0]	R/W	PIO32_OEN[x] 0 = Disabled 1 = Enabled

Note: 0900h-[7:0], 0901h-[15:8], 0902h-[23:16], 0903h-[31:24]

TABLE 6: PIO[63:32] OUTPUT ENABLE REGISTER

PIO64_OEN OFFSET: 0904h RESET = 0000_0000h			PIO64 Output Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_OEN[63:32]	R/W	PIO64_OEN[x] 0 = Disabled 1 = Enabled

Note: 0904h-[7:0], 0905h-[15:8], 0906h-[23:16], 0907h-[31:24]

TABLE 7: PIO[95:64] OUTPUT ENABLE REGISTER

PIO96_OEN OFFSET: 0908h RESET = 0000_0000h			PIO96 Output Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_OEN[95:64]	R/W	PIO96_OEN[x] 0 = Disabled 1 = Enabled

Note: 0908h-[7:0], 0909h-[15:8], 090Ah-[23:16], 090Bh-[31:24]

TABLE 8: PIO[31:0] INPUT ENABLE REGISTER

PIO32_IEN OFFSET: 0910h RESET = 0000_0000h			PIO32 Input Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_IEN[31:0]	R/W	PIO32_IEN[x] 0 = Disabled 1 = Enabled

Note: 0910h-[7:0], 0911h-[15:8], 0912h-[23:16], 0913h-[31:24]

TABLE 9: PIO[63:32] INPUT ENABLE REGISTER

PIO64_IEN OFFSET: 0914h RESET = 0000_0000h			PIO64 Input Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_IEN[63:32]	R/W	PIO64_IEN[x] 0 = Disabled 1 = Enabled

Note: 0914h-[7:0], 0915h-[15:8], 0916h-[23:16], 0917h-[31:24]

TABLE 10: PIO[95:64] INPUT ENABLE REGISTER

PIO96_IEN OFFSET: 0918h RESET = 0000_0000h			PIO96 Input Enable Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_IEN[95:64]	R/W	PIO96_IEN[x] 0 = Disabled 1 = Enabled

Note: 0918h-[7:0], 0919h-[15:8], 091Ah-[23:16], 091Bh-[31:24]

TABLE 11: PIO[31:0] OUTPUT REGISTER

PIO32_OUT OFFSET: 0920h RESET = 0000_0000h			PIO32 Output Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_OUT[31:0]	R/W	PIO32_OUT[x] 0 = Output is 0 1 = Output is 1

Note: 0920h-[7:0], 0921h-[15:8], 0922h-[23:16], 0923h-[31:24]

TABLE 12: PIO[63:32] OUTPUT REGISTER

PIO64_OUT OFFSET: 0924h RESET = 0000_0000h			PIO64 Output Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_OEN[63:32]	R/W	PIO64_OUT[x] 0 = Output is 0 1 = Output is 1

Note: 0924h-[7:0], 0925h-[15:8], 0926h-[23:16], 0927h-[31:24]

TABLE 13: PIO[95:64] OUTPUT REGISTER

PIO96_OUT OFFSET: 0928h RESET = 0000_0000h			PIO96 Output Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_OUT[95:64]	R/W	PIO96_OUT[x] 0 = Output is 0 1 = Output is 1

Note: 0928h-[7:0], 0929h-[15:8], 092Ah-[23:16], 092Bh-[31:24]

TABLE 14: PIO[31:0] INPUT REGISTER

PIO32_IN OFFSET: 0930h RESET = 0000_0000h			PIO32 Input Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_IN[31:0]	R/W	PIO32_IN[x] 0 = Input is 0 1 = Input is 1

Note: 0930h-[7:0], 0931h-[15:8], 0932h-[23:16], 0933h-[31:24]

TABLE 15: PIO[63:32] INPUT REGISTER

PIO64_IN OFFSET: 0934h RESET = 0000_0000h			PIO64 Input Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_IN[63:32]	R/W	PIO64_IN[x] 0 = Input is 0 1 = Input is 1

Note: 0934h-[7:0], 0935h-[15:8], 0936h-[23:16], 0937h-[31:24]

TABLE 16: PIO[95:64] INPUT REGISTER

PIO96_IN OFFSET: 0938h RESET = 0000_0000h			PIO96 Input Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_IN[95:64]	R/W	PIO96_IN[x] 0 = Input is 0 1 = Input is 1

Note: 0938h-[7:0], 0939h-[15:8], 093Ah-[23:16], 093Bh-[31:24]

TABLE 17: PIO[31:0] PULL-UP RESISTOR REGISTER

PIO32_PU OFFSET: 0940h RESET = 0000_0000h			PIO32 Pull-Up Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_PU[31:0]	R/W	PIO32_PU[x] 0 = Pull-up disabled 1 = Pull-up enabled

Note: 0940h-[7:0], 0941h-[15:8], 0942h-[23:16], 0943h-[31:24]

TABLE 18: PIO[63:32] PULL-UP RESISTOR REGISTER

PIO64_PU OFFSET: 0944h RESET = 0000_0000h			PIO64 Pull-Up Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_PU[63:32]	R/W	PIO64_PU[x] 0 = Pull-up disabled 1 = Pull-up enabled

Note: 0944h-[7:0], 0945h-[15:8], 0946h-[23:16], 0947h-[31:24]

TABLE 19: PIO[95:64] PULL-UP RESISTOR REGISTER

PIO96_PU OFFSET: 0948h RESET = 0000_0000h			PIO96 Pull-Up Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_PU[95:64]	R/W	PIO96_PU[x] 0 = Pull-up disabled 1 = Pull-up enabled

Note: 0948h-[7:0], 0949h-[15:8], 094Ah-[23:16], 094Bh-[31:24]

TABLE 20: PIO[31:0] PULL-DOWN RESISTOR REGISTER

PIO32_PD OFFSET: 0950h RESET = 0000_0000h			PIO32 Pull-Down Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_PD[31:0]	R/W	PIO32_PD[x] 0 = Pull-down disabled 1 = Pull-down enabled

Note: 0950h-[7:0], 0951h-[15:8], 0952h-[23:16], 0953h-[31:24]

TABLE 21: PIO[63:32] PULL-DOWN RESISTOR REGISTER

PIO64_PD OFFSET: 0954h RESET = 0000_0000h			PIO64 Pull-Down Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_PD[63:32]	R/W	PIO64_PD[x] 0 = Pull-down disabled 1 = Pull-down enabled

Note: 0954h-[7:0], 0955h-[15:8], 0956h-[23:16], 0957h-[31:24]

TABLE 22: PIO[95:64] PULL-DOWN RESISTOR REGISTER

PIO96_PD OFFSET: 0958h RESET = 0000_0000h			PIO96 Pull-Down Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_PD[95:64]	R/W	PIO96_PD[x] 0 = Pull-down disabled 1 = Pull-down enabled

Note: 0958h-[7:0], 0959h-[15:8], 095Ah-[23:16], 095Bh-[31:24]

TABLE 23: PIO[31:0] OPEN DRAIN MODE REGISTER

PIO32_OD OFFSET: 0960h RESET = 0000_0000h			PIO32 Open Drain Mode Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_OD[31:0]	R/W	PIO32_OD[x] 0 = Open drain disabled 1 = Open drain enabled If bit is 1 and the corresponding output is enabled { If output register is 1, output is Hi-Z unless pull-up is enabled If output register is 0, output is 0}

Note: 0960h-[7:0], 0961h-[15:8], 0962h-[23:16], 0963h-[31:24]

TABLE 24: PIO[63:32] OPEN DRAIN MODE REGISTER

PIO64_OD OFFSET: 0964h RESET = 0000_0000h			PIO64 Open Drain Mode Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_OD[63:32]	R/W	PIO64_OD[x] 0 = Open drain disabled 1 = Open drain enabled If bit is 1 and the corresponding output is enabled { If output register is 1, output is Hi-Z unless pull-up is enabled If output register is 0, output is 0}

Note: 0964h-[7:0], 0965h-[15:8], 0966h-[23:16], 0967h-[31:24]

TABLE 25: PIO[95:64] OPEN DRAIN MODE REGISTER

PIO96_OD OFFSET: 0968h RESET = 0000_0000h			PIO96 Open Drain Mode Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_OD[95:64]	R/W	PIO96_OD[x] 0 = Open drain disabled 1 = Open drain enabled If bit is 1 and the corresponding output is enabled { If output register is 1, output is Hi-Z unless pull-up is enabled If output register is 0, output is 0}

Note: 0968h-[7:0], 0969h-[15:8], 096Ah-[23:16], 096Bh-[31:24]

TABLE 26: PIO[31:0] DEBOUNCE REGISTER

PIO32_DEB OFFSET: 09E0h RESET = 0000_0000h			PIO32 Debounce Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO32_DEB[31:0]	R/W	PIO32_DEB[x] 0 = No debounce 1 = Input debounced as specified in GPIO_DEBOUNCE

Note: 09E0h-[7:0], 09E1h-[15:8], 09E2h-[23:16], 09E3h-[31:24]

TABLE 27: PIO[63:32] DEBOUNCE REGISTER

PIO64_DEB OFFSET: 09E4h RESET = 0000_0000h			PIO64 Debounce Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO64_DEB[63:32]	R/W	PIO64_DEB[x] 0 = No debounce 1 = Input debounced as specified in GPIO_DEBOUNCE

Note: 09E4h-[7:0], 09E5h-[15:8], 09E6h-[23:16], 09E7h-[31:24]

TABLE 28: PIO[95:64] DEBOUNCE REGISTER

PIO96_DEB OFFSET: 09E8h RESET = 0000_0000h			PIO96 Debounce Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:0	PIO96_DEB[95:64]	R/W	PIO96_DEB[x] 0 = No debounce 1 = Input debounced as specified in GPIO_DEBOUNCE

Note: 09E8h-[7:0], 09E9h-[15:8], 09EAh-[23:16], 09EBh-[31:24]

TABLE 29: GPIO[31:0] DEBOUNCE REGISTER

GPIO_DEBOUNCE OFFSET: 09F0h RESET = 01h			GPIO Debounce Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
31:8	Reserved	R	Reserved
7:0	DEBOUNCE	R/W	Debounce count in 10-millisecond increments

Note: 09F0h-[7:0], 09F1h-[15:8], 09F2h-[23:16], 09F3h-[31:24]

TABLE 30: VENDOR ID LSB

VID_LSB OFFSET: 3000h RESET = 24h			Vendor ID LSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	VID_LSB	R/W	Least Significant Byte of the Hub Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementers Forum).

TABLE 31: VENDOR ID MSB

VID_MSB OFFSET: 3001h RESET = 04h			Vendor ID MSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	VID_MSB	R/W	Most Significant Byte of the Hub Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementors Forum).

TABLE 32: PRODUCT ID LSB

PID_LSB OFFSET: 3002h RESET = XXh			Product ID LSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PID_LSB	R/W	Least Significant Byte of the Hub Product ID. This is a 16-bit value that the vendor can assign and uniquely identifies this product. The default value is dependent on the part as shown below: USB4712 = 12h USB4715 = 15h USB4912 = 12h USB4914 = 14h USB4916 = 16h USB4925 = 25h USB4927 = 27h Note that if port disable straps are implemented, these values automatically decrement by the N of ports disabled by strapping. For example, if a design that implements USB4925 with two ports disabled by strapping, the PID automatically changes to 0x4923.

TABLE 33: PRODUCT ID MSB

PID_MSB OFFSET: 3003h RESET = 4Xh			Product ID MSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PID_MSB	R/W	Most Significant Byte of the Hub Product ID. This is a 16-bit value that uniquely identifies this product and can be assigned by the vendor. The default value is dependent on the part as shown below: USB49xx = 49h USB47xx = 47h

TABLE 34: DEVICE ID LSB

DID_LSB OFFSET: 3004h RESET = 21h			Device ID LSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	DID_LSB	R/W	Least Significant Byte of the Hub Device ID. This is a 16-bit device release number in BCD format assigned by OEM.

TABLE 35: DEVICE ID MSB

DID_MSB OFFSET: 3005h RESET = 01h			Device ID MSB Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	DID_MSB	R/W	Most Significant Byte of the Hub Device ID. This is a 16-bit device release number in BCD format assigned by OEM.

TABLE 36: HUB CONFIGURATION DATA BYTE 1

HUB_CFG1 OFFSET: 3006h RESET = 00h(3006h)			Hub Configuration Data Byte 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	SELF_BUS_PWR	R/W	Self or Bus Power: Selects between Self-Powered and Bus-Powered operations. The hub is either Self-Powered (draws less than 2 mA of upstream bus power) or Bus-Powered (limited to 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a Bus-Powered device, the Microchip Hub consumes less than 100 mA of current prior to being configured. After configuration, the Bus-Powered Microchip Hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB2.0 specifications are not violated. When configured as a Self-Powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. 0 = Bus-powered operation 1 = Self-powered operation
6	VSM_DISABLE	R/W	0 = VSM Messaging is supported. 1 = VSM Messaging is disabled. When VSM is disabled, all vendor-specific messaging to the hub endpoint is ignored with no ill effect.
5	HS_DISABLE	R/W	High Speed Disable: Disables the capability to attach as either a High-speed or Full-speed device, and forces attachment as Full-speed only (that is, no High-speed support). 0 = High-speed/Full-speed 1 = Full-speed-only (High-speed disabled!)
4	MTT_ENABLE	R/W	Multi-TT enable: Enables one transaction translator per port operation. Selects between modes where only one transaction translator is available for all ports (Single-TT), or each port gets a dedicated transaction translator (Multi-TT). The host may force Single-TT mode only. 0 = Single TT for all ports 1 = One TT per port (multiple TT's supported)
3	EOP_DISABLE	R/W	EOP Disable: Disables EOP generation of EOF1 when in Full-speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See *Section 11.3.1* of the *USB 2.0 Specification* for additional details. Note: Generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend. 0 = An EOP is generated at the EOF1 point if no traffic is detected. 1 = EOP generation at EOF1 is disabled This is a normal USB operation.

TABLE 36: HUB CONFIGURATION DATA BYTE 1 (CONTINUED)

HUB_CFG1 OFFSET: 3006h RESET = 00h(3006h)			Hub Configuration Data Byte 1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
2:1	CURRENT_SNS	R/W	Overcurrent Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a port or ganged basis is hardware-implementation dependent. 00 = Ganged sensing (all ports together). The OCS source select registers need to be updated to select the OCS ganged input. 01 = Individual port-by-port 1x = Over current sensing not supported (must only be used with Bus-Powered configurations)
0	PORT_PWR	R/W	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is hardware implementation dependent. 0 = Ganged switching (all ports together) 1 = Individual port-by-port switching

TABLE 37: HUB CONFIGURATION DATA BYTE 2

HUB_CFG2 OFFSET: 3007h RESET = 00h			Hub Configuration Data Byte 2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R/W	Reserved
5:4	OC_TIMER	R/W	Overcurrent Timer: Overcurrent Timer delay. This measures the minimum pulse width for which a pulse is considered valid. 00 = 50 ns 01 = 100 ns 10 = 200 ns 11 = 400 ns
3	COMPOUND	R/W	Compound Device: Allows the OEM to indicate that the hub is part of a compound (see the *USB Specification* for definition) device. The applicable ports must also be defined as having a “Non-Removable Device.” When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 = No. 1 = Yes, the hub is part of a compound device.
2:0	Reserved	R/W	Always read ‘0’

TABLE 38: HUB CONFIGURATION DATA BYTE 3

HUB_CFG3 OFFSET: 3008h RESET = 00h			Hub Configuration Data Byte 3 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Reserved
3	PRTMAP_EN	R/W	Port Re-Mapping enable: Selects the method used by the hub to assign port numbers and disable ports. ‘0’ = Standard mode. Strap options or the following registers are used to define which ports are enabled, and the port mapped as port ‘n’ on the hub is reported as port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped to report contiguous port numbers to the host. ‘1’ = Port Re-Map mode. The mode enables remapping via the registers defined below. Disable the LPM to use this feature in USB 2 Hub Control.
2:1	Reserved	R/W	Always read ‘0’
0	STRING_EN	R/W	Enables String Descriptor Support ‘0’ = String Support Disabled ‘1’ = String Support Enabled

TABLE 39: HUB NON-REMOVABLE DEVICE

HUB_NRD OFFSET: 3009h RESET = 00h			Hub Non-Removable Device Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HUB_NON_REM	R/W	Non-Removable Device: Indicates which ports include non-removable devices. ‘0’ = Port is removable. ‘1’ = Port is non-removable. Informs the host if one of the active ports has a permanent device that is non-detachable from the hub. The device must provide its own descriptor data. Bit 7 = Reserved Bit 6 = Reserved Bit 5 = 1; Port 5 non-removable Bit 4 = 1; Port 4 non-removable Bit 3 = 1; Port 3 non-removable Bit 2 = 1; Port 2 non-removable Bit 1 = 1; Port 1 non removable Bit 0 = Reserved, always = ‘0’ When using the CFG_NON_REM strap, the port configuration is selected by the resistor used as follows: 200K PD – All removable 200K PU – Port 1 non-removable 10K PD – Port 1, 2 non-removable 10K PU – Port 1, 2, 3 non-removable (USB4916/USB4927/USB47xx) 10R PD – Port 1, 2, 3, 4 non-removable (USB4916/USB4927/USB47xx) 10R PU – Not used No resistor – Not allowed

TABLE 40: PORT DISABLE – SELF POWERED

PORT_DIS_S OFFSET: 300Ah RESET = 00h			Port Disable for Self-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_SELF	R/W	Port Disable Self-Powered: Disables 1 or more ports. ‘0’ = Port is available. ‘1’ = Port is disabled. During Self-Powered operation, when PRTMAP_EN = 0, this selects the ports that are permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order; the internal logic automatically reports the correct number of enabled ports to the USB host, and reorders the active ports to ensure proper function. When using the internal default option, the PRT_DIS[1:0] pins disable the appropriate ports. Bit 7 = 1; Port 7 is disabled. Bit 6 = 1; Port 6 is disabled. Bit 5 = 1; Port 5 is disabled. Bit 4 = 1; Port 4 is disabled. Bit 3 = 1; Port 3 is disabled. Bit 2 = 1; Port 2 is disabled. Bit 1 = 1; Port 1 is disabled. Bit 0 = Reserved, always = ‘0’

TABLE 41: PORT DISABLE – BUS POWERED

PORT_DIS_B OFFSET: 300Bh RESET = 00h			Port Disable for Bus Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PORT_DIS_BUS	R/W	Port Disable Bus-Powered: Disables 1 or more ports. ‘0’ = Port is available. ‘1’ = Port is disabled. During Bus-Powered operation, when PRTMAP_EN = 0, this selects the ports that are permanently disabled, and are not available to be enabled or enumerated by a host controller. The ports can be disabled in any order. The internal logic automatically reports the correct number of enabled ports to the USB host and reorders the active ports to ensure proper functioning. When using the internal default option, the PRT_DIS[1:0] pins disable the appropriate ports. Bit 7 = 1; Port 7 is disabled. Bit 6 = 1; Port 6 is disabled. Bit 5 = 1; Port 5 is disabled. Bit 4 = 1; Port 4 is disabled. Bit 3 = 1; Port 3 is disabled. Bit 2 = 1; Port 2 is disabled. Bit 1 = 1; Port 1 is disabled. Bit 0 = Reserved, always = ‘0’

TABLE 42: HUB MAX POWER – SELF POWERED

H_MAXP_S OFFSET: 300Ch RESET = 00h			Maximum Current for Self-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MAX_PWR_SP	R/W	Maximum Power Self-Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. The *USB2.0 Specification* does not permit this value to exceed 100 mA.

TABLE 43: HUB MAXIMUM POWER – BUS POWERED

H_MAXP_B OFFSET: 300Dh RESET = 00h			Maximum Current for Bus-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MAX_PWR_BP	R/W	Maximum Power Bus Powered: Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors.

TABLE 44: HUB CONTROLLER MAXIMUM CURRENT – SELF POWERED

HC_MAXP_S OFFSET: 300Eh RESET = 00h			Hub Controller Maximum Current for Self-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HC_MAX_C_SP	R/W	Hub Controller Max Current Self-Powered: Value in 1 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. The *USB2.0 Specification* does not permit this value to exceed 100 mA.

TABLE 45: HUB CONTROLLER MAXIMUM CURRENT – BUS POWERED

HC_MAXP_B OFFSET: 300Fh RESET = 00hh			Hub Controller Maximum Current for Bus-Powered Operation Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HC_MAX_C_BP	R/W	Hub Controller Maximum Current Bus-Powered: Value in 1 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device.

TABLE 46: POWER-ON TIME REGISTER

PWR_ON_TIME OFFSET: 3010h RESET = FFh			Power-On Time Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	POWER_ON_TIME	R/W	Power On Time: The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is good on that port. The system software uses this value to determine how long to wait before accessing a powered-on port.

TABLE 47: MANUFACTURER STRING INDEX REGISTER

MFR_STR_INDEX OFFSET: 3013h RESET = 01h			Manufacturer String Index Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MFR_STR_INDEX	R/W	Manufacturer String Index

TABLE 48: PRODUCT STRING INDEX REGISTER

PRD_STR_INDEX OFFSET: 3014h RESET = 02h			Product String Index Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRD_STR_INDEX	R/W	Product String Index

TABLE 49: SERIAL STRING INDEX REGISTER

SER_STR_INDEX OFFSET: 3015h RESET = 00h			Serial String Index Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	SER_STR_INDEX	R/W	Serial String Index

TABLE 50: BATTERY CHARGING ENABLE STATUS REGISTER

BC_EN OFFSET: 30D0h RESET = 00h			Battery Charging Enable Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always 0
4:1	BC_EN_STAT	R	Bit 4 = 1; Port 4 Battery Charging Enabled Bit 3 = 1; Port 3 Battery Charging Enabled Bit 2 = 1; Port 2 Battery Charging Enabled Bit 1 = 1; Port 1 Battery Charging Enabled
0	Reserved	R	Always 0

TABLE 51: START OCS LOCKOUT TIMER REGISTER

OCS_LOCKOUT OFFSET: 30E1h RESET = 0Ah			Start OCS Lockout Timer Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	Start_OCS_Lock	R/W	This timer blocks OCS events after the port power is enabled and is specified in 1-millisecond increments.

TABLE 52: PORT POWER STATUS

PORT_PWR_STAT OFFSET: 30E5h RESET = 00h			Port Power Status Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Always 0
4:1	BPRTPWR[4:1]	R	Bit 4 = 1; State of Port Power Enable 4 Bit 3 = 1; State of Port Power Enable 3 Bit 2 = 1; State of Port Power Enable 2 Bit 1 = 1; State of Port Power Enable 1
0	Reserved	R	Always 0

TABLE 53: OCS MINIMUM WIDTH REGISTER

OCS_MIN_WIDTH OFFSET: 30EAh RESET = 05h			OCS Minimum Width Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	OCS _MIN_WIDTH	R/W	OCS_MIN_WIDTH contains the minimum OCS pulse width required to detect an OCS event. This field provides a range from 0 millisecond to 5 milliseconds in 1-millisecond increments.

TABLE 54: OCS INACTIVE TIMER

OCS_INACTIVE_TIMER OFFSET: 30EBh RESET = 14h			OCS Inactive Timer After First OCS Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	OCS _INACTIVE	R/W	OCS_INACTIVE contains the maximum delay between two consecutive OCS pulses to occur to register as an OCS event. This field provides a range from 0 millisecond to 255 milliseconds in 1-millisecond increments.

TABLE 55: HUB PORT SWAP REGISTER

HUB_PRT_SWAP OFFSET: 30FAh RESET = 00h			Hub Port Swap Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRT_SWAP	R/W	Port Swap: Swaps the Upstream and Downstream USB DP and DM Pins for ease of board routing to devices and connectors. ‘0’ = USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. ‘1’ = USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin Bit 5 = ‘1’: Port 5 DP/DM is swapped. Bit 4 = ‘1’: Port 4 DP/DM is swapped. Bit 3 = ‘1’: Port 3 DP/DM is swapped. Bit 2 = ‘1’: Port 2 DP/DM is swapped. Bit 1 = ‘1’: Port 1 DP/DM is swapped. Bit 0 = ‘1’: Upstream Port DP/DM is swapped.

TABLE 56: HUB PORT REMAP 12 REGISTER

HUB_PRT_REMAP_12 OFFSET: 30FBh RESET = 00h			Hub Port 1-2 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT_2_MAP	R/W	0000b – Physical Port 2 is disabled. 0001b – Physical Port 2 is mapped to Logical Port 1. 0010b – Physical Port 2 is mapped to Logical Port 2. 0011b – Physical Port 2 is mapped to Logical Port 3. 0100b – Physical Port 2 is mapped to Logical Port 4. 0101b – Physical Port 2 is mapped to Logical Port 5. 0110b – Physical Port 2 is mapped to Logical Port 6. 0111b – Physical Port 2 is mapped to Logical Port 7. All other values default to 0000b value.
3:0	PRT_1_MAP	R/W	0000b – Physical Port 1 is disabled. 0001b – Physical Port 1 is mapped to Logical Port 1. 0010b – Physical Port 1 is mapped to Logical Port 2. 0011b – Physical Port 1 is mapped to Logical Port 3. 0100b – Physical Port 1 is mapped to Logical Port 4. 0101b – Physical Port 1 is mapped to Logical Port 5. 0110b – Physical Port 1 is mapped to Logical Port 6. 0111b – Physical Port 1 is mapped to Logical Port 7. All other values default to 0000b value.

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 57: HUB PORT REMAP 34 REGISTER

HUB_PRT_REMAP_34 OFFSET: 30FCh RESET = 00h			Hub Port 3-4 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT-4_MAP	R/W	0000b – Physical Port 4 is disabled. 0001b – Physical Port 4 is mapped to Logical Port 1. 0010b – Physical Port 4 is mapped to Logical Port 2. 0011b – Physical Port 4 is mapped to Logical Port 3. 0100b – Physical Port 4 is mapped to Logical Port 4. 0101b – Physical Port 4 is mapped to Logical Port 5. 0110b – Physical Port 4 is mapped to Logical Port 6. 0111b – Physical Port 4 is mapped to Logical Port 7. All other values default to 0000b value.
3:0	PRT-3_MAP	R/W	0000b – Physical Port 3 is disabled. 0001b – Physical Port 3 is mapped to Logical Port 1. 0010b – Physical Port 3 is mapped to Logical Port 2. 0011b – Physical Port 3 is mapped to Logical Port 3. 0100b – Physical Port 3 is mapped to Logical Port 4. 0101b – Physical Port 3 is mapped to Logical Port 5. 0110b – Physical Port 3 is mapped to Logical Port 6. 0111b – Physical Port 3 is mapped to Logical Port 7. All other values default to 0000b value.

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 58: HUB PORT REMAP 56 REGISTER

HUB_PRT_REMAP_56 OFFSET: 30FDh RESET = 00h			Hub Port 5-6 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	PRT-6_MAP	R/W	0000b – Physical Port 6 is disabled. 0001b – Physical Port 6 is mapped to Logical Port 1. 0010b – Physical Port 6 is mapped to Logical Port 2. 0011b – Physical Port 6 is mapped to Logical Port 3. 0100b – Physical Port 6 is mapped to Logical Port 4. 0101b – Physical Port 6 is mapped to Logical Port 5. 0110b – Physical Port 6 is mapped to Logical Port 6. 0111b – Physical Port 6 is mapped to Logical Port 7. All other values default to 0000b value.
3:0	PRT-5_MAP	R/W	0000b – Physical Port 5 is disabled. 0001b – Physical Port 5 is mapped to Logical Port 1. 0010b – Physical Port 5 is mapped to Logical Port 2. 0011b – Physical Port 5 is mapped to Logical Port 3. 0100b – Physical Port 5 is mapped to Logical Port 4. 0101b – Physical Port 5 is mapped to Logical Port 5. 0110b – Physical Port 5 is mapped to Logical Port 6. 0111b – Physical Port 5 is mapped to Logical Port 7. All other values default to 0000b value.

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 59: HUB PORT REMAP 7 REGISTER

HUB_PRT_REMAP_7 OFFSET: 30FEh RESET = 00h			Hub Port 7 Remap Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always read 0
3:0	PRT-7_MAP	R/W	0000b – Physical Port 7 is disabled 0001b – Physical Port 7 is mapped to Logical Port 1. 0010b – Physical Port 7 is mapped to Logical Port 2. 0011b – Physical Port 7 is mapped to Logical Port 3. 0100b – Physical Port 7 is mapped to Logical Port 4. 0101b – Physical Port 7 is mapped to Logical Port 5. 0110b – Physical Port 7 is mapped to Logical Port 6. 0111b – Physical Port 7 is mapped to Logical Port 7. All other values default to 0000b value.

Note: Writes to this register are disabled unless PRTMAP_EN bit in HUB_CFG_3 is set.

TABLE 60: USB 2 LINK STATE 1

USB2_LINK_STATE1 OFFSET: 3100h RESET = FFh			USB2 Link State1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	L_STATE3	R	Indicates the state of Downstream Port 3 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off
5:4	L_STATE2	R	Indicates the state of Downstream Port 2 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off
3:2	L_STATE1	R	Indicates the state of Downstream Port 1 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off
1:0	L_STATE0	R	Indicates the state of Upstream Port 0 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off

TABLE 61: USB 2 LINK STATE 2

USB2_LINK_STATE2 OFFSET: 3101h RESET = FFh			USB2 Link State2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	L_STATE7	R	Indicates the state of Downstream Port 7 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off
5:4	L_STATE6	R	Indicates the state of Downstream Port 6 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off
3:2	L_STATE5	R	Indicates the state of Downstream Port 5 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off
1:0	L_STATE4	R	Indicates the state of Downstream Port 4 00b – L0 Normal Operation 01b – L1 Sleep 10b – L2 Suspend 11b – L3 Off

TABLE 62: USB 2 HUB CONTROL

USB2_HUB_CTL OFFSET: 3104h RESET = 00h			USB2 Hub Control Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:2	RESERVED	R	Reserved
1	LPM_DISABLE	R/W	Disables Link Power Management
0	RESET	R/W	Hub reset downstream 0: Hub is in Normal mode. 1: Hub is kept in reset.

TABLE 63: USB 2 VERSION BCD[15:0]

USB2_BCDUSB OFFSET: 3108h RESET = 0201h			USB2 Version BCD Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
15:0	USBVCD[15:0]	R/W	USB Specification Release Number in BCD format

Note: 3108h-[15:8], 3109h-[7:0]

TABLE 64: PRIMARY HUB CONTROL PORTABLE TEST

CNTLP OFFSET: 318Ch RESET = 00h			Primary Hub Control Portable Test Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	RESERVED	R	Reserved
3:1	EMBEDTEST	R/W	Embedded Host Compliance Testing Modes. Enables test modes on USB ports. To facilitate embedded host compliance testing, the SOC may select any of the following test modes using the serial port interface instead of modifying the embedded host stack to accomplish the same modes using USB communication to the hub controller with standard SETUP packet commands. Both methods can be used for embedded host compliance testing with equivalent results. The test modes described below are related to *Section 7.1.20* of the *USB 2.0 Specification* and associated errata. Encoded values match the low nibble of the PID asserted by the HS-OPT when it requests the host to enter the associated test mode. When the test mode is entered, it continues until the embedTest control is written back to '000' by the SOC. 0 (000) – Default Operation – no test mode asserted 1 (001) – TEST_SE0_NAK – hub enters high-speed receive and drives SE0 on the hub's downstream port 2 (010) – TEST_J – hub's downstream port enters high-speed J state 3 (011) – TEST_K – hub's downstream port enters high-speed K state 4 (100) – TEST_PACKET – send test packets on downstream port All others are reserved. The port in use is selected using the EMBED_TEST_PORT_SEL register.
0	Reserved	R	Reserved

TABLE 65: EMBEDDED PRIMARY HUB TEST PORT SELECT

EMBED_TEST_PORT_SEL OFFSET: 318Dh RESET = 00h			Primary Hub Test Port Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:5	Reserved	R	Reserved
4:0	PORT_SEL[4:0]	R/W	Enables a port at the particular bit position. Any combination is permissible. Some examples are shown below: 00000 – Normal operation 00001 – Downstream Port 1 00010 – Downstream Port 2 00100 – Downstream Port 3 01000 – Downstream Port 4 10000 – Downstream Port 5 00011 – Downstream Port 1 and Port 2 00111 – Downstream Port 1, Port 2, and Port 3 01111 – Downstream Port 1, Port 2, Port 3, and Port 4 11111 – Downstream port 1, Port 2, Port 3, Port 4, and Port 5 To enable testing of the upstream port, use FlexConnect to swap port 1 with the upstream port, and then run the EMBEDTEST on port 1 (see Section 6.0, "FlexConnect Command").

TABLE 66: USB 2 HUB STATUS REGISTER

USB2_HUB_STAT OFFSET: 3194h RESET= 00h			USB2 Hub Status Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	Reserved	R	Always read ‘0’
5:1	USB2_DN_CONNECTED	R	USB Device connected on downstream port Bit 5 = ‘1’: Port 5 device connected Bit 4 = ‘1’: Port 4 device connected Bit 3 = ‘1’: Port 3 device connected Bit 2 = ‘1’: Port 2 device connected Bit 1 = ‘1’: Port 1 device connected
0	USB2_HOST_DETECT	R	Bit 0= ‘1’: USB2 Host connected

TABLE 67: USB 2 DOWNSTREAM DEVICE SPEED [4-1]

USB2_DN_SPEED14 OFFSET: 3195h RESET = 00h			USB2 Downstream Device Speed1 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	P4_SPEED	R	Indicates the state of Downstream Port 4 00b: No connect 01b: LS 10b: FS 11b: HS
5:4	P3_SPEED	R	Indicates the state of Downstream Port 3 00b: No connect 01b: LS 10b: FS 11b: HS
3:2	P2_SPEED	R	Indicates the state of Downstream Port 2 00b: No connect 01b: LS 10b: FS 11b: HS
1:0	P1_SPEED	R	Indicates the state of Downstream Port 1 00b: No connect 01b: LS 10b: FS 11b: HS

TABLE 68: USB 2 DOWNSTREAM DEVICE SPEED [5]

USB2_DN_SPEED5 OFFSET: 3196h RESET = 00h			USB2 Downstream Device Speed2 Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:2	Reserved	R	Always reads 0
1:0	P5_SPEED	R	Indicates the state of Downstream Port 5 00b: No connect 01b: LS 10b: FS 11b: HS

TABLE 69: USB 2 SUSPEND INDICATOR

USB2_SUSP_IND OFFSET: 3197h RESET = 00h			USB2 Suspend Indicator Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:1	Reserved	R	Always read ‘0’
0	USB_SUSPEND	R/W	Suspend Indicator 0 = Active; the hub is configured and operational. 1 = Inactive; the hub is not configured or configured and is suspended in a Sleep state.

TABLE 70: SECONDARY HUB CONTROL PORTABLE TEST (USB4925/USB4927)

SCNTLP OFFSET: 398Ch RESET = 00h			Secondary Hub Portable Test (USB4925/USB4927) Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Reserved
3:1	EMBEDTEST	R/W	Embedded Host Compliance Testing Modes. Enables test modes on ports. To facilitate embedded host compliance testing, the SOC may select any of the following test modes using the serial port interface instead of modifying the embedded host stack to accomplish the same modes using USB communication to the hub controller with standard SETUP packet commands. Both methods can be used for embedded host compliance testing with equivalent results. The test modes described below are related to *Section 7.1.20* of the *USB 2.0 Specification* and associated errata. Encoded values match the low nibble of the PID asserted by the HS-OPT when it requests the host to enter the associated test mode. When the test mode is entered, it continues until the embedTest control is written back to '000' by the SOC. 0 (000) – Default Operation – no test mode asserted 1 (001) – TEST_SE0_NAK – hub enters high-speed receive and drives SE0 on the hub's downstream port 2 (010) – TEST_J – hub's downstream port enters high-speed J state 3 (011) – TEST_K – hub's downstream port enters high-speed K state 4 (100) – TEST_PACKET – send test packets on downstream port All others are reserved. The port in use is selected using the EMBED_SEC_TEST_PORT_SEL register.
0	Reserved	0	Reserved

Note: Before the SCNTLP register is used, a SET_ROLE_SWITCH command packet must be sent to Endpoint 0 of the Hub Function Controller to enable the secondary hub. See Section 7.0, "Dual Upstream (DUST) Command (USB4925/USB4927)".

TABLE 71: EMBEDDED SECONDARY HUB TEST PORT SELECT

EMBED_SEC_TEST_PORT_SEL OFFSET: 398Dh RESET = 00h			Secondary Hub Test Port Select (USB4925/USB4927) Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:1	RESERVED	R	Reserved
0	PORT_SEL	R/W	Enables port 1 0 – Normal operation 1 – Downstream Port 1

TABLE 72: PORT 1 PORT POWER SELECT

PORT_CFG_SEL_1 OFFSET: 3C00h RESET = 80h			Port 1 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = Port power and overcurrent sense use separate pins (Test mode). 1 = Port power and overcurrent sense use the same pin (Normal mode).
6	GANG_PIN	R/W	Port is connected to GANG_PWR_pin.
5:4	RESERVED	R/W	Always reads 0
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL1. 0000b = Port power is disabled. 0001b = Port is on if USB2 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 73: PORT 2 PORT POWER SELECT

PORT_CFG_SEL_2 OFFSET: 3C04h RESET = 80h			Port 2 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = Port power and overcurrent sense use separate pins (Test mode). 1 = Port power and overcurrent sense use the same pin (Normal mode).
6	GANG_PIN	R/W	Port is connected to GANG_PWR_pin.
5:4	RESERVED	R/W	Always reads 0
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL2. 0000b = Port power is disabled. 0001b = Port is on if USB2 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 74: PORT 3 PORT POWER SELECT

PORT_CFG_SEL_3 OFFSET: 3C08h RESET = 80h			Port 3 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = Port power and overcurrent sense use separate pins (Test mode). 1 = Port power and overcurrent sense use the same pin (Normal mode).
6	GANG_PIN	R/W	Port is connected to GANG_PWR_pin.
5:4	RESERVED	R/W	Always reads 0
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL3. 0000b = Port power is disabled. 0001b = Port is on if USB2 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 75: PORT 4 PORT POWER SELECT

PORT_CFG_SEL_4 OFFSET: 3C0Ch RESET = 80h			Port 4 Power Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = Port power and overcurrent sense use separate pins (Test mode). 1 = Port power and overcurrent sense use the same pin (Normal mode).
6	GANG_PIN	R/W	Port is connected to GANG_PWR_pin.
5:4	RESERVED	R/W	Always reads 0
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL4. 0000b = Port power is disabled. 0001b = Port is on if USB2 port power is on. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 76: PORT POWER SELECT GANG

PORT_CFG_SEL_GANG OFFSET: 3C1Ch RESET = 80h			Port Power Select Gang Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7	COMBINED_MODE	R/W	0 = Port power and overcurrent sense use separate pins (Test mode). 1 = Port power and overcurrent sense use the same pin (Normal mode).
6	GANG_PIN	R/W	0 = GANG_PWR is not connected. 1 = GANG_PWR is connected to the port.
5:4	Reserved	R	Always reads 0
3:0	PRT_SEL	R/W	This selects the source for PRT_CTL_GANG. 0000b = Port power is disabled. 0001b = Port is on if GANG_PIN is 1. 0100b = Port is on if designated GPIO is on. All other values are reserved.

TABLE 77: USB PORT 1 OCS SOURCE SELECT

USB_OCS_SEL_1 OFFSET: 3C20h RESET = 00h			Port 1 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R	Always reads 0
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 1. 0000b = OCS is disabled. 0001b = OCS comes from OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 78: USB PORT 2 OCS SOURCE SELECT

USB_OCS_SEL_2 OFFSET: 3C24h RESET = 00h			Port 2 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read 0
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 2. 0000b = OCS is disabled. 0001b = OCS comes from OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 79: USB PORT 3 OCS SOURCE SELECT

USB_OCS_SEL_3 OFFSET: 3C28h RESET = 00h			Port 3 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read 0
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 3. 0000b = OCS is disabled. 0001b = OCS comes from OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 80: USB PORT 4 OCS SOURCE SELECT

USB_OCS_SEL_4 OFFSET: 3C2Ch RESET = 00h			Port 4 OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always read 0
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for Port 4. 0000b = OCS is disabled. 0001b = OCS comes from OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

TABLE 81: GANG OCS SOURCE SELECT

GANG_OCS_SEL OFFSET: 3C3Ch RESET = 00h			Gang OCS Source Select Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Always reads 0
3:0	OCS_SEL	R/W	This selects the source for the OCS signal for PORT_CTL_GANG. 0000b = OCS is disabled. 0001b = OCS comes from OCS pin. 0010b = OCS pin comes from GPIO. 0011b = OCS pin comes from GANG_PWR pin. 1111b = OCS is forced on (for testing). All other values are reserved.

3.3.1.1 Port Control Registers

These registers control the analog signaling of specific ports.

TABLE 82: USB PORT 0 BOOST REGISTER

HS_P0_BOOST OFFSET: 60CAh RESET = 00h			USB Port 0 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the HS_P0_VSENSE register if High-speed disconnect issues are encountered.

TABLE 83: USB PORT 0 VARISENSE REGISTER

HS_P0_VSENSE OFFSET: 60CCh RESET = 00h			USB Port 0 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
5:3	Reserved	R	Reserved

TABLE 83: USB PORT 0 VARISENSE REGISTER (CONTINUED)

HS_P0_VSENSE OFFSET: 60CCh RESET = 00h			USB Port 0 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100 mV trip point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

TABLE 84: USB PORT 1 BOOST REGISTER

HS_P1_BOOST OFFSET: 64CAh RESET = 00h			USB Port 1 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the HS_P1_VSENSE register if High-speed disconnect issues are encountered.

TABLE 85: USB PORT 1 VARISENSE REGISTER

HS_P1_VSENSE OFFSET: 64CCh RESET = 00h			USB Port 1 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
5:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100 mV trip point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

TABLE 86: USB PORT 2 BOOST REGISTER

HS_P2_BOOST OFFSET: 68CAh RESET = 00h			USB Port 2 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the HS_P2_VSENSE register if High-speed disconnect issues are encountered.

TABLE 87: USB PORT 2 VARISENSE REGISTER

HS_P2_VSENSE OFFSET: 68CCh RESET = 00h			USB Port 2 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
5:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100 mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

TABLE 88: USB PORT 3 BOOST REGISTER

HS_P3_BOOST OFFSET: 6CCAh RESET = 00h			USB Port 3 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current. 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the HS_P3_VSENSE register if High-speed disconnect issues are encountered.

TABLE 89: USB PORT 3 VARISENSE REGISTER

HS_P3_VSENSE OFFSET: 6CCCh RESET = 00h			USB Port 3 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
5:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100 mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note: The USB Port 3 registers are available in the USB4916, USB4927, and USB47xx.

TABLE 90: USB PORT 4 BOOST REGISTER

HS_P4_BOOST OFFSET: 70CAh RESET = 00h			USB Port 4 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved

TABLE 90: USB PORT 4 BOOST REGISTER (CONTINUED)

HS_P4_BOOST OFFSET: 70CAh RESET = 00h			USB Port 4 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the HS_P4_VSENSE register if High-speed disconnect issues are encountered.

TABLE 91: USB PORT 4 VARISENSE REGISTER

HS_P4_VSENSE OFFSET: 70CCh RESET = 00h			USB Port 4 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
5:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000: Nominal 100 mV Trip Point 001: Decrease by 12.5 mV 010: Decrease by 25 mV 011: Decrease by 37.5 mV 100: Decrease by 50 mV 101: Decrease by 62.5 mV 110: Increase by 25 mV 111: Increase by 12.5 mV

Note: The USB PORT4 registers are available in the USB4916, USB4927, and USB47xx.

TABLE 92: USB PORT 5 BOOST REGISTER

HS_P5_BOOST OFFSET: 74CAh RESET = 00h			USB Port 5 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the HS_P_VSENSE register if High-speed disconnect issues are encountered.

TABLE 93: USB PORT 5 VARISENSE REGISTER

HS_P5_VSENSE OFFSET: 74CCh RESET = 00h			USB Port 5 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DISC_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
5:3	Reserved	R	Reserved
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100 mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note 1: For the USB4914 and USB4925, the USB PORT5 registers above are associated with USB Port 3.

2: The USB Port 5 registers are not available on theUSB47xx.

TABLE 94: SEC PORT 1 BOOST REGISTER

SEC_P1_BOOST OFFSET: 78CAh RESET = 00h			Secondary USB Port 1 Boost Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
2:0	HS_BOOST	R/W	HS Output Current 000b: Nominal 17.78 mA 001b: Decrease by 5% 010b: Increase by 10% 011b: Increase by 5% 100b: Increase by 20% 101b: Increase by 15% 110b: Increase by 30% 111b: Increase by 25% Note: If adjusting this register, it might be necessary to also adjust the USB2_HS_DISC_TUNE[1:0] field of the SEC_P1_VSENSE register if High-speed disconnect issues are encountered.

Note: This register is only used with USB4925/USB4927 hubs.

TABLE 95: SEC PORT 1 VARISENSE REGISTER

SEC_P1_VSENSE OFFSET: 78CCh RESET = 00h			Secondary USB Port 1 Varisense Register Base Address: BF80_0000h
Bit	**Name**	**R/W**	**Description**
7:6	USB2_HS_DIS-C_TUNE[1:0]	R/W	HS Disconnect Threshold Tuning 00b: Nominal (575 mV) threshold 01b: 625 mV threshold (+8.6%) 10b: 675 mV threshold (+17%) 11b: 700 mV threshold (+22%)
2:0	SQ_TUNE[2:0]	R/W	Squelch Tune 000b: Nominal 100 mV Trip Point 001b: Decrease by 12.5 mV 010b: Decrease by 25 mV 011b: Decrease by 37.5 mV 100b: Decrease by 50 mV 101b: Decrease by 62.5 mV 110b: Increase by 25 mV 111b: Increase by 12.5 mV

Note: This register is only used with USB4925/USB4927 hubs.

TABLE 96: HFC PRODUCT ID LSB

HFC_PID_LSB OFFSET: 2856h RESET = 4Xh			HFC Product ID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PID_LSB	R/W	Least Significant Byte of the HFC Product ID. This is a 16-bit value that uniquely identifies this HFC device. The default value depends on the features enabled on the device as shown below: I2S Audio only = 42h I2S Audio/HID = 43h CDC = 44h I2S, CDC = 46h I2S Audio/HID, CDC = 47h WinUSB only = 40h I2S Audio, WinUSB = 4Ah I2S Audio/HID, WinUSB = 4Bh WinUSB, CDC = 4Ch I2S Audio, WinUSB, CDC = 4Eh I2S Audio/HID, WinUSB, CDC = 4Fh

TABLE 97: HFC PRODUCT ID MSB

HFC_PID_MSB OFFSET: 2857h RESET = 4Xh			HFC Product ID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	HFC_PID_MSB	R/W	Most Significant Byte of the HFC Product ID. This is a 16-bit value that uniquely identifies this HFC device. The default value is dependent on the part as shown below: USB47xx = 47h USB49xx= 49h

TABLE 98: LANG_ID [15:0] LANGUAGE IDENTIFIER

LANG_ID OFFSET: 3202h RESET = 0409h			USB-IF Language Identifier Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
15:0	LANG_ID	R/W	USB-IF Language Identifier. Default is English (United States).

Note: 3202h-[7:0], 3203h-[15:8]

TABLE 99: MANUFACTURER STRING DESCRIPTOR

MFG_STR OFFSET: 3204h RESET = 1Eh			Manufacturer String Base Address: BFD2_0000h
BYTE	**Name**	**R/W**	**Description**
0	Length	R/W	Descriptor size which is the Manufacturer String Size + 2. If this field is changed, the Manufacturer String Length register must also be updated with the same value.
1	Descriptor Type	R/W	03h
2	String	R/W	Manufacturer String. This is the actual string in UNICODE UTF-16LE characters. Each character is stored with the LSB at the lower address and the MSB at the next contiguous higher address.

TABLE 100: PRODUCT STRING DESCRIPTOR

PROD_STR OFFSET: 3244h RESET = 10h			Product String Base Address: BFD2_0000h
BYTE	**Name**	**R/W**	**Description**
0	Length	R/W	Descriptor size which is the Product String Size + 2. If this field is changed, the Product String Length register must also be updated with the same value.
1	Descriptor Type	R/W	03h
2	String	R/W	Product String. This is the actual string in UNICODE UTF-16LE characters. Each character is stored with the LSB at the lower address, and the MSB at the next contiguous higher address.

TABLE 101: I2S FEATURE SELECT REGISTER

I2S_FEAT_SEL OFFSET: 3412h RESET = 03h			I2S Feature Unit Select Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:3	Reserved	R	Reserved
7:0	I2S_UNIT_SEL	R/W	Control features of the I2S interface if an I2S configuration is selected. 00h: I2S is disabled. 001h: Audio IN through microphone is enabled. 02h: Audio OUT is enabled. 03h: Both Audio IN are enabled. All other values are reserved.

TABLE 102: I2S HID FEATURE SELECT REGISTER

I2S_HFEAT_SEL OFFSET: 3413h RESET = 00h			I2S HID Feature Select Register Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	I2S_HID_SEL	R/W	Control features of the HID Control of the I2S interface if an I2S configuration is selected. 00h: No I2S HID control 01h: Reserved 02h: HID interface controls speaker mute 03h: HID interface controls speaker mute and microphone mute All other values are reserved.

TABLE 103: SEC HUB PID MSB

SECH_PID_MSB OFFSET: 3417h RESET = 00h			Secondary Hub Default PID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	SECH_PIDM	R/W	USB Secondary Hub Default PID MSB. Reflects the SKU based on the bond and strap options, and could be different from the product PID.

Note: This register is only used with USB4925/USB4927 hubs.

TABLE 104: SEC HUB PID LSB

SECH_PID_LSB OFFSET: 3418h RESET = 00h			Secondary Hub Default PID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	SECH_PIDL	R/W	USB Secondary Hub Default PID LSB. Reflects the SKU based on the bond and strap options, and could be different from the product PID.

Note: This register is only used with USB4925/USB4927 hubs.

TABLE 105: SMBUS OTP RESULT

SMBUS_OTP_RES OFFSET: 3419h RESET = 00h			SMBUS OTP Result Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:1	RESERVED	R	Always reads 0
0	RESULT	R	Result of the last OTP command received through SMBUS 0: Command completed successfully 1: Command failed

TABLE 106: OTP UDC ENUMERATION

OTP_UDC_ENABLE OFFSET: 341Bh RESET = 00h			OTP UDC Enumeration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	MODE	R/W	Control features of the HID Control of the I2S interface if an I2S configuration is selected. 00h: No change from default ROM behavior 01h: Enable UDC enumeration 02h: Disable UDC enumeration All other values are reserved.

TABLE 107: PRIMARY HUB PID MSB

HUB_DEF_PIDM OFFSET: 341Eh RESET = 00h			Primary Hub Default PID MSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRIH_PIDM	R/W	USB Primary Hub Default PID MSB. Reflects the SKU based on the bond and strap options and could be different from the product PID.

TABLE 108: PRIMARY HUB PID LSB

HUB_DEF_PIDL OFFSET: 341Fh RESET = 00h			Primary Hub Default PID LSB Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	PRIH_PIDL	R/W	USB Primary Hub Default PID LSB. Reflects the SKU based on the bond and strap options and could be different from the product PID.

TABLE 109: LED DISABLE

BC_LED_DIS OFFSET: 3433h RESET = 00h			LED Disable Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:4	Reserved	R/W	Reserved
3	BC_LED_DP4	R/W	Disable BC LED for Port 4 0: BC LED for Port 4 enabled 1: BC LED for Port 4 disabled
2	BC_LED_DP3	R/W	Disable BC LED for Port 3 0: BC LED for Port 3 enabled 1: BC LED for Port 3 disabled
1	BC_LED_DP2	R/W	Disable BC LED for Port 2 0: BC LED for Port 2 enabled 1: BC LED for Port 2 disabled
0	BC_LED_DP1	R/W	Disable BC LED for Port 1 0: BC LED for Port 1 enabled 1: BC LED for Port 1 disabled

TABLE 110: PORT 1 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P1 OFFSET: 343Ch RESET = 00h			Port 1 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b: 500 mA 01b: 1000 mA 10b: 1500 mA 11b: 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable, if bit 4 is set this bit is ignored. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 0: DCP disabled 1: DCP enabled
4	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D- while shorting D+/D- together to allow certain Chinese market phones to charge. 0: China mode disabled 1: China mode enabled
3	Reserved	R/W	Reserved
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b: SE1 mode disabled 01b: SE1 1A mode enabled (D-: 2.7V, D+: 2.0V) 10b: SE1 2A mode enabled (D-: 2.0V, D+: 2.7V) 11b: SE1 2.5A mode enabled (D-: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. 0: Battery charging support disabled 1: Battery charging support enabled

TABLE 111: PORT 2 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P2 OFFSET: 343Dh RESET = 00h			Port 2 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b: 500 mA 01b: 1000 mA 10b: 1500 mA 11b: 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 0: DCP disabled 1: DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D- while shorting D+/D- together to allow certain Chinese market phones to charge. 0: China mode disabled 1: China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b: SE1 mode disabled 01b: SE1 1A mode enabled (D-: 2.7V, D+: 2.0V) 10b: SE1 2A mode enabled (D-: 2.0V, D+: 2.7V) 11b: SE1 2.5A mode enabled (D-: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. 0: Battery charging support disabled 1: Battery charging support enabled

TABLE 112: PORT 3 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P3 OFFSET: 343Eh RESET = 00h			Port 3 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b: 500 mA 01b: 1000 mA 10b: 1500 mA 11b: 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 0: DCP disabled 1: DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D- while shorting D+/D- together to allow certain Chinese market phones to charge. 0: China mode disabled 1: China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b: SE1 mode disabled 01b: SE1 1A mode enabled (D-: 2.7V, D+: 2.0V) 10b: SE1 2A mode enabled (D-: 2.0V, D+: 2.7V) 11b: SE1 2.5A mode enabled (D-: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. 0: Battery charging support disabled 1: Battery charging support enabled

TABLE 113: PORT 4 BATTERY CHARGING CONFIGURATION

BC_CONFIG_P4 OFFSET: 343Fh RESET = 00h			Port 4 Battery Charging Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:6	UCS_LIM	R/W	When controlling UCS through I^2C, this sets the current limit. 00b: 500 mA 01b: 1000 mA 10b: 1500 mA 11b: 2000 mA
5	DCP	R/W	USB-IF Dedicated Charging Mode Enable. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 0: DCP disabled 1: DCP enabled
4:3	CHINA_MODE	R/W	China mode. Enables a 125k pull-up to D+/D- while shorting D+/D- together to allow certain Chinese market phones to charge. 0: China mode disabled 1: China mode enabled
2:1	SE1_EN[1:0]	R/W	Enables SE1 charging mode for certain devices. This mode is only activated when a USB host is not present. When a host is present, the mode of operation is CDP. When SE1 mode and DCP mode are both enabled, the hub toggles between the two modes of operation as necessary to ensure the device can charge. 00b: SE1 mode disabled 01b: SE1 1A mode enabled (D-: 2.7V, D+: 2.0V) 10b: SE1 2A mode enabled (D-: 2.0V, D+: 2.7V) 11b: SE1 2.5A mode enabled (D-: 2.7V, D+: 2.7V)
0	BC_EN	R/W	Battery Charging Support Enable. This bit enables CDP and must be set for any battery charging functions to be enabled. Other functions in addition to CDP are enabled by setting their respective bits in addition to this bit. 0: Battery charging support disabled 1: Battery charging support enabled

TABLE 114: FLEX_IN_PORT1

FLEX_IN_PORT1 Offset: 3442h RESET = 00h			FlexConnect Trigger Input Configuration Port 1 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 1 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b: FlexConnect trigger is disabled. 1b: FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 115: FLEX_IN_PORT2

FLEX_IN_PORT2 Offset: 3443h RESET = 00h			FlexConnect Trigger Input Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 2 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b: FlexConnect trigger is disabled. 1b: FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 116: FLEX_IN_PORT3

FLEX_IN_PORT3 Offset: 3444h RESET = 00h			FlexConnect Trigger Input Configuration Port 3 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 3 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b: FlexConnect trigger is disabled. 1b: FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 117: FLEX_IN_PORT4

FLEX_IN_PORT4 Offset: 3445h RESET = 00h			FlexConnect Trigger Input Configuration Port 4 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_IN_EN	R/W	This bit is used to enable FlexConnect trigger for Port 4 through the PIO input. The PIO is specified in the FLEX_IN_IO field. 0b: FlexConnect trigger is disabled. 1b: FlexConnect trigger is enabled.
6:3	RESERVED	R/W	Reserved
2:0	FLEX_IN_IO	R/W	Selects the PIO used for FlexConnect trigger 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 118: FLEX_OUT_PORT1

FLEX_OUT_PORT1 Offset: 3446h RESET = 00h			FlexConnect State Indicator Configuration Port 1 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 1 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b: FlexConnect state indicator is disabled. 1b: FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO active state polarity 0b: PIO is driven active low in Flex state. 1b: PIO is driven active high in Flex state.
5	FLEX_OUT_OD	R/W	This bit is used to enable open drain output. 0b: PIO output is set as standard push-pull. 1b: PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 119: FLEX_OUT_PORT2

FLEX_OUT_PORT2 Offset: 3447h RESET = 00h			FlexConnect State Indicator Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for port 2 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b: FlexConnect state indicator is disabled. 1b: FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO active state polarity 0b: PIO is driven active low in Flex state. 1b: PIO is driven active high in Flex state.
5	FLEX_OUT_OD	R/W	This bit is used to enable open drain output. 0b: PIO output is set as standard push-pull. 1b: PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 120: FLEX_OUT_PORT3

FLEX_OUT_PORT3 Offset: 3448h RESET = 00h			FlexConnect State Indicator Configuration Port 3 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for port 3 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b: FlexConnect state indicator is disabled. 1b: FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO active state polarity 0b: PIO is driven active low in Flex state. 1b: PIO is driven active high in Flex state.
5	FLEX_OUT_OD	R/W	This bit is used to enable open drain output. 0b: PIO output is set as standard push-pull. 1b: PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 121: FLEX_OUT_PORT4

FLEX_OUT_PORT4 Offset: 3449h RESET = 00h			FlexConnect State Indicator Configuration Port 4 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_OUT_EN	R/W	This bit is used to enable the FlexConnect state indicator for Port 4 through the PIO input. The PIO is specified in the FLEX_OUT_IO field. 0b: FlexConnect state indicator is disabled. 1b: FlexConnect state indicator is enabled.
6	FLEX_OUT ACTIVE_HIGH	R/W	Selects PIO active state polarity 0b: PIO is driven active low in Flex state. 1b: PIO is driven active high in Flex state.
5	FLEX_OUT_OD	R/W	This bit is used to enable open drain output. 0b: PIO output is set as standard push-pull. 1b: PIO output is set as open drain.
4:3	RESERVED	R/W	Reserved
2:0	FLEX_OUT_IO	R/W	Selects the PIO used as the FlexConnect state indicator 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 122: FLEX_PRTCTL_PORT1

FLEX_PRTCTL_PORT1 Offset: 344Ah RESET = 00h			FlexConnect PRTCTL Configuration Port 1 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for Port 1. The PIO is specified in the FLEX_PRTCTL_IO field. 0b: Disables Flex PRTCTL1 output 1b: Enables Flex PRTCTL1 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL1 output mode 00b: PRTCTL1 is tristated. 01b: PRTCTL1 is driven high. 10b: PRTCTL1 is driven low. 11b: PRTCTL1 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL1 to output. 0b: Flex PRTCTL1 output is disabled. 1b: Flex PRTCTL1 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL1 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 123: FLEX_PRTCTL_PORT2

FLEX_PRTCTL_PORT2 Offset: 344Bh RESET = 00h			FlexConnect PRTCTL Configuration Port 2 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for Port 2. The PIO is specified in the FLEX_PRTCTL_IO field. 0b: Disables Flex PRTCTL2 output 1b: Enables Flex PRTCTL2 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL2 output mode 00b: PRTCTL2 is tristated. 01b: PRTCTL2 is driven high. 10b: PRTCTL2 is driven low. 11b: PRTCTL2 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL2 to output. 0b: Flex PRTCTL2 output is disabled. 1b: Flex PRTCTL2 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL2 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 124: FLEX_PRTCTL_PORT3

FLEX_PRTCTL_PORT3 Offset: 344Ch RESET = 00h			FlexConnect PRTCTL Configuration Port 3 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for Port 3. The PIO is specified in the FLEX_PRTCTL_IO field. 0b: Disables Flex PRTCTL3 output 1b: Enables Flex PRTCTL3 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL3 output mode 00b: PRTCTL3 is tristated. 01b: PRTCTL3 is driven high. 10b: PRTCTL3 is driven low. 11b: PRTCTL3 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL3 to output. 0b: Flex PRTCTL3 output is disabled. 1b: Flex PRTCTL3 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL3 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 125: FLEX_PRTCTL_PORT4

FLEX_PRTCTL_PORT4 Offset: 344Dh RESET = 00h			FlexConnect PRTCTL Configuration Port 4 Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_PRTCTL_EN	R/W	This bit is used to enable Flex PRTCTL for Port 4. The PIO is specified in the FLEX_PRTCTL_IO field. 0b: Disables Flex PRTCTL4 output 1b: Enables Flex PRTCTL4 output
6:5	PRTCTL_OUT[1:0]	R/W	Selects the Flex PRTCTL4 output mode 00b: PRTCTL4 is tristated. 01b: PRTCTL4 is driven high. 10b: PRTCTL4 is driven low. 11b: PRTCTL4 is pulled up with internal pull-up.
4	RESERVED	R/W	Reserved
3	FLEX_PRTCTL_OEN	R/W	This bit is used to enable the Flex PRTCTL4 to output. 0b: Flex PRTCTL4 output is disabled. 1b: Flex PRTCTL4 output is enabled.
2:0	FLEX_PRTCTL_IO	R/W	Selects the PIO used as Flex PRTCTL4 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 126: FLEX_VBUSDET

FLEX_VBUSDET Offset: 344Eh RESET = 00h			FlexConnect VBUSDET Configuration Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7	FLEX_VBUSDET_EN	R/W	This bit is used to select the source for VBUS_DET while in Flex state. 0b: VBUS_DET Hub pin is the VBUS_DET in Flex state. 1b: PFx pin selected in FLEX_VBUSDET_IO is the VBUS_DET in Flex state.
6	FLEX_VBUSDET_HIGH	R/W	0b: VBUS_DET is driven as selected by FLEX_VBUSDET_EN. 1b: VBUS_DET is driven high internally.
5:3	RESERVED	R/W	Reserved
2:0	FLEX_VBUSDET_IO	R/W	Selects the PFx used as Flex VBUSDET 000b: PF2 001b: PF3 010b: PF4 011b: PF5 100b: PF6 101b: PF7

TABLE 127: FLEX_ATTACHDELAY

FLEX_ATTACH_DELAY Offset: 344Fh RESET = 00h			FlexConnect Hub Attach Delay Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	FLEX_ATTACH_DELAY	R/W	This field specifies the delay in 10-millisecond increments after Flex-Connect is initiated before the hub is attached. This might be required to provide a debounce time between a USB device detach and a subsequent attach.

TABLE 128: ROLESWITCHDELAY

ROLE_SWITCH_DELAY Offset: 3450h RESET = 00h			Role Switch Delay Base Address: BFD2_0000h
Bit	**Name**	**R/W**	**Description**
7:0	ROLE_SWITCH_DELAY	R/W	This field specifies the delay in 10-millisecond increments after the SET_ROLE_SWITCH command is initiated before the role switch is done. This might be required to provide a debounce time between a USB device detach and a subsequent attach.

TABLE 129: MANUFACTURER STRING LENGTH

MFG_STR_LEN OFFSET: 346Ah RESET = 1Eh			Manufacturer String Length Base Address: BFD2_0000h
BIT	**Name**	**R/W**	**Description**
7:0	Length	R/W	Manufacturer String Descriptor size. This must be same as the value in the Length field of the Manufacturer String Descriptor.

TABLE 130: PRODUCT STRING LENGTH

PROD_STR_LEN OFFSET: 3472h RESET = 10h			Product String Length Base Address: BFD2_0000h
BIT	**Name**	**R/W**	**Description**
7:0	Length	R/W	Product String Descriptor size. This must be same as the value in the Length field of the Product String Descriptor.

4.0 SMBUS CONFIGURATION

The SMBus configuration begins in the SOC Configuration Stage. In this stage, the SOC may modify any of the configuration settings to customize the hub to their purposes. The SOC can configure the hub as Full-speed only, or have the hub report a port as non-removable. The SOC can also disable a port entirely to conserve power. The hub can be addressed at the address 2Dh and interprets the data bytes as shown in the following sub-sections.

4.1 SMBus Block Write

The SMBus block write consists of an Address+Direction(0) byte followed by the 16-bit memory address, split into two bytes. The address is used for special commands and as a pointer to the hub's internal memory. Following the address, the next byte of data corresponds to the count of data bytes that follows, which is up to 128 bytes in a block. Finally, a 00h write is used to terminate the write operation, followed by the SMBus stop signal.

TABLE 131: SMBUS BLOCK WRITE

Field	Description
Start bit (S)	Start condition
I2C Address	7-bit SMBus Address (2Dh)
Direction	1-bit, 0 = Write
ACK	Acknowledge from SMBus slave
Offset MSB	Most Significant Byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus slave
Offset LSB	Least Significant Byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus slave
Count	Start condition
ACK	Acknowledge from SMBus slave
Data 0	First byte of data
ACK	Acknowledge from SMBus slave
Data 1	Second byte of data
ACK	Acknowledge from SMBus slave
Data n	Last byte of data
ACK	Acknowledge from SMBus slave
Stop (P)	Stop condition

Note: The 7-bit address of the hub is 2Dh, or the first byte is 5Ah for an SMBus write.

4.2 SMBus Block Read

The SMBus block read consists of an Address+Direction(0) byte with the 16-bit memory address, followed by a repeat Start signal and an Address+Direction(1) byte. The hub then starts to output the count (128 bytes) and the contents of the internal registers starting at the 16-bit address specified.

TABLE 132: SMBUS BLOCK READ

Field	Description
Start bit (S)	Start condition
I2C Address	7-bit SMBus Address (2Dh)
Direction	1-bit, 0 = Write
ACK	Acknowledge from SMBus slave
Offset MSB	Most Significant Byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus slave
Offset LSB	Least Significant Byte of address to internal buffer (00h)
ACK	Acknowledge from SMBus slave
Start bit (Sr)	Repeated Start condition
I2C Address	7-bit SMBus Address (2Dh)
Direction	1-bit, 1 = Read
ACK	Acknowledge from SMBus slave
Count	Number of bytes to read from slave
ACK	Acknowledge from SMBus master
Data 0	First byte of data from SMBus slave
ACK	Acknowledge from SMBus master
Data 1	Second byte of data from SMBus slave
ACK	Acknowledge from SMBus master
Data n	Last data byte from SMBus slave
ACK	Acknowledge from SMBus master
Stop (P)	Stop condition

Note: The 7-bit address of the hub is 2Dh, or the first byte is 5Ah for a write and 5Bh for a read.

4.3 Special Commands

Special commands can be sent in the place of the 16-bit address bytes. These commands are used to enumerate the hub, access the configuration registers, or reset the device. The commands consist of the 16-bit command followed by a 00h byte to terminate the command.

TABLE 133: SPECIAL SMBUS COMMANDS

Operation	OPCODE	Description
Configuration Register Access	9937h	Read and Write Configuration registers
USB Attach	AA55h	Exit SOC_CONFIG and Enter HUB_CONFIG Stage
USB Attach with SMBus Runtime Access	AA56h	Exit SOC_CONFIG and Enter HUB_CONFIG stage with SMBus slave enabled
OTP Program	9933h	Permanently program configuration commands to the OTP
OTP Read	9934h	Read the values of the OTP register

Note: OTP Program and OTP Read commands reference data starting at configuration register 4800h.

4.4 Accessing Configuration Registers

The Configuration Register Access command allows the SMBus Master to read or write to the internal registers of the hub. When the Configuration Register Access command is sent, the hub interprets the memory starting at offset 0000h as in Table 134.

TABLE 134: MEMORY FORMAT FOR CONFIGURATION REGISTER ACCESS

Buffer Address	Description	Notes
0000h	Direction	0 = Register Write, 1 = Register Read
0001h	Data Length	Number of bytes to read or write, maximum of 128 bytes
0002h-0005h	Memory Address	32-bit memory address to read or write in big endian format
0006h~0084h	Data	Data to write or read from the Memory Address, number of bytes specified in the Data Length field

4.4.1 CONFIGURATION REGISTER WRITE EXAMPLE

To write to a configuration register:

1. Write the command block to the buffer area.
2. Execute the special Configuration Register Access command.

The following example shows how the SMBus messages are formatted to set the VID of the hub to a custom value, 1234h:

1. Write the command block to the buffer area:

TABLE 135: SMBUS WRITE COMMAND BLOCK FOR REGISTER WRITE

Byte	Value	Comment
0	5Ah	Slave address plus write bit (2Dh left shifted by 1)
1	00h	Buffer address MSB **00**00h
2	00h	Buffer address LSB 00**00**h
3	08h	Number of bytes to write to command block buffer area
4	00h	Write VID Register
5	02h	Writing two bytes to VID register
6	BFh	VID is in register **BF**803000h
7	80h	VID is in register BF**80**3000h
8	30h	VID is in register BF80**30**00h
8	00h	VID is in register BF8030**00**h
A	34h	LSB of Vendor ID 12**34**h
B	12h	MSB of Vendor ID **12**34h

2. Execute the Configuration Register Access command:

TABLE 136: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command Completion

4.4.2 CONFIGURATION REGISTER READ EXAMPLE

To read configuration registers:

1. Write the command block to the buffer area.
2. Execute the Configuration Register Access command.
3. Read the data from the memory.

The following example shows how to read the PID:

1. Write the data to the memory of the hub:

TABLE 137: SMBUS WRITE COMMAND BLOCK FOR REGISTER READ

Byte	Value	Comment
0	5Ah	Slave address plus write bit (2Dh left shifted by 1)
1	00h	Memory address **00**00h
2	00h	Memory address 00**00**h
3	06h	Number of bytes to write to memory
4	01h	Read Configuration register
5	02h	Reading two bytes from PID register
6	BFh	VID is in register **BF**803002h
7	80h	VID is in register BF**80**3002h
8	30h	VID is in register BF80**30**02h
9	02h	VID is in register BF8030**02**h

2. Execute the Configuration Register Access command:

TABLE 138: CONFIGURATION REGISTER ACCESS COMMAND

Byte	Value	Comment
0	5Ah	Address plus write bit (2Dh left shifted by 1)
1	99h	Command **99**37h
2	37h	Command 99**37**h
3	00h	Command Completion

3. Read back data starting at memory offset 04h, which is where the Data byte starts:

TABLE 139: EXAMPLE SMBUS READ COMMAND

Byte	Value	Comments
0	5Ah	Slave address plus write bit (2Dh left shifted by 1)
1	00h	Memory Address **00**06h
2	06h	Memory Address 00**06**h
3	5Bh	Slave address plus read bit (2Dh left shifted by 1 + 1)
4	08h	Device sends a count of 8 bytes
5	16h	PID LSB
6	49h	PID MSB

Note: Although the device can send out 8 bytes, it is not necessary to read the 8 bytes. The SMBus Master can send a stop at any time.

4.5 SMBus Runtime

After the hub is enumerated (after USB Attach with SMBus Runtime Access), the same registers can be accessed during runtime.

5.0 OTP CONFIGURATION

The USB47xx/USB49xx hubs have 8k bytes of one-time programmable (OTP) memory to enable customization and limited firmware updates in the field. OTP memory organization and OTP configuration are described in the next sections.

5.1 OTP Memory Organization

The OTP memory is divided into four regions as follows:

- OTP Flags
- Configuration Commands
- Blank Memory
- Configuration Index Records

Figure 2 shows the OTP memory organization.

FIGURE 2: OTP MEMORY ORGANIZATION

	0h	1h	2h	3h	4h	5h	6h	7h	8h	9h	Ah	Bh	Ch	Dh	Eh	Fh
0000h	**OTP Flags**															
0010h						**Configuration Commands**										
0020h																
0030h								00h	00h	00h	00h	00h	00h	00h	00h	00h
0040h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
0050h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
	00h	00h	00h	00h	00h	**Blank Memory**							00h	00h	00h	00h
...	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FC0h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h	00h
1FD0h	00h	00h	00h	00h	00h	00h	00h									
1FE0h						**Configuration Index Records**										
1FF0h																

5.1.1 OTP FLAGS

The first two bytes of the OTP memory are the OTP Flags indicating how many times the OTP has been programmed by the MPLAB Connect Configurator tool (when programming via SMBus, these bits are not updated). For an unprogrammed part, these two bytes are 0000h. Every time the OTP is programmed using MPLAB Connect Configurator, a bit is set. When the first OTP is programmed, this becomes 0001h, then 0003h, 0007h, and continues until all bits are set. After all OTP Flag bits are set, OTP programming is still possible as long as OTP space is available.

5.1.2 CONFIGURATION COMMANDS

The Configuration Commands section grows from the start of the OTP data. These are the commands that are appended every time a Program OTP command is sent through SMBus and can vary in length depending on how many configuration registers have been manipulated.

5.1.3 BLANK MEMORY

This memory region is initially 00h on an unprogrammed part and decreases in size as configuration commands and configuration index records are programmed.

5.1.4 CONFIGURATION INDEX RECORDS

The Configuration Index Records area contains Configuration Index Records that are automatically generated when the OTP data is programmed. A Configuration Index Record is always 8 bytes per OTP program and is appended to the back of the OTP memory space every time the Program OTP command is sent. It contains a checksum to confirm that the configuration command was written correctly as well as information on the location of the configuration commands within the OTP memory space and total length. The Configuration Index Record format is shown in Figure 3.

FIGURE 3: CONFIGURATION INDEX RECORD FORMAT

BYTE	1	2	3	4	5	6	7	8
Description	Signature			Checksum	CFG ADDRESS		CFG LENGTH	
Contents	I (49h)	D (44h)	X (58h)	Checksum	MSB	LSB	MSB	LSB

5.2 OTP Configuration using MPLAB® Connect Configurator

The easiest method to program the USB47xx/USB49xx Hub OTP is with the *MPLAB Connect Configurator* tool, available at: http://www.microchip.com/design-centers/usb/mplab-connect-configurator.

MPLAB Connect Configurator programs the configuration in the next available slot in the Configuration Commands area, programs the Index Record in the Configuration Index Records area, and updates the OTP Flags count field.

This tool can be used to generate a configuration file (.cfg) and to program the generated configuration file permanently to the hub's OTP memory space using USB commands.

Alternatively, the .cfg file can be constructed manually using a binary/hex editor. Follow the formatting instructions shown in Table 140, and see the example in Section 5.3.1, "OTP Configuration File Examples".

5.3 OTP Configuration using SMBus

The OTP memory can be programmed through the SMBus interface in the SOC_CONFIG stage (during start-up). The OTP memory is configured as a series of commands that manipulates the configuration registers. The USB49xx/USB47xx hubs have a total of 8 kB of OTP memory space, and each byte of OTP memory may be written only once. The OTP memory space can be successively written to (each programming instance appends the new command to the bottom of the OTP memory space) until the space is completely filled.

During the HUB_CONFIG stage, temporary OTP configuration registers are written to. The contents in the OTP configuration registers are then permanently loaded to the OTP memory space after sending a special OTP program command. These registers permanently change the default behavior of the hub during normal operation. These commands are stored into the OTP memory as shown in Figure 2.

TABLE 140: OTP STORAGE COMMANDS

Command	OPCODE	Length	Description
NULL	00h	N/A	No action, advance memory counter by 1 and move to the next instruction
WRITE_BYTES_SHORT	01h-7Fh	OPCODE	Writes the following bytes starting at the current memory address for length = OPCODE
SET_MEMORY ADDRESS	80h	4	Load the MEMORY_ADDRESS register with the four bytes following the opcode. The address is specified in little-endian format.
SKIP_MEMORY_WRITE	81h-FDh	OPCODE [6:0]	Skip the length number of bytes starting at the location of the MEMORY_ADDRESS register. At the end of the operation, the MEMORY_ADDRESS register is incremented by length = OPCODE[6:0].
SET_MODE_WRITE_BYTE	FEh	1	If the byte following SET_MODE = 00h, all writes replace the memory value at that location.
SET_MODE_SET_BITS			If the byte following SET_MODE = 01h, all writes are ORed in. This is a mechanism to set the selected bits in a register without changing the others. Set the bits to be set.
SET_MODE_CLEAR_BITS			If the byte following SET_MODE = 02h, all writes are NANDed in. This is a mechanism to clear the selected bits in a register without changing the others. Set the bits to be cleared.
STOP	FFh	N/A	After the storage commands are complete, this indicates the termination of the command sequence.

5.3.1 OTP CONFIGURATION FILE EXAMPLES

These examples show the hex data in a configuration file.

5.3.1.1 Example: Configuring PF6 as an output assuming PF6 is configured as a GPIO via the device CONFIGURATION STRAPx pins

To configure PF6 as an output assuming that PF6 is configured as a GPIO via the device CONFIGURATION STRAPx pins, the corresponding bit in the output enable register must be set, which from Table 3 is PIO10.

TABLE 141: EXAMPLE: SET BIT COMMAND SEQUENCE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	BFh	Address **BF**800901h
3	80h	Address BF**80**0901h
4	09h	Address BF80**09**01h
5	01h	Address BF8009**01**h
6	FEh	SET_MODE command
7	01h	SET_BITS mode
8	01h	Data length of 1 byte
9	04h	Set PIO32_OEN[10]
10	FFh	Stop command

5.3.1.2 Example: Changing the USB downstream Port 1 Boost Register to increase the HS output current by 5%

TABLE 142: EXAMPLE: WRITE BYTE COMMAND SEQUENCE

Byte	Value	Comment
1	80h	SET_ADDRESS command
2	BFh	Address **BF**8064CAh
3	80h	Address BF**80**64CAh
4	64h	Address BF80**64**CAh
5	CAh	Address BF8064**CA**h
6	FEh	SET_MODE command
7	01h	WRITE_BYTE mode
8	01h	Data length of 1 byte
9	03h	Increase HS output current by 5%
10	FFh	Stop command

5.3.2 OTP CONFIGURATION VIA SMBUS

The following commands can be used to access and program the OTP memory. These can be used by ATE equipment.

TABLE 143: SPECIAL OTP SMBUS COMMANDS

Operation	OPCODE	Description
SMB_CMD_OTP	9933h	Execute OTP Command based on CMD_TYPE
SMB_CMD_READ_OTP	9934h	Read OTP register
SMB_CMD_OTP_ATE	9939h	Execute OTP Command based on CMD_TYPE. This command is for use with automated test equipment (ATE). Command success or failure is reported via signal pins. The device does not respond afterwards until reset. • Command status pin: PRT_PWR1 (0 = Passed, 1 = OTP Failed) • Command completion pin: PRT_PWR2 (0 = In progress, 1 = done)

Note: Before any OTP commands can be executed, a data structure must be created in the memory using SMBus block writes.

5.3.3 SMBUS OTP COMMAND STRUCTURE

The following OTP command structure is used for accessing the OTP memory.

TABLE 144: SMBUS OTP COMMAND STRUCTURE

Buffer Address	Description	Notes
BFD2_2100h	CMD_TYPE	Command Type is one of the commands in Table 145.
BFD2_2101h	ADDR[15:0]	OTP Address to read from or write to, set to 0000h
BFD2_2103h	LENGTH[15:0]	Number of bytes to transfer
BF90_7000h	Data	Data for OTP transaction. MULTI_HOST_CLK_EN and MHB_MEM_CLK_EN bits must be set before accessing the DATA_BUFFER.
BFD2_3419h	SMBusOTPResult	Result of OTP operation as specified in the OTP Return status

TABLE 145: OTP COMMAND TYPE

Code	CMD_TYPE	Description
00h	SMB_OTP_RAW_PGM	This is a raw programming mode where the OTP will be programmed starting at ADDR for size LENGTH. If an OTP configuration block is programmed, the index record must be updated at the appropriate OTP location for the firmware to consider this record as a valid OTP configuration block. Status on completion: • 00h = OTP was programmed and verified successfully • 01h = OTP programming failed
03h	SMB_OTP_PGM	This programs the OTP record after the last programmed OTP record, including the index record consisting of the IDX signature, record checksum, start offset, and length. The LENGTH and DATA buffer must be initialized before issuing this command. Status on completion: • 00h = OTP was programmed and verified successfully • 01h = OTP programming failed
05h	SMB_OTP_BLANKCHECK	This verifies that the OTP is blank and has not been programmed. Status on completion: • 00h = PASS; OTP is blank and has not been programmed • 01h = FAIL; OTP blank check failed
06h	SMB_OTP_RESET	This resets the OTP core. Status on completion: • 00h = OTP_NO_ERROR/
07h	SMB_OTP_READ	This command reads the number of bytes specified in the LENGTH field and stores them in data buffer. Status on completion: • 00h = OTP data was read successfully • 01h = OTP read failed

5.3.4 STEPS FOR PROGRAMMING OTP USING SMBUS

1. Write the OTP memory structure.
2. Send the Execute OTP command.
3. Read SMBus OTP Result.
4. When programming on ATE, use the PRT_PWR1 and PRT_PWR2 to read the status.

5.3.5 SMBUS OTP PROGRAMMING EXAMPLE

This example changes the PID LSB at BF803002h to 34h, and the PID MSB at BF803003h to 12h.

The OTP configuration data for this is `80 BF 80 30 02 02 34 12 FF`.

Write OTP Memory Structure

1. Set MULTI_HOST_CLK_EN and MHB_MEM_CLK_EN at BF80_0B01h: `5A 00 00 07 00 01 BF 80 0B 01 E5`
2. Write SMBus Configuration Register Access command: `5A 99 37 00`
3. Write OTP Command, Address, Length at BFD2_2100h: `5A 00 00 0B 00 05 BF D2 21 00 03 00 00 00 09`
4. Write SMBus Configuration Register Access command: `5A 99 37 00`
5. Write OTP Patch to Data Area at BF90_7000h: `5A 00 00 0F 00 09 BF 90 70 00 80 BF 80 30 02 02 34 12 FF`
6. Write SMBus Configuration Register Access command: `5A 99 37 00`

Send the Execute OTP Command

7. Write to SMBus: `5A 99 33 00`

Read SMBus OTP Result Register

8. Set the command block for status read at BFD2_3419h: `5A 00 00 06 01 01 BF D2 34 19`
9. Write SMBus Configuration Register Access command: `5A 99 37 00`
10. Read Data: `5A 00 06 5B 08 XX`

Note: `XX` is the status returned: 00 = Pass.

5.3.6 SMBUS OTP RAW PROGRAMMING EXAMPLE

This example changes the OTP Flags field to 0001h to indicate that the first OTP block (from the previous example) was programmed. This assumes that the OTP Flags are initially 0000h. In a real application, the OTP Flags must be read first to identify the next available bit.

Write OTP Memory Structure

1. Set MULTI_HOST_CLK_EN and MHB_MEM_CLK_EN at BF80_0B01h: `5A 00 00 07 00 01 BF 80 0B 01 E5`
2. Write SMBus Configuration Register Access command: `5A 99 37 00`
3. Write OTP command, Address, Length at BFD2_2100h: `5A 00 00 0B 00 05 BF D2 21 00 00 00 00 00 02`
4. Write SMBus Configuration Register Access command: `5A 99 37 00`
5. Write OTP Flags to Data Area at BF90_7000h: `5A 00 00 08 00 02 BF 90 70 00 00 01`
6. Write SMBus Configuration Register Access command: `5A 99 37 00`

Send the Execute OTP Command

7. Write to SMBus: `5A 99 33 00`

Read SMBus OTP Result Register

8. Set the command block for status read at BFD2_3419h: `5A 00 00 06 01 01 BF D2 34 19`
9. Write SMBus Configuration Register Access command: `5A 99 37 00`
10. Read Data: `5A 00 06 5B 08 XX`

5.4 OTP Configuration via USB

5.4.1 PROGRAM OTP SETUP PACKET

Once the OTP programming parameters are set in SRAM, the USB host must issue a CMD_OTP_PROGRAM setup packet.

TABLE 146: OTP PROGRAM SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, using vendor-specific command, targeting interface
bRequest	0x00	CMD_OTP_PROGRAM
wValue	OTP_ADRESS	Address of the OTP to be written
wIndex	0x00	Reserved
wLength	Data Length	Length of data to be written

Command phase: Receives the setup packet with the parameters specified above

Data phase: Receives the data bytes of length wLength and programs the OTP accordingly

Status phase:

- STALL – on programming error
- ACK – on successful completion of programming

Use the CMD_OTP_GET_STATUS to get the status for more information on the failure.

5.4.2 READ OTP SETUP PACKET

Issue this command to read the OTP memory.

TABLE 147: OTP READ SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC1	Device-to-host to data transfer using vendor-specific command targeting interface
bRequest	0x01	CMD_OTP_READ
wValue	OTP_ADRESS	Address of the OTP ROM to be read
wIndex	0x00	Reserved
wLength	Data Length	Length of data to be read

Command phase: Receives the SETUP packet with the parameters specified above

Data phase: Sends the data bytes of length wLength from address wValue

Status phase:

- STALL – on read error
- ACK – on successful completion of command

5.4.3 GET STATUS OTP SETUP PACKET

Issue this command to get the OTP status.

TABLE 148: OTP GET STATUS SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC1	Device-to-host to data transfer using vendor-specific command targeting interface
bRequest	0x02	CMD_OTP_GET_STATUS
wValue	0x0000	Address of the OTP ROM to be read
wIndex	0x0000	Reserved
wLength	0x01	One byte status to be returned

Command phase: Receives the SETUP packet with the parameters specified above

Data phase: Sends the status byte

Status phase:

- STALL – on read error
- ACK – on successful completion of command

5.4.4 STATUS CODE

The status code returned is shown in Table 149.

TABLE 149: OTP STATUS CODES

Status Code	Description
0x00	Command successful completion
0x01	Generic error

5.4.5 SET OTP PROGRAM CODE

The OTP memory can be programmed by either the PROGRAM command or the PROGRAMVERIFY command. CMD_OTP_SET_PROGRAM_MODE selects the internal command that the ROM will issue to the OTP during subsequent CMD_OTP_PROGRAM commands.

The default mode in the ROM is PROGRAMVERIFY (without requiring the Set OTP Program Mode command to be issued always).

TABLE 150: SET OTP PROGRAM MODE SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device to data transfer using vendor-specific command targeting interface
bRequest	0xF1	CMD_OTP_SET_PROGRAM_MODE
wValue	Programming Option	Indicates if the future CMD_OTP_PROGRAM commands will issue the PROGRAMVERIFY or PROGRAM command 0x01 – PGMVFY 0x02 – PROGRAM
wIndex	0x0000	Reserved
wLength	Data Length	No Data command

Command phase: Receives the SETUP packet as specified in the table.

Status phase:

- ACK – On successful completion of the command

5.5 Memory Access during Runtime via USB

The hub memory mapped registers can be accessed during runtime via USB.

Note: Not all registers should be modified during runtime as this could affect normal operation.

TABLE 151: MEMORY WRITE SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x40	Host-to-device data transfer, vendor class, targeted to interface
bRequest	0x03	CMD_MEMORY_WRITE
wValue	ADDR_LO	Lower 16 bits of the Target Memory Address in little-endian Format
wIndex	ADDR_HI	Upper 16 bits of the Target Memory Address in little-endian Format
wLength	Data Length	Length of data to be written

Command phase: Receives the SETUP packet with the parameters specified above

Data phase: Receives the data bytes of length wLength and writes data starting at the Target Memory Address

Status phase:

- ACK – on successful completion of memory write

TABLE 152: MEMORY READ SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC0	Device-to-host data transfer, vendor class, targeted to interface
bRequest	0x04	CMD_MEMORY_READ
wValue	ADDR_LO	Lower 16 bits of the Target Memory Address in *little-endian* format
wIndex	ADDR_HI	Upper 16 bits of the Target Memory Address in *little-endian* format
wLength	Data Length	Length of data to read

Command phase: Receives the SETUP packet with the parameters specified above

Data phase: Send the data bytes of length wLength starting from the target memory address

Status phase:

- ACK – on successful completion of programming

5.5.1 USB MEMORY WRITE EXAMPLE

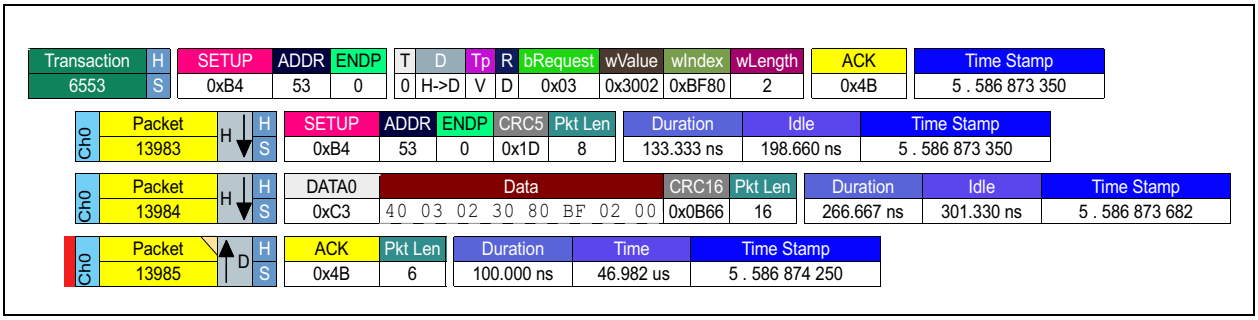
This example changes the product ID (PID) at location BF80_3002h.

1. **Memory Write SETUP Phase Transaction:** The USB host sends the SETUP packet below to the hub feature controller at Endpoint 0.

TABLE 153: MEMORY WRITE SETUP PACKET

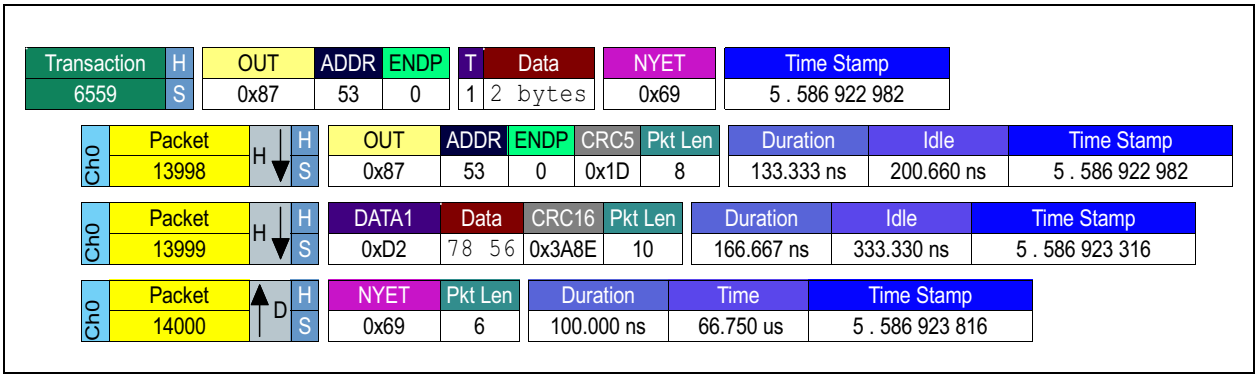
SETUP Packet	Value	Description
bmRequestType	0x40	Host-to-device data transfer, vendor class
bRequest	0x03	CMD_MEMORY_WRITE
wValue	0x3002	Lower 16 bits of the Target Memory Address in *little-endian* format
wIndex	0xBF80	Upper 16 bits of the Target Memory Address in *little-endian* format
wLength	0x0002	Length of data to be written

FIGURE 4: MEMORY WRITE SETUP TRANSACTION



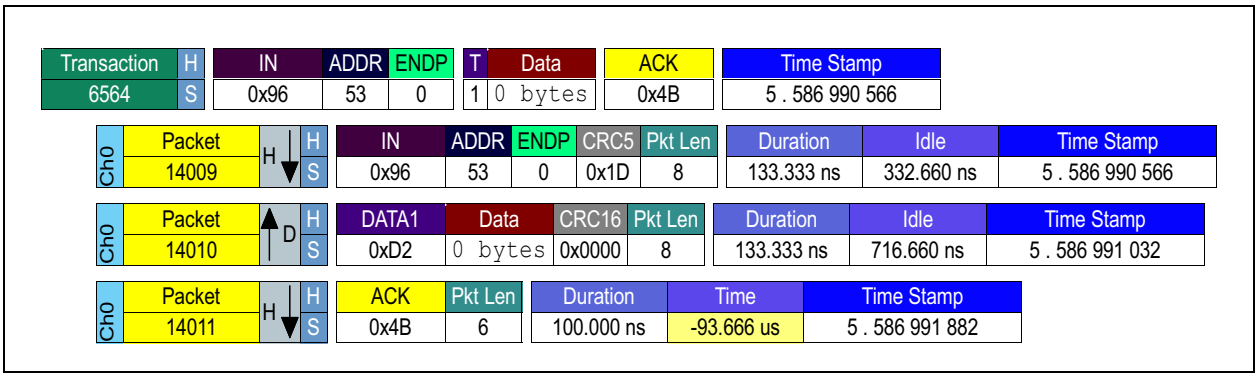
2. **Memory Write Data Phase OUT Transaction:** The USB host sends two data bytes to set BF803002=5678h.

FIGURE 5: MEMORY WRITE OUT TRANSACTION



3. **Memory Write Status Phase IN Transaction:** The USB host sends an IN packet to complete the transfer. The hub feature controller responds with a zero-length data packet.

FIGURE 6: MEMORY WRITE IN TRANSACTION



5.5.2 USB MEMORY READ EXAMPLE

This example reads the PID at location BF80_3002h.

1. **Memory Read SETUP Phase Transaction:** The USB host sends the SETUP packet below to the Hub Feature Controller at Endpoint 0.

TABLE 154: READ SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0xC0	Device-to-host data transfer, vendor class
bRequest	0x04	CMD_MEMORY_READ
wValue	0x3002	Lower 16 bits of the Target Memory Address in *little-endian* format
wIndex	0xBF80	Upper 16 bits of the Target Memory Address in *little-endian* format
wLength	0x0002	Length of data to read

FIGURE 7: MEMORY READ SETUP TRANSACTION

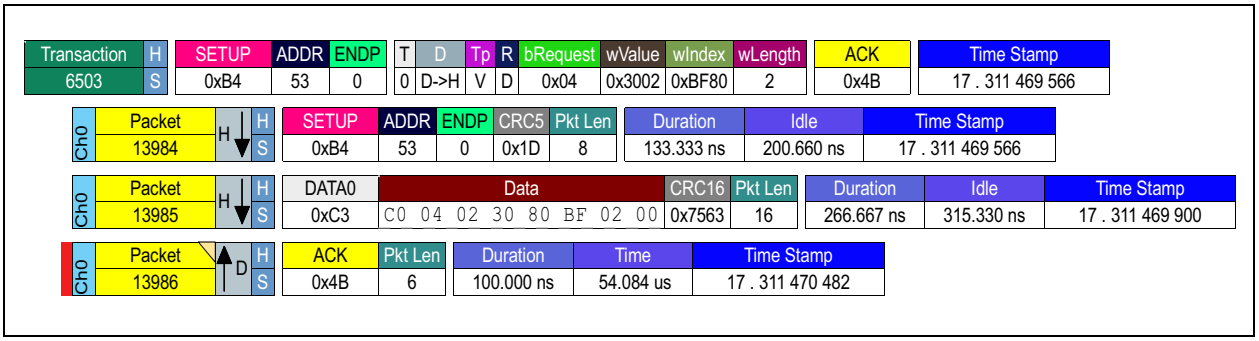
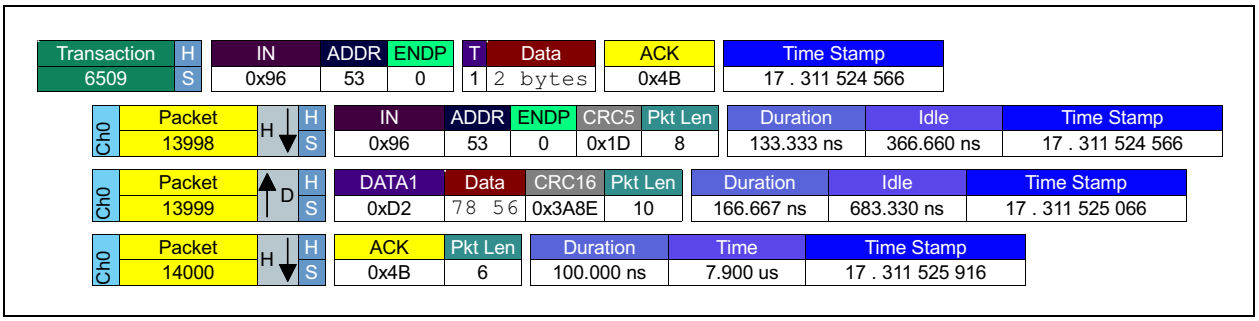
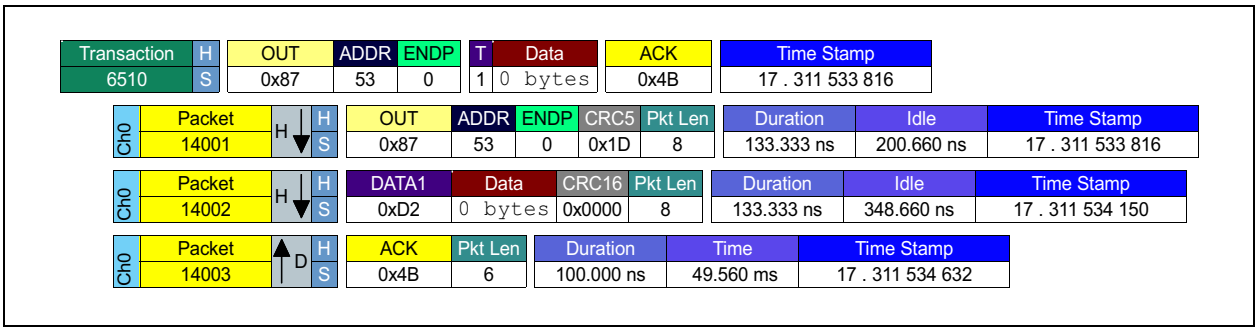


FIGURE 8: MEMORY READ IN TRANSACTION



2. **Memory Read Data Phase IN Transaction:** The USB host sends an IN packet to read the data. The Hub Feature Controller returns two bytes of data to complete the transfer. Data 5678h is read from location BF803002h.
3. **Memory Read Status Phase OUT Transaction:** The USB host sends an OUT packet to complete the transfer. The Hub Feature Controller responds with a zero-length data packet.

FIGURE 9: MEMORY READ OUT TRANSACTION



6.0 FLEXCONNECT COMMAND

This USB command is used to allow one of the downstream ports to switch roles with the upstream port. This is documented here because the use of this command is required to use the special test modes with USB port 0 as described in Table 65. For a more detailed description and general usage of this command, see *AN2341 - USB4715 FlexConnect Operation*.

6.1 FlexConnect Setup Packet

This is a SETUP packet with no data as shown in Table 155.

TABLE 155: FLEX SETUP PACKET

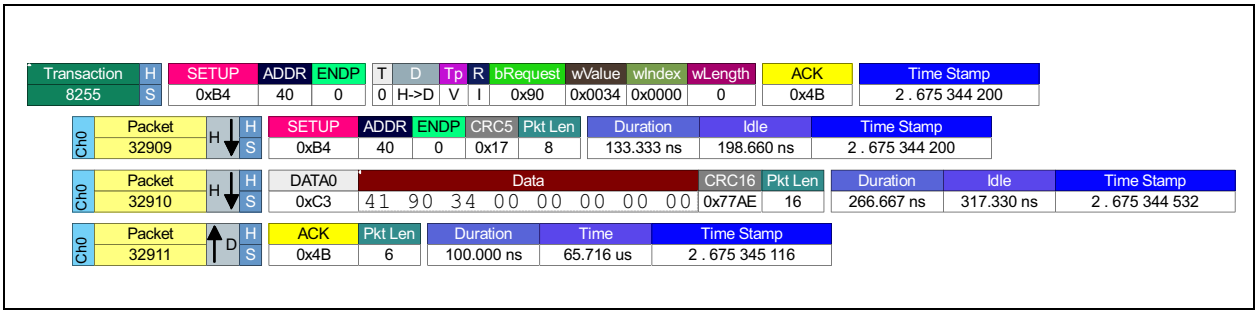
SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, vendor class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0x003X	This is a 16-bit value, with X a 4-bit value as follows: 0001b – port 1 0010b – port 2 0011b – port 3 0100b – port 4
wIndex	0x0000	Reserved
wLength	0x00	No data

6.2 FlexConnect Setup Packet Example

TABLE 156: FLEXCONNECT SETUP PACKET TO PORT 4

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, vendor class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0x0034	FlexConnect session, no timeout (hub will not terminate session), set to port 4
wIndex	0x0000	Reserved
wLength	0x00	No data

FIGURE 10: FLEXCONNECT SETUP TRANSACTION



7.0 DUAL UPSTREAM (DUST) COMMAND (USB4925/USB4927)

This command is used to enable the secondary hub in the USB4925 and USB4927 hubs.This is documented here because it is required to enable the secondary hub before using the special test modes described in Table 70, "Secondary Hub Control Portable Test (USB4925/USB4927)". For a more detailed description and general usage of this command, see *AN2342 - USB4927/USB4925 Dual Upstream Operation*.

7.1 DUST Setup Packet (USB4925/USB4927)

This is a SETUP packet with no data as shown in Table 157.

TABLE 157: DUST SETUP PACKET

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, vendor class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0x005X	This is a 16-bit value, with X a 4-bit value as follows: 0001b – port 1 0010b – port 2 0011b – port 3 0100b – port 4
wIndex	0x0000	Reserved
wLength	0x00	No data

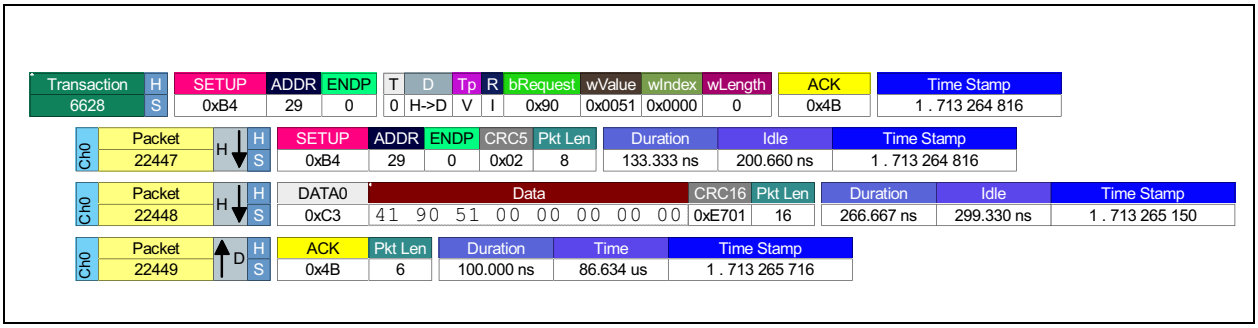
7.2 DUST Setup Packet Example

The following example is a SETUP packet to Port 1.

TABLE 158: DUST SETUP PACKET TO PORT 1

SETUP Packet	Value	Description
bmRequestType	0x41	Host-to-device data transfer, vendor class, targeted to interface
bRequest	0x90	SET_ROLE_SWITCH
wValue	0x0051	DUST session, no timeout (hub will not terminate session), set to Port 1
wIndex	0x0000	Reserved
wLength	0x00	No data

FIGURE 11: DUST SETUP TRANSACTION



8.0 HUB PIDS

8.1 Hub Function Controller (UDC0)

The Hub Function Controller (UDC0) is enabled by default, thus reported as a non-removable device.

The Hub Function Controller exposes different USB interfaces depending on the state of the configuration straps (CONFIG_STRAPx pins), enabling the features relevant to the selected PFx pins. Exposing a different PID for different configurations is required so that the correct USB client drivers are loaded.

The base PID is maintained as 0x4940. However, the last nibble is maintained to reflect the enabled features as shown in Table 159, with bit 0 indicating the presence of I2S HID, bit 1 indicating the presence of I2S Audio, bit 2 indicating the presence of CDC, and bit 3 indicating the presence of WinUSB.

TABLE 159: HUB FUNCTION CONTROLLER (UDC0) PIDS

WinUSB	CDC	I2S Audio	I2S HID	UDC0 Device Configuration	PID
No	No	No	No	No interface present, will not enumerate	NA
No	No	No	Yes	Invalid	NA
No	No	Yes	No	I2S Audio	4942h
No	No	Yes	Yes	I2S Audio, I2S HID	4943h
No	Yes	No	No	CDC Data, CDC Control	4944h
No	Yes	No	Yes	Invalid	NA
No	Yes	Yes	No	CDC Data, CDC Control, I2S Audio	4946h
No	Yes	Yes	Yes	CDC Data, CDC Control, I2S Audio, I2S HID	4947h
Yes	No	No	No	WinUSB	4940h
Yes	No	No	Yes	Invalid	NA
Yes	No	Yes	No	WinUSB, I2S Audio	494Ah
Yes	No	Yes	Yes	WinUSB, I2S Audio, I2S HID	494Bh
Yes	Yes	No	No	WinUSB, CDC Data, CDC Control	494Ch
Yes	Yes	No	Yes	Invalid	NA
Yes	Yes	Yes	No	WinUSB, CDC Data, CDC Control, I2S Audio	494Eh
Yes	Yes	Yes	Yes	WinUSB, CDC Data, CDC Control, I2S Audio, I2S HID	494Fh

8.2 Hub PID Selection

Table 160 shows the primary hub, secondary hub, UDC1, and UDC2 PIDs based on part number.

TABLE 160: PID SELECTION OPTIONS

Device	Package	Primary HUB PID	Secondary Hub PID	UDC1 PID (HU Side)	UDC2 PID (Phone Side)
USB4712	QFN48	4712h	NA	NA	NA
USB4912	QFN48	4912h	NA	4910h	4920h
USB4715	QFN48	4715h	NA	NA	NA
USB4914	QFN48	4914h	NA	4910h	4920h
USB4916	QFN64	4916h	NA	4910h	4920h
USB4925	QFN48	4925h	4931h	NA	NA
USB4927	QFN64	4927h	4931h	NA	NA

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002651C (12-12-24)	Table 82,Table 84, Table 86, Table 88, Table 90, Table 92, and Table 94	Changed Bits 7:6 to 7:3 (Reserved) Edited notes on the HS_BOOST bit
	Table 95	Added Bits 7:6 (USB2_HS_DISC_TUNE[1:0]).
DS00002651B (10-26-18)	Configuration of Microchip USB47xx/USB49xx	Changed the document title from “Configuration of USB491x/USB492x/USB4715” to “Configuration of Microchip USB47xx/USB49xx”
	Author	Added “Mick Davis” as author
	Section 1.0, "Introduction"	Changed “USB491x/USB492x/USB4715” to “USB47xx and USB49xx.
	Section 1.2, "References"	Added “*USB4712 Data Sheet*” and “*USB4715 Data Sheet”* to the list of references
	Table 3	Added information on USB4712 and USB4912 to the table
	Table 32	Added “USB4912 = 12h” and “USB4712 = 12h” to the description section. Changed “USB4715” to “USB47xx”
	Section 5.0, "OTP Configuration"	Changed “USB4715” to “USB47xx”
	Table 160	Added specifications for USB4912 and USB4712 to the table
DS00002651A (03-14-18)	Initial release	

NOTES:

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ISBN: 979-8-3371-0290-0

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