



Designing with the LAN9118 - Getting Started

1 Overview

This application note contains guidelines for the successful implementation of the LAN9118. It contains good general design practices as well as specific requirements of the LAN9118. It contains a list of product features, device and system block diagrams, circuit design requirements, clock requirements, magnetic selection, FAQs, and a sample layout and a reference design.

1.1 Reference Documents

The following documents are referred to in this application note:

1. SMSC LAN9118 Datasheet
2. SMSC LAN9118 Reference Design Schematic
3. SMSC Application Note AN8.13 - "Suggested Magnetics"
4. SMSC Application Note AN10.7 - "Parallel Crystal Circuit Input Voltage Control"

Please note that it is important to always refer to the SMSC LAN9118 Datasheet and the LAN9118 Reference Design Schematic for complete and current information regarding LAN9118 designs. Additionally, the circuit examples shown in this document are for illustrative purposes only. Please reference the LAN9118 Reference Design Schematic when implementing actual circuits in your design.

Please visit SMSC's website at <http://www.smSC.com/> for the latest updated documentation.

Please Note: Prior to the release of the LAN9118 Datasheet, the LAN9118 Advanced Technical Information document may be used in its place.

1.2 Product Description and Features

The LAN9118 is a full-featured, integrated 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and low cost are required. The LAN9118 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant.

LAN9118 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit and 32-bit microprocessors and microcontrollers. LAN9118 includes large transmit and receive data FIFO's with a high-speed host bus interface to accommodate high bandwidth, high latency applications. In addition, the LAN9118 memory buffer architecture allows the most efficient use of memory resources by optimizing packet granularity.

1.2.1 Product Features

- Integrated Ethernet controller
 - Fully compliant with IEEE 802.3/802.3u standards
 - Integrated Ethernet MAC and PHY
 - 10BASE-T and 100BASE-TX support
 - Full- and Half-duplex support

- Full-duplex flow control
- Backpressure for half-duplex flow control
- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Automatic payload padding and pad removal
- Loop-back modes
- Flexible address filtering modes
 - One 48-bit perfect address
 - 64 hash-filtered multicast addresses
 - Pass all multicast
 - Promiscuous mode
 - Inverse filtering
 - Pass all incoming with status report
 - Disable reception of broadcast packets
- Integrated Ethernet PHY
 - Auto-negotiation
 - Automatic polarity correction
- High-Performance host bus interface
 - Simple, SRAM-like interface
 - 32/16-bit data bus
 - Large, 16Kbyte FIFO memory that can be allocated to RX or TX functions
 - One configurable host interrupt
- Comprehensive power management features
 - Numerous power management modes
 - Wake on LAN
 - Magic packet wakeup
 - Wakeup indicator event signal
 - Link Status Change
- Miscellaneous features
 - Low profile 100-pin TQFP package
 - Single 3.3V power supply with 5V tolerant I/O
 - Integral 1.8V regulator
 - General Purpose Timer
 - Support for optional EEPROM
 - Support for 3 status LEDs multiplexed with Programmable GPIO signals

1.3 Device Level Block Diagram

This section provides an overview of each of these functional blocks. Please refer to the LAN9118 Datasheet document for more details.

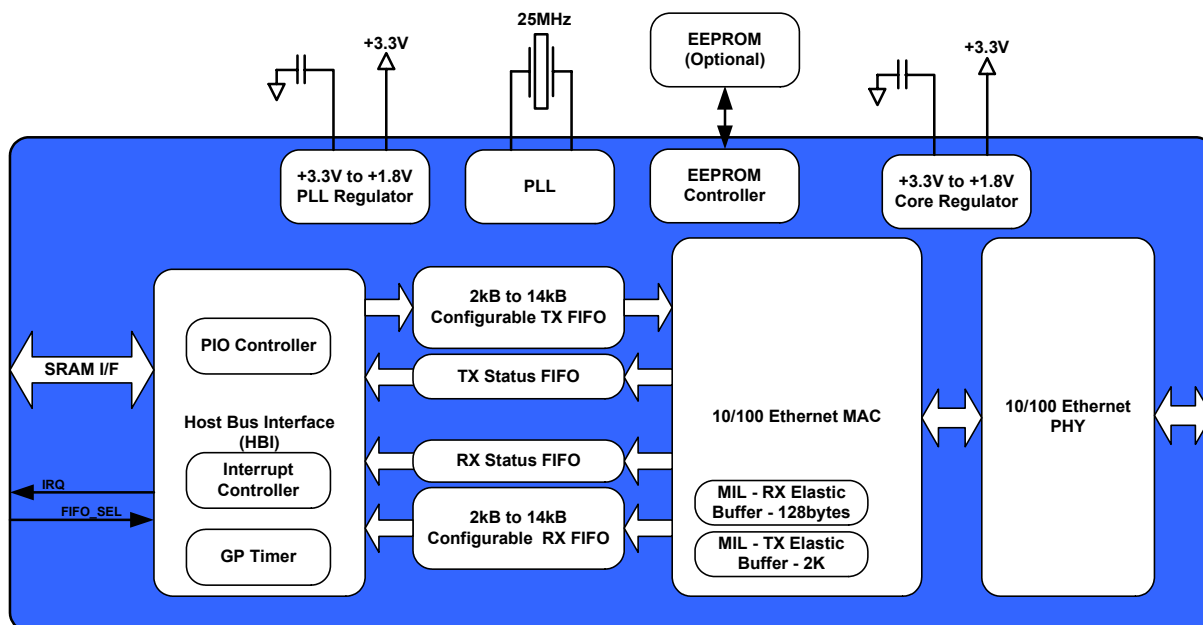


Figure 1.1 LAN9118 Internal Block Diagram

1.4 System Level Block Diagram

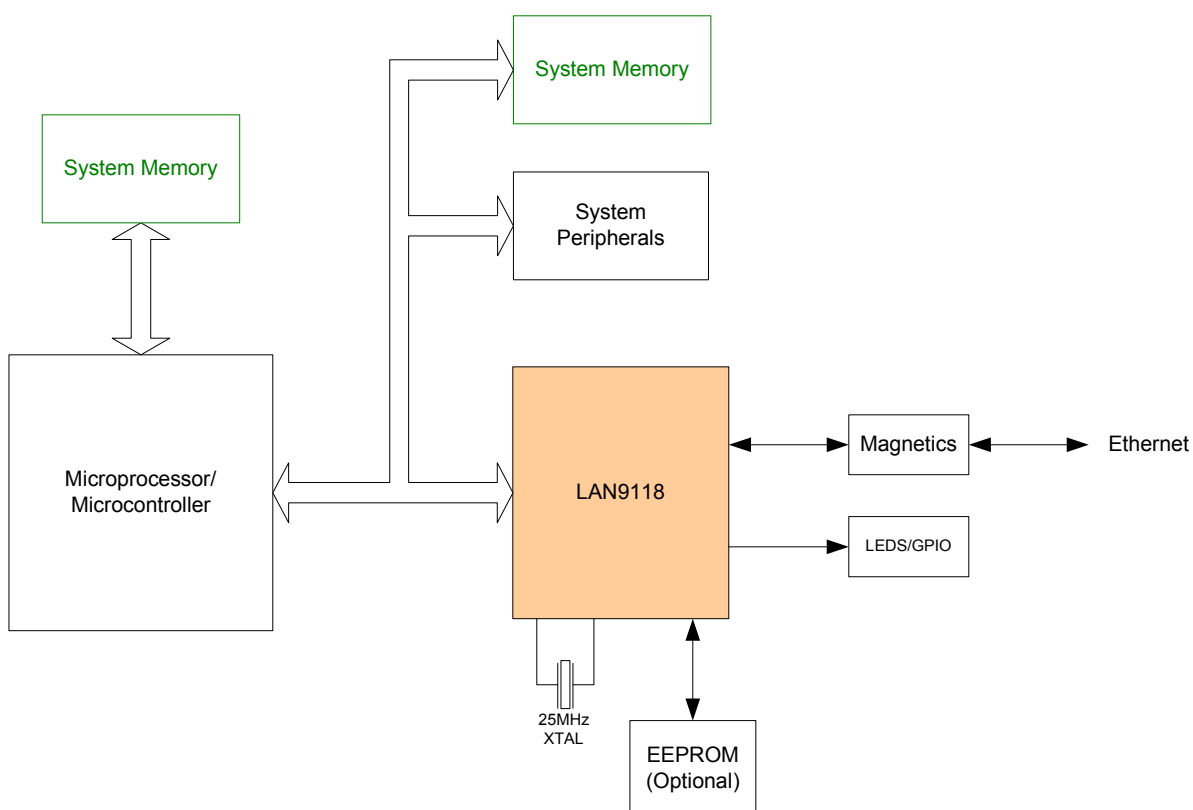


Figure 1.2 LAN9118 System Level Block Diagram

1.5 Compatible Bus Interfaces

The SMSC LAN9118 Integrated 10/100 MAC/PHY Controller is a peripheral device that converts data from a host controller into Ethernet packets, and vice-versa. The LAN9118 has been designed to operate efficiently in, but not necessarily limited to, an embedded environment.

The LAN9118 has been designed to be a platform-independent, general-purpose device. The LAN9118 features a simple, SRAM-like bus, which can easily be interfaced to any embedded processor, microcontroller or SOC. Data transfer to and from the LAN9118 can be accomplished with simple programmed I/O transactions, or using a DMA controller.

SMSC has validated the LAN9118 with a number of microcontrollers that were selected for their popularity among a target customer base or because they represented current technology and industry trends.

The LAN9118 host bus interface supports both 32-bit and 16-bit modes of operation. In 16-bit mode, the bus can be programmed for either Big-Endian or Little-Endian byte ordering. The LAN9118 host bus interface supports three basic types of bus cycles: programmed I/O, burst-read, and direct-access. In all three modes, the LAN9118 requires a separately decoded chip-select signal (nCS), with software programmable wait-states. The LAN9118 does not provide an asynchronous ready signal; all transactions must be timed using processor-generated wait states. The three modes are further described in the paragraphs and figures immediately below.

1.5.0.1 PIO Read and Write Cycles

PIO Read cycles (refer to Figure 1.3, "Simplified PIO Read Timing") are initiated with the assertion of chip select (nCS), address (A[7:1]) and the read (nRD) signals. Since the LAN9118 does not generate a "ready" signal, the de-assertion of these signals must be controlled by programming wait-states associated with the chip-select signal inside the processor.



Figure 1.3 Simplified PIO Read Timing

PIO write cycles (refer to Figure 1.4, "Simplified PIO Write Timing") are initiated with the assertion of chip select (nCS), address (A[7:1]), data (D[31:0]) and the read (nWR) signals. Since the LAN9118 does not generate a "ready" signal, the de-assertion of these signals must be controlled by programming wait-states associated with the chip-select signal inside the processor.



Figure 1.4 Simplified PIO Write Timing

1.5.0.2 Burst Read Mode

Many processors and DMA controllers have the capability to burst entire cache-lines using a single operation to improve performance. The LAN9118 supports this capability by allowing burst read cycles of up to eight, 32-bit D-words or sixteen, 16-bit words. In this mode the nRD and nCS signals are held low and the address is toggled. New data is presented after each new address. Refer to Figure 1.5, "Simplified Burst Read Timing".



Figure 1.5 Simplified Burst Read Timing

1.5.0.3 FIFO Direct-Access Mode

The LAN9118 provides a third mode of operation for host processors that increment the upper address lines during DMA operations. In this case, in order to prevent the address from overflowing the LAN9118 register map, the upper address bits, A[7-3] are ignored, and replaced by a separate FIFO_SEL input. When this signal is asserted high, along with nCS and nRD, data is bursted directly from receive FIFO. Each time the A[2:1] pins are toggled, the LAN9118 presents a new 32-bit or 16-bit data value on the bus (note that this mode works with either 16-bit or 32-bit modes of operation). Similarly, if nCS and nWR are asserted, data is bursted directly to the transmit FIFO. A simplified timing diagram for a Direct FIFO Access burst read is provided in Figure 1.6, "Burst Read Operation Using Direct FIFO Access".



Figure 1.6 Burst Read Operation Using Direct FIFO Access

The timing diagrams in this section are simplified versions of the LAN9118 timing. Please refer to the LAN9118 Datasheet for detailed timing diagrams.

1.6 Power and Ground Requirements

1.6.1 LAN9118 Power Requirements

The LAN9118 requires a +3.3V power source, which may be obtained from any existing on-board +3.3V source, or, if none is available, by incorporating an external regulator, - such as the Linear Technologies LT1086 +5V-input to +3.3V-output fixed-voltage regulator.

The +3.3V voltage level is supplied to the LAN9118 core via the pins listed in [Table 1.1, "LAN9118 Power Pins"](#).

Table 1.1 LAN9118 Power Pins

SIGNAL NAME	LAN9118 PIN NO'S.
VDD_IO	20, 28, 35, 42, 48, 55, 61, 97
VDD_A	81, 85, 89, 91
VREG_3.3	2

It is recommended that VDD_A (analog) on the LAN9118 be supplied +3.3V from the board's power plane via a ferrite bead (see Figure 1.7, "Power Pin Connections – LAN9118 to +3.3V").

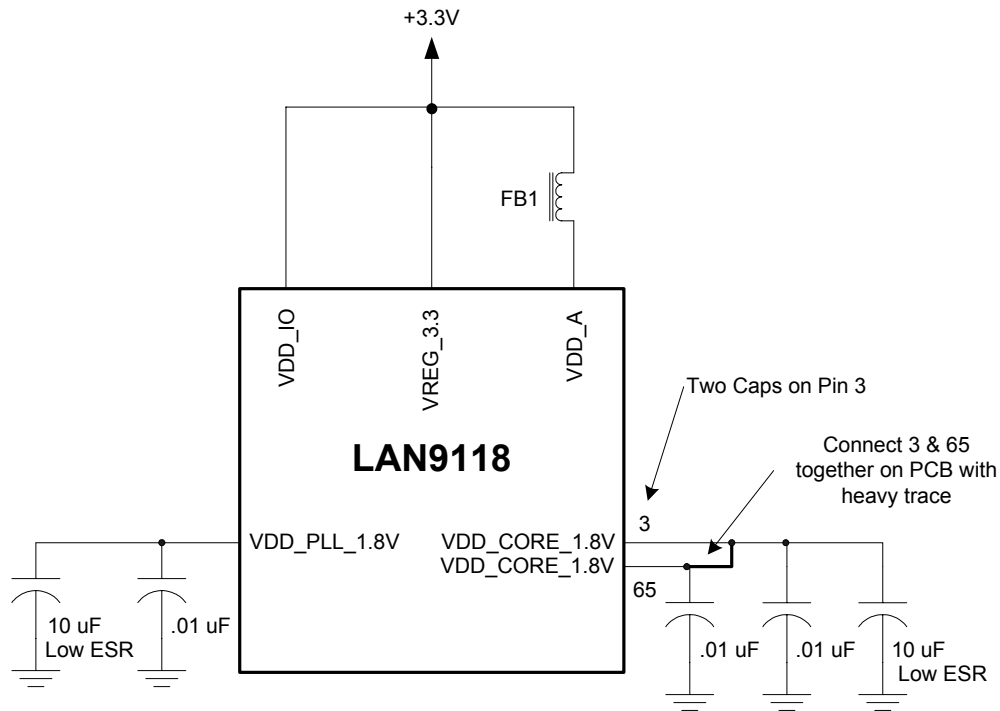


Figure 1.7 Power Pin Connections – LAN9118 to +3.3V

1.6.2 LAN9118 Ground Requirements

The LAN9118 requires that all the ground connections below be connected to one, solid, contiguous ground plane. This requirement must be considered design critical.

The Ground reference to the LAN9118 is furnished via the pins listed in [Table 1.2, "LAN9118 Ground Pins"](#).

Table 1.2 LAN9118 Ground Pins

SIGNAL NAME	LAN9118 PIN NO'S.
GND_IO	19, 27, 34, 41, 47, 54, 60, 96
VSSA	77, 80, 86, 88, 90
GND_CORE	1, 66
VSS_PLL	4
VSS_REF	11

1.6.3 LAN9118 Current Measurements

Current numbers are preliminary and were obtained with DUT running in normal operating mode. For currents in different operating modes and power management states, refer to the LAN9118 datasheet.

Table 1.3 LAN9118 Current Figures

SIGNAL NAME	LAN9118 CURRENT
VDD_IO	20 mA
VDD_A	40 mA
VREG_3.3	70 mA
VREF	10 mA

1.6.4 LAN9118 Case Temperature

The LAN9118 is expected to operate at about a 10 degree Celsius rise above the board ambient on the device case during normal active operation (without power management turning off any clocks.) This corresponds to about a ¼ watt power dissipation for the LAN9118.

1.7 Cable Interface

The requirements for the cable interface, including the magnetics and RJ45 connector interfaces, are outlined in the sections below.

1.7.1 Magnetics

The LAN9118 Reference Design Schematic currently uses the Bel S558-5999-46 magnetics module. Please refer to SMSC Application Note AN8.13 - "Suggested Magnetics" for a current listing of approved magnetics.

1.7.2 Transmit and Receive Terminations

1.7.2.1 Transmit Terminations

The LAN9118 transmit signals (TPO+, TPO-) should be pulled to +3.3V (VDD_A) supplied from the board's power plane via a ferrite bead and termination resistors R_{Term} (see Figure 1.8, "Tx to Magnetics Interface"). Power is supplied to the transmitter via the 10-ohm resistor and the transformer center tap.

The TPO+ & the TPO- traces must be routed as paired differential traces with 100-ohm characteristic impedance. Termination components R3 & R4 should be placed as close to the magnetics module as possible. Locate R5, which feeds the transformer center tap and then back into the LAN9118, as close to the magnetics as possible.

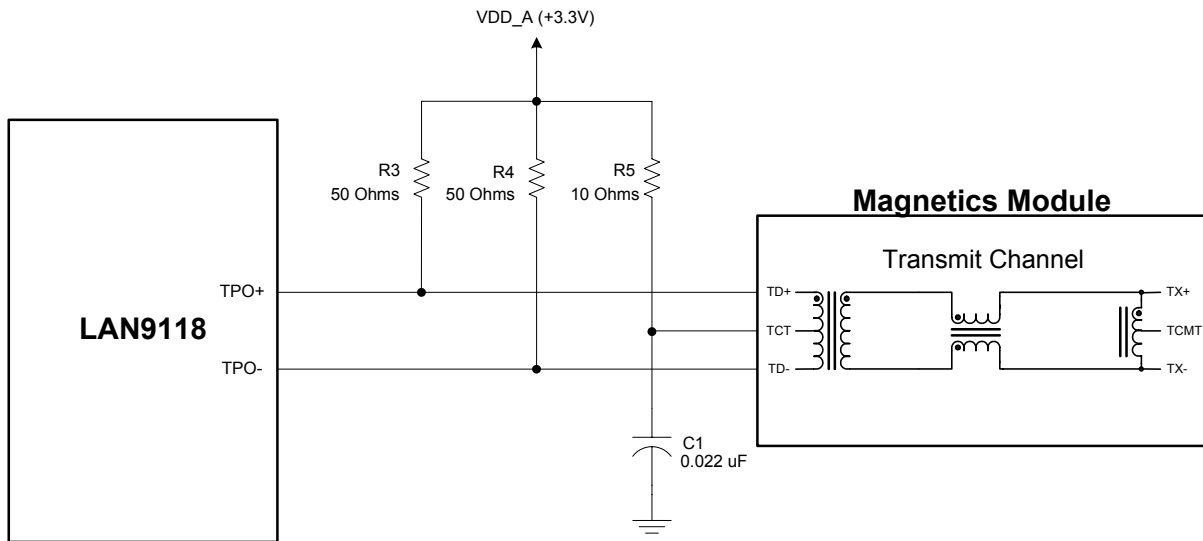


Figure 1.8 Tx to Magnetics Interface

1.7.2.2 Receive Terminations

Each of the LAN9118 receive signals (TPI+, TPI-) should be AC-coupled to the magnetics module's receive interface via a capacitor. Additionally, TPI+ and TPI- signals should be terminated through a resistor via a capacitor connected to ground (see Figure 1.9, "Rx to Magnetics Interface"). Please refer to the LAN9118 Reference Schematic for recommended values.

The TPI+ & the TPI- traces must be routed as paired differential traces with 100-ohm characteristic impedance. Terminations R1, R2 & C3 must be placed as close to the LAN9118 as possible. AC coupling components C1 & C2 must be placed as close to the LAN9118 as possible. These capacitors play an integral role in the devices ability to compensate properly for baseline wander.

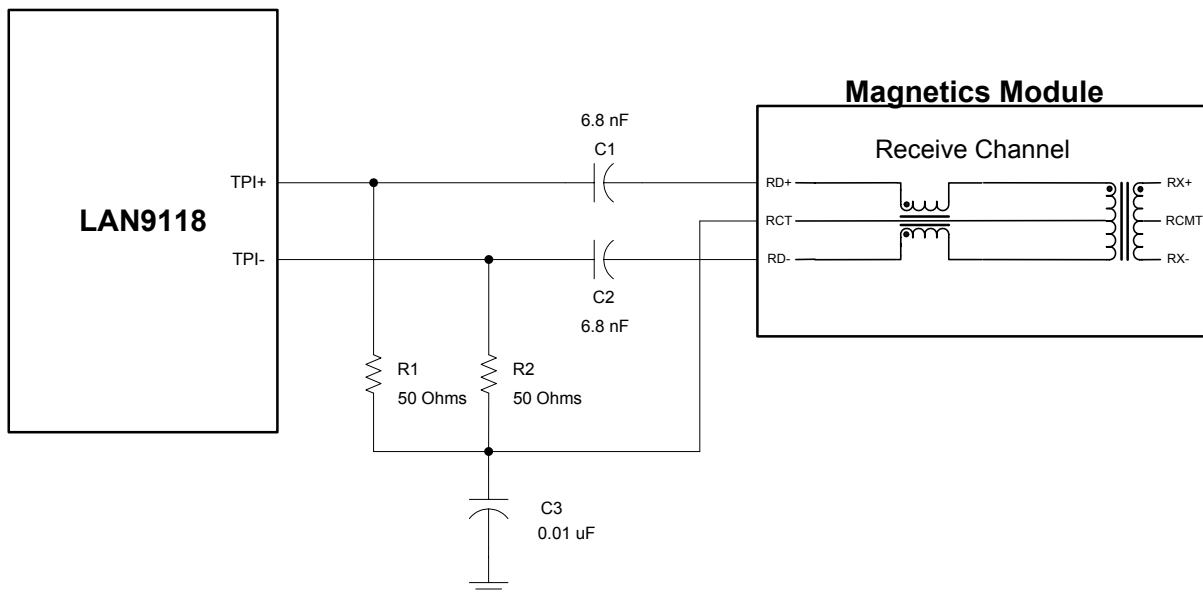


Figure 1.9 Rx to Magnetics Interface

1.8 Clock Circuit

The LAN9118 can accept either a 25MHz crystal (preferred) or a 25 MHz clock oscillator (± 50 PPM) input. The LAN9118 shares the 25MHz clock oscillator input (CLKIN) with the crystal input XTAL1/CLKIN (pin 6).

It is recommended that a crystal utilizing matching parallel load capacitors be used for the LAN9118 crystal input/output signals (XTAL1, XTAL2). See [Table 1.4, "LAN9118 Crystal Specifications"](#).

Table 1.4 LAN9118 Crystal Specifications

LAN9118 CRYSTAL SPECIFICATIONS	
Frequency Tolerance @ 25° C	± 50 PPM
Frequency Stability Over Temp	± 50 PPM
Operating Temp Range	0° C to 70° C
Shunt Capacitance	7.0 pF
Load Capacitance	10 pF ~ Series
Drive Level	0.5 mW

Table 1.5 LAN9118 Recommended Crystals

LAN9118 RECOMMENDED CRYSTALS	
Fox Electronics	FOX5/250F-20

Additionally, SMSC recommends a series resistor for the crystal circuit. Further details are provided in SMSC Application Note AN10.7 - "Parallel Crystal Circuit Input Voltage Control" and in the LAN9118 Reference Schematic.

1.9 EEPROM Considerations

A serial EEPROM interface is included in the LAN9118. The serial EEPROM is optional and can be programmed with the LAN9118 MAC address. The LAN9118 can be configured to load the MAC address automatically after power-on.

Table 1.6 LAN9118 Recommended EEPROMs

LAN9118 RECOMMENDED EEPROMS	
Microchip	93LC46A-SN
ISSI	IS93C46
SGS-Thomson	ST93C46A
SGS-Thomson	ST93C46T

General purpose I/O and power-up configuration straps share pins with the EEPROM. The EEPROM data pins are connected by a resistor to create a bi-directional serial data bus to reduce LAN9118 I/O pin count. The value of the feedback resistor is selected to overdrive the strapping options when data is being read from the EEPROM. Use the recommended resistor values and EEPROMs to ensure performance. Refer to the Reference Schematic in section 15. of this document for details.

1.10 LEDs

The LAN9118 provides three LED output signals, which share pins with general purpose I/O pins. These signals are:

- Speed LED
- Link / Activity LED
- Full-Duplex LED

1.10.1 GPIO Functions

General Purpose I/O Data All three general-purpose signals are fully programmable as either push-pull output, open-drain output, input, or bi-directional by writing the GPIO_CFG configuration register in the CSR's. They are also multiplexed as GP LED connections. GPIO signals are Schmitt-triggered inputs. When configured as LED outputs these signals are open-drain.

1.10.2 LED Speed Indicator

nLED1 / Speed Indicator This signal is driven low (LED on) when the operating speed is 100Mbps, or during auto-negotiation. This signal is driven high during 10Mbps operation, or during line isolation. nLED1 is pin 98 on the LAN9118.

1.10.3 LED Link & Activity Indicator

nLED2 / Link & Activity Indicator This signal is driven low (LED on) when the LAN9118 detects a valid link. This signal is pulsed high (LED off) for 80mS whenever transmit or receive activity is detected. This signal is then driven low again for a minimum of 80mS, after which time it will repeat the process if TX or RX activity is detected. Effectively, LED2 is activated solid for a link. When transmit or receive activity is sensed LED2 will flash as an activity indicator. nLED2 is pin 99 on the LAN9118.

1.10.4 LED Full Duplex Indicator

nLED3 / Full Duplex Indicator This signal is driven low (LED on) when the link is operating in full-duplex mode. nLED3 is pin 100 on the LAN9118.

1.11 General Requirements

The topics described in the following sub-sections below require additional attention by the systems designer when incorporating the LAN9118.

1.11.1 Pin Specific Requirements

The following pins of the LAN9118 have very specific design requirements. Always refer to the LAN9118 Datasheet and LAN9118 Reference Schematic when implementing a design using the LAN9118.

1.11.1.1 ATEST

This pin serves as a voltage reference input to the LAN9118. This pin must always be at the same potential as the VDD_REF pin. ATEST on the LAN9118 is pin 9.

1.11.1.2 VDD_REF

This pin serves as a voltage reference input to the LAN9118. This pin must always be at the same potential as the VDD_IO power pins. VDD_REF on the LAN9118 is pin 8.



1.11.1.3 EXRES1

This pin is a precision analog current reference input for the 10/100 PHY embedded in the LAN9118. This pin requires a 12.4K ohm, 1.0% resistor terminated to ground. Other values and tolerances are not recommended. EXRES1 on the LAN9118 is pin 87.

1.11.1.4 RBIAS

This pin is a high precision analog current reference input for the PLL circuit embedded in the LAN9118. This pin requires a 12.0K ohm, 0.1% resistor terminated to ground. Other values and tolerances are not recommended. RBIAS on the LAN9118 is pin 10.

1.11.1.5 TESTBUSA

This pin on the LAN9118 is an analog test output from the LAN9118. This pin is used for factory test purposes only. This pin should always be left as a no-connect. TESTBUSA on the LAN9118 is pin 84.

1.11.1.6 VDD_CORE_1.8V

These two pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 uF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 3 requires a bulk capacitor placed as close as possible to pin 3. The capacitor must have a value of at least 10 uF, and have an ESR of no more than 2 Ω . SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended. VDD_CORE_1.8V on the LAN9118 are pins 3 & 65.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD_CORE_1.8V to VDD_PLL_1.8V.

1.11.1.7 VDD_PLL_1.8V

This pin is used to provide an external supply decoupling capacitor to the internal +1.8V PLL regulator. A 0.01 uF decoupling capacitor must be attached to this pin. The capacitor should be located as close as possible to the VDD_PLL_1.8V pin, and must be attached without using vias. In addition, a bulk capacitor must also be attached to this pin. The bulk capacitor must have a value of at least 10uF, and must have a very low ESR (equivalent series resistance) of less than 2 Ω . SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended. VDD_PLL_1.8V is located on pin 7.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD_PLL_1.8V to VDD_CORE_1.8V.

1.11.1.8 EEPROM Data / 32/16 Strap Option

EEPROM Data: This bi-directional pin can be connected to a serial EEPROM DIO. This is optional.

General Purpose Output 3: This pin can also function as a general purpose output, or it can be configured to monitor the TX_EN or TX_CLK signals on the internal MII port. When configured as a GPO signal, or as a TX_EN/TX_CLK monitor, the EECS pin is deasserted so as to never unintentionally access the serial EEPROM. This signal cannot function as a general-purpose input.

Data Bus Width Select: This signal also functions as a configuration input on power-up and is used to select the host bus data width. Upon deassertion of reset, the value of the input is latched. When high, a 32-bit data bus is utilized. When low, a 16-bit interface is utilized.

1.11.1.9 10/100 Strap Option

This signal functions as a configuration input on power-up and is used to select the default Ethernet settings. Upon deassertion of reset, the value of the input is latched. As a configuration input this signal functions as follows:

Table 1.7 LAN9118 Speed Selections

SPEED_SEL	DEFAULT ETHERNET SETTINGS		
	SPEED	DUPLEX	AUTO NEG.
0	10Mbps	Half-Duplex	Disabled
1	100Mbps	Half-Duplex	Enabled

1.11.1.10 Reset

This pin on the LAN9118 is an active-low reset input. It resets all logic and registers within the LAN9118. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9118 will rely on its internal power-on reset circuitry.

1.11.1.11 No-Connects

There are 3 no-connect pins on the LAN9118. Nothing should be connected to these pins; they do not require external pull-ups or pull-downs. The no-connections on the LAN9118 are pins 75, 73 & 71.

1.12 Frequently Asked Questions

1.12.1 Hardware Related Questions

1. Can I change the EXRES1 or RBIAS resistors?

Answer: No, you cannot change the value of these resistors. The values of these resistors affect the bias currents in ALL analog blocks in the PHY, the amplitudes of the transmitter, bias currents to the PLLs, etc. It is very important that the value be exactly 12.4K, 1.0% for EXRES1 and 12.0K, 0.1% for RBIAS.

2. Can I change the termination components in the Ethernet front end?

Answer: No, all the components and voltage reference levels located between the magnetics and the LAN9118 are considered "By Design". They are correct as put forth in the Reference Schematic. All validation testing accomplished by SMSC and all UNH 802.3 Compliance testing has been accomplished with these values. Any deviation from any of the recommended values may invalidate that conformance testing.

3. Since VDD_PLL and VDD_CORE are both 1.8V, can I connect them together?

Answer: No. These power supplies are outputs from two different internal regulators. Connecting them together will likely damage the LAN9118.

4. Can I use the LAN9118's internal 1.8V power supplies to supply power to other devices on my board?

Answer: No. These supplies are for internal logic only.

5. Can the LAN9118's internal pull-up and pull-down resistors be used to pull-up logic external to the LAN9118?

Answer: No. The internal pull-up and pull-down resistors are to prevent unconnected pins from floating. These will not function as reliable pull-ups and pull-downs for external signals.

6. Do I need to reset the LAN9118 after power-up?

Answer: No. Although it can be done, it's not a requirement. The LAN9118 has an internal power-on reset circuit. The device is held in reset for about 23ms after power-up.



7. How do I know if the LAN9118 is ready to operate after power-up or reset, or after it wakes from a sleep state?

Answer: A Device Ready indicator bit ("READY") is provided in the PMT_CTRL register. When this bit is low, the LAN9118 is not ready for operation. A host processor must check this bit after reset, after power-up, or after waking from a sleep state to verify that the LAN9118 is ready for normal operation.

8. What package types is the LAN9118 available in?

Answer: The LAN9118 is available in leaded and lead-free 100-pin TQFP packages

9. I can't get my parts to solder down reliably. What's wrong?

Answer: Make sure the solder re-flow characteristics properly match the package type chosen.

10. I'm using a 16-bit bus. Can I tie D[31:16] to ground?

Answer: No. The LAN9118 has the proper terminations inside the device to properly terminate these signals if they are not required. Leave them as no-connects.

11. I'm using a 16-bit STMicro processor and I'm having trouble. What's wrong?

Answer: Be certain when designing with the STMicro families to shift the address bits up by one when connecting to the LAN9118.

12. Is the LAN9118 available for industrial temperature applications?

Answer: Currently the LAN9118 is available for commercial temperature applications (0-70C) only

1.12.2 Software Related Questions

1. What is the maximum throughput of the LAN9118?

Answer: Network throughput depends on a large number of factors. These include the speed and bus-width (16 or 32 bits) of the CPU, the speed and architecture of the system buses, the choice of operating system, as well as the traffic statistics, network protocols used and software application used. On the XScale reference platform, running Linux, using the Netperf performance measurement applications, traffic rates over 90 Mbps have been observed.

2. What are some tools used to benchmark LAN9118 network speed?

Answer: We use Netperf and SmartBits NicTest.

3. Can I re-use my existing LAN91C96, LAN91C111 drivers?

Answer: No. In order to maximize performance and efficiency, the LAN9118 has a completely different architecture and register structure than either the LAN91C111 or LAN91C96. As a result, drivers designed for the LAN91C111 or LAN91C96 will not run on the LAN9118. However, a large number of drivers for various operating systems and processors has already been developed by SMSC.

4. For which operating systems and CPUs does SMSC provide sample device drivers?

Answer: At the date of the writing of this document, SMSC has written device drivers for the following platforms:

- Linux on Intel XScale (PXA27x) & Renesas SH3
- Windows CE for Intel XScale (PXA27x) and Renesas SH3
- OS20 for STMicro STi5517

5. How do I find SMSC drivers?

Answer: Refer to the SMSC web site (<http://www.smsc.com>) for the latest list of supported drivers, as well as directions for gaining access to the source code for these drivers.

6. Does the LAN9118 support Power Management for CE/PalmOS/Linux?

Answer: Yes.

7. What support does SMSC provide for driver development?

Answer: Please contact your local SMSC FAE.

1.13 Qualifying Alternate Magnetics

Magnetics play a crucial role in Ethernet performance and meeting IEEE standards. SMSC performs extensive testing before qualifying any magnetic device; customers should expect to do the same.

As a strategy, SMSC recommends that all designs **first** be built with approved devices and tested to verify compliance **before** evaluation of alternatives is made. This strategy has the following advantages: it ensures that problems with the alternative magnetics do not affect the production schedule, it provides a back-up plan if the alternatives do not work, and it provides a stable basis for evaluating the alternative devices.

Qualifying alternate magnetics is a three-step process. First, the alternatives need to be identified. Next, the specifications need to be compared to those of the recommended devices. Finally, the devices need to be tested in the lab to ensure all requirements are met; this last step is an arduous process that requires some skill.

1.13.0.1 Identifying Alternate Magnetics

The first step is to narrow down the large number of potential magnetic vendors to a few good candidates, based on the design criteria. A critical factor is the available space. If there is ample space, the best choice is always to use a large footprint, discrete magnetic. If space is at an absolute premium, integrated magnetics with RJ45 connector may be considered. The reputation of the vendor and the quality of the components should be considered very strongly. Price should be considered last; however SMSC cautions against choosing vendors simply on the basis of price without consideration for quality.

One good practice is to choose the alternatives so that they all have the same footprint and electrical schematic. This ensures that choices can be interchanged seamlessly, and allows flexibility in the event that there are performance or supply issues with some of the sources

1.13.0.2 Comparing Magnetics

The next step is to compare the datasheets of the proposed alternatives to the datasheets of the magnetics recommended by SMSC, in order to ensure that the alternative will work properly with the LAN9118.

Considerations:

- Test certifications required for the product. For example, if FCC/CISPR certifications are required, plan to use a five-core type magnetic solution. If FCC/CISPR certifications are not required, a less expensive three- or four-core solution may be considered.
- Quality. Not all vendors provide the same levels of quality. Be especially cautious of low-price offerings.
- Specifications and performance, which are often inversely related to the price. Accepting magnetics with inferior specifications and performance may cause trouble later in the field.

1.13.0.3 Verifying Proper Operation of the New Magnetics

This is the most arduous part of the process, and is a major reason for **not** deviating from the magnetics recommended by SMSC. Determining the suitability of an alternative magnetic device requires repeating all of the tests performed by SMSC to qualify a recommended magnetic device. These tests include analyzing:

- Voltage levels
- Timing Requirements

- Return-Loss Characteristics
- Eye-Patterns for both 10BASE-T and 100BASE-TX

The University of New Hampshire (UNH) Ethernet Compliance website, and in particular the 100BASE-TX PMD and 10BASE-TX MAU Test Suites, can be consulted for a list of tests that need to be completed and specifications that need to be met. Many third parties, including UNH, offer verification services for a fee. Unless magnetic qualification is done on a routine basis, out-sourcing the verification process may be the most cost-effective and reliable approach.

1.14 Performance Graphs

The following graphs show the relative performance of the LAN9118 on an XScale platform using a Linux driver. The CPU clock was running at 390 MHz with the system clock running at 195 MHz. The memory clock was running at 97 MHz. The operating mode of the LAN9118 was set to DMA mode.

The test vehicle used was the SmartBits platform using the ICMP Throughput Test to obtain the following numbers. Each operating mode (10BASE-T, 100BASE-TX, Half & Full Duplex) was exercised. See below.

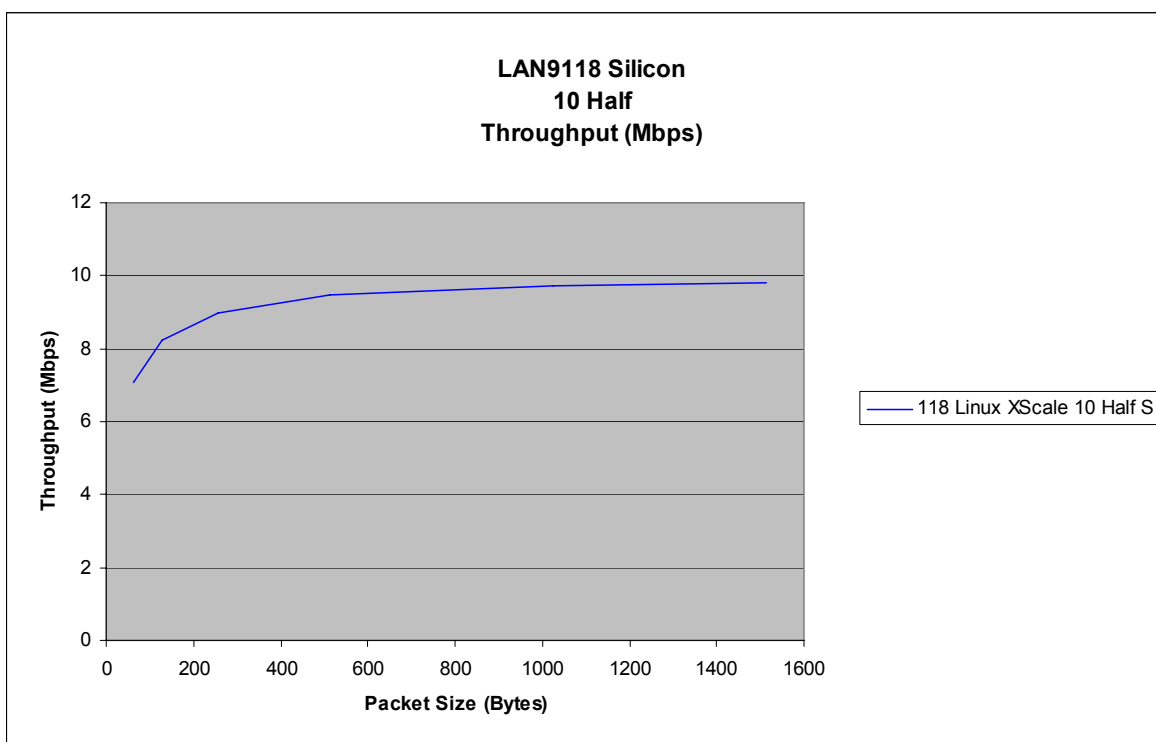


Figure 1.10 LAN9118 10M, Half Duplex

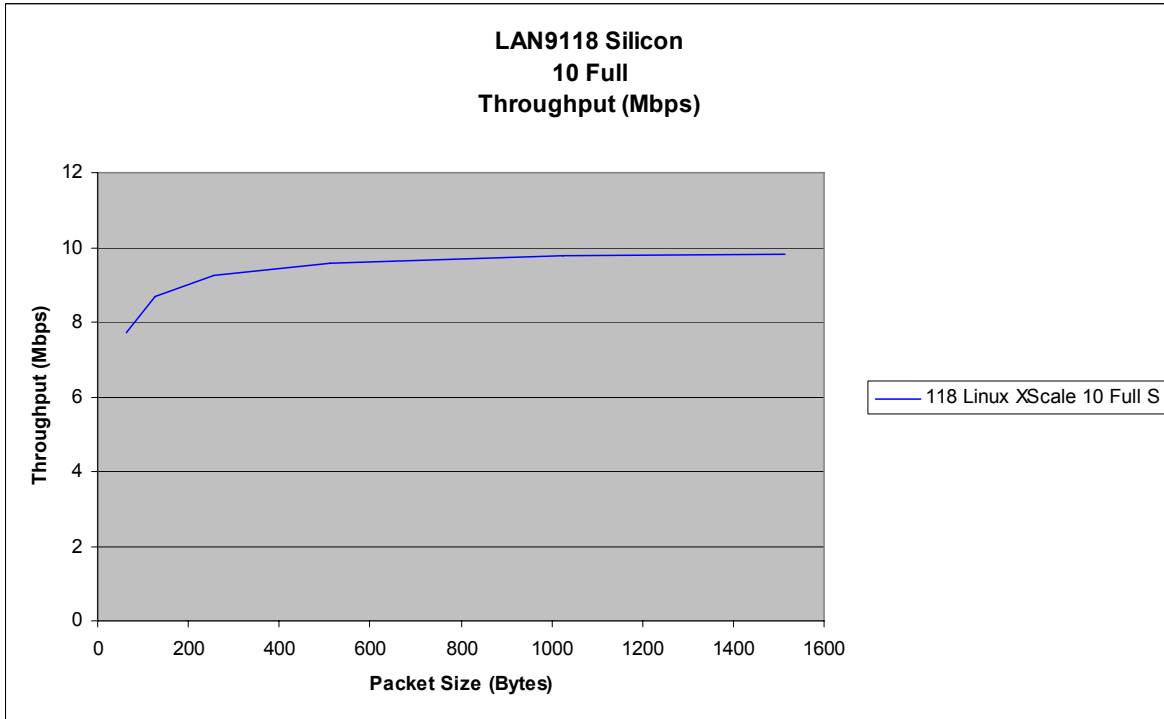


Figure 1.11 LAN9118 10M, Full Duplex

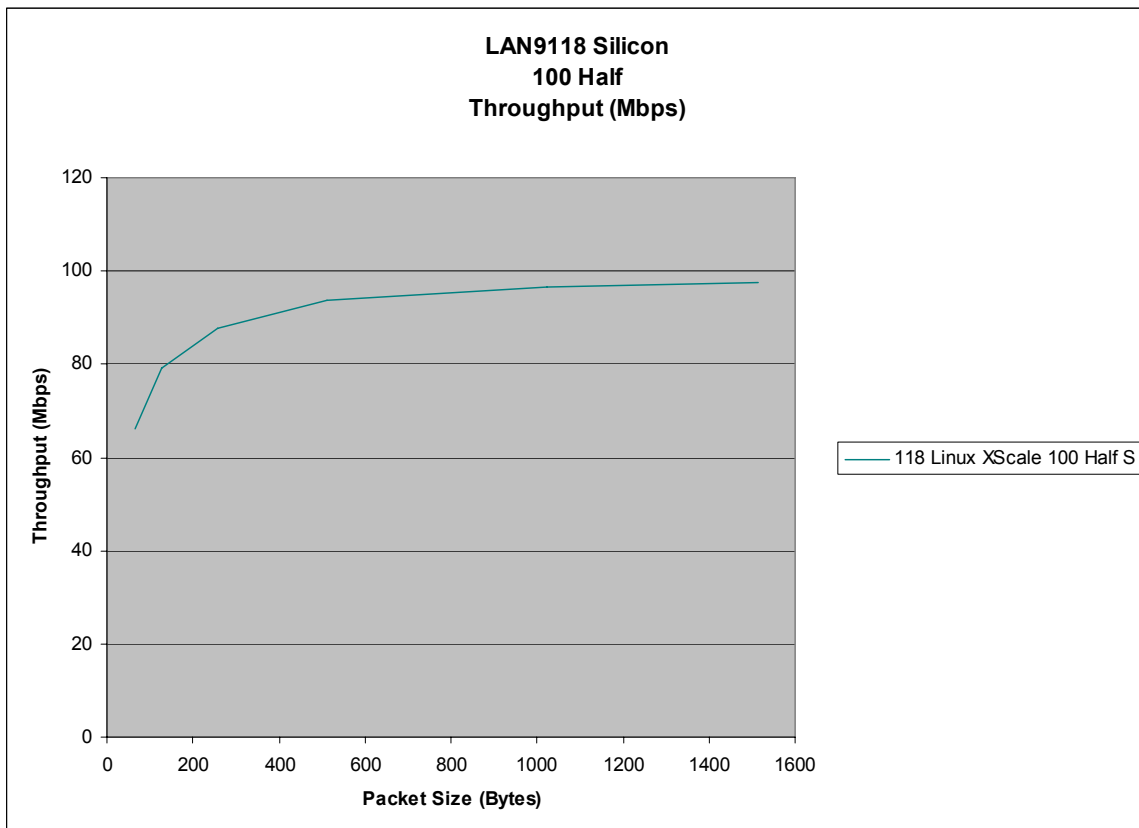


Figure 1.12 LAN9118 100M, Half Duplex

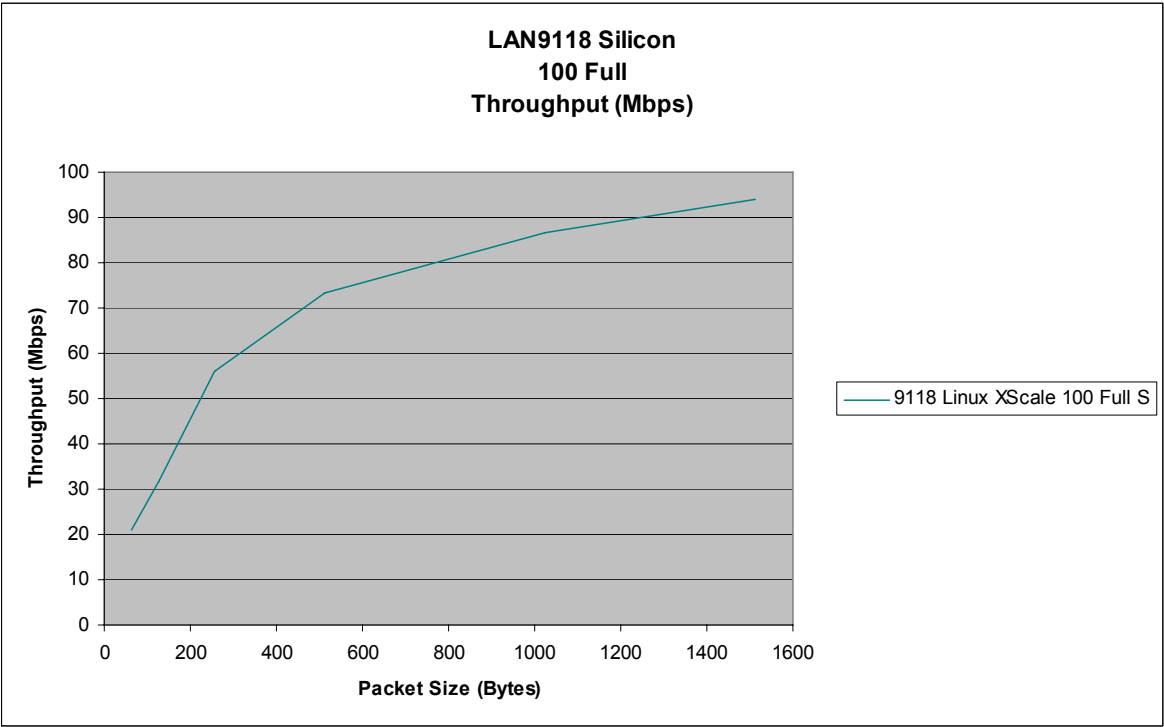
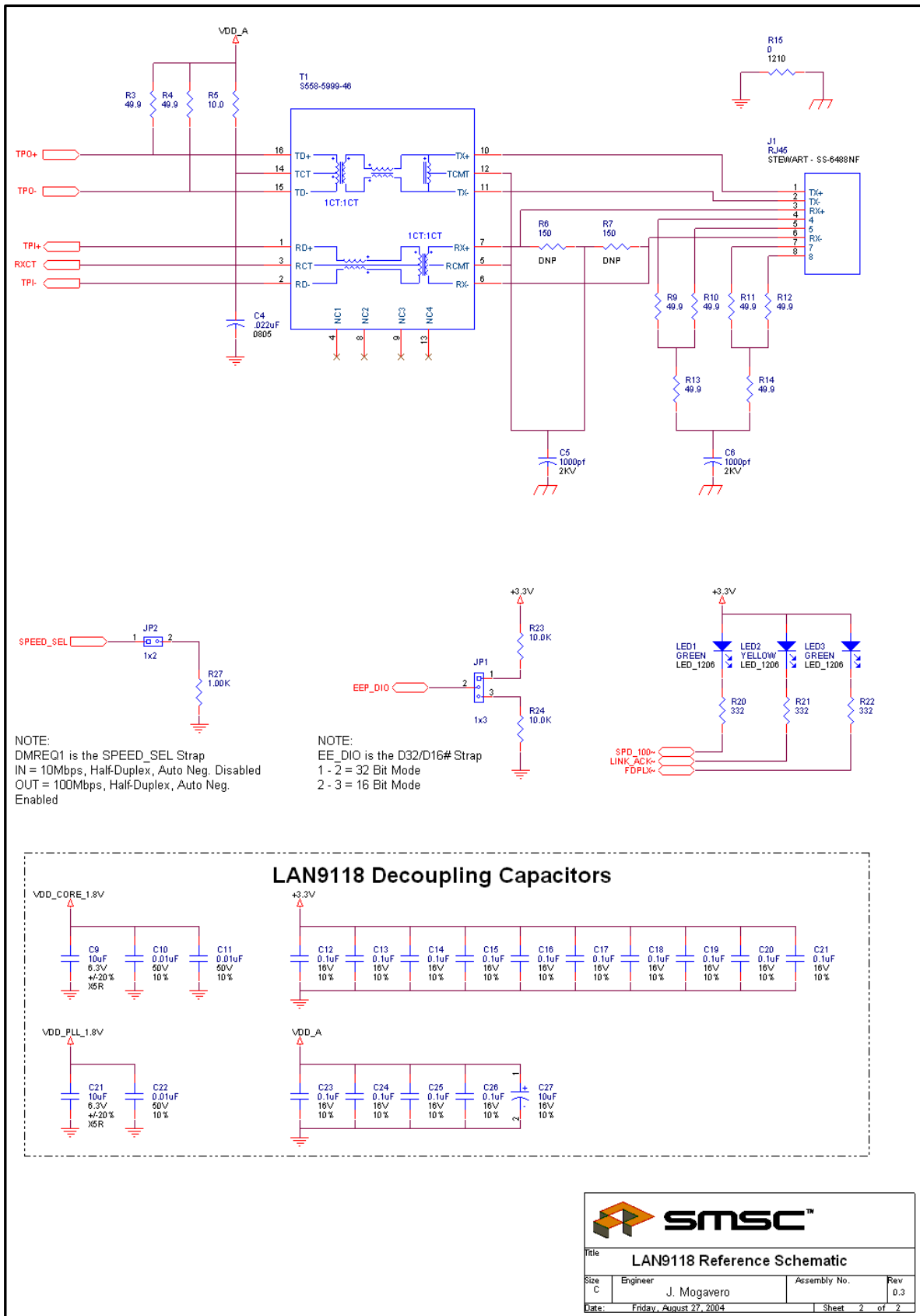


Figure 1.13 LAN9118 100M, Full Duplex



1.16 Reference Schematic BOM

Table 1.8 LAN9118 Reference Schematic Bill Of Materials

ITEM	QTY	DESIGNATOR	VALUE	FOOT PRINT	PART NUMBER
1	2	C1,C2	6.8nF	0805	KEMET - C0805C682K4RAC
2	1	C3	.01uF	0805	KEMET - C0805C103K5RAC
3	1	C4	.022uF	0805	KEMET - C0805C223K5RAC
4	2	C5,C6	1000pf 2KV	1808	AVX - 1808GC102ZA11A
5	2	C8,C7	30pf 50V	0805	KEMET - C0805C300K3RAC
6	2	C21,C9	10uF 6.3V	0805	ECJ - 2FB0J106M
7	3	C10,C11,C22	0.01uF 50V	0603	Kemet C0603C103K5RAC
8	15	C12,C13,C14,C15,C16,C17,	0.1uF 16V	0603	Kemet-C0603C104K4RAC
		C18,C19,C20,C21,C23,C24,			
		C25,C26,C28			
9	1	C27	10uF 16V	SMD_B	Kemet-T491B106K016AS
10	1	FB1	200ma/0.4DCR	0603	Murata-BLM11B121SD
11	1	JP1	1x3	Head1x3	Adam Tech PH1-03-U-A
12	1	JP2	1x2	Head1x2	Adam Tech PH1-2-U-A
13	1	J1	RJ45	RJ45_MTJ	STEWART - SS-6488NF
14	2	LED1,LED3	GREEN	LED_1206	Chicago Miniature - 7010X5
15	1	LED2	YELLOW	LED_1206	Chicago Miniature - 7010X7
16	10	R1,R2,R3,R4,R9,R10,R11,	49.9	0805	ROHM - MCR10EZHF49R9
		R12,R13,R14			
17	2	R5,R18	10.0	0805	ROHM - MCR10EZHF10R0
18	DNP	R7,R6	150	0805	ROHM - MCR10EZHF1500
19	1	R8	12.4K	0603	Rohm-MCR03EZHF1242
20	1	R15	0	1210	ROHM - MCR25JZHB000
21	1	R16	12.0K	0603	Yageo - 9T06031A1202BAHFT
22	1	R17	0	3PIN_0603	ROHM - MCR03EZHF000
23	DNP	R19	1M	0805	ROHM - MCR10EZHF1004
24	3	R20,R21,R22	332	0805	ROHM - MCR10EZHF3320
25	3	R25,R26,R27	1.00K	0603	ROHM - MCR03EZHF1001
26	1	R28	680	0805	ROHM - MCR10EZHF6800
27	2	R23, R24	10.0K	0805	ROHM - MCR10EZHF1002
28	2	TP1,TP2	Test Point-1x1	HEAD1X1	AdamTech - PH1-01-U-A

Table 1.8 LAN9118 Reference Schematic Bill Of Materials (continued)

ITEM	QTY	DESIGNATOR	VALUE	FOOT PRINT	PART NUMBER
29	1	T1	BEL - S558-5999-46	BEL - S558-5999-46	BEL - S558-5999-46
30	1	U1	LAN9118	TQFP100	LAN9118
31	1	U2	93LC46A	SOIC-8	Microchip - 93LC46A-SN
32	1	Y1	25 MHZ	HC49US	FOX - FOXS/250F-20

1.17 Sample Layout

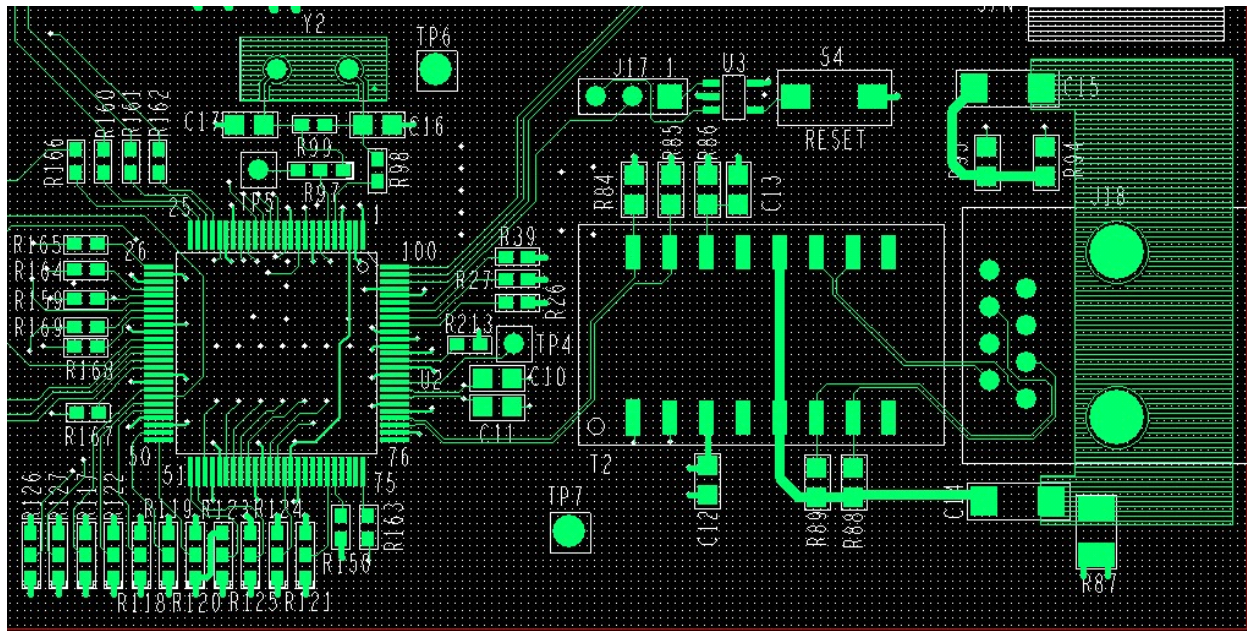


Figure 1.14 Layer 1 – Top Side Component



Figure 1.15 Layer 2 – Ground Plane

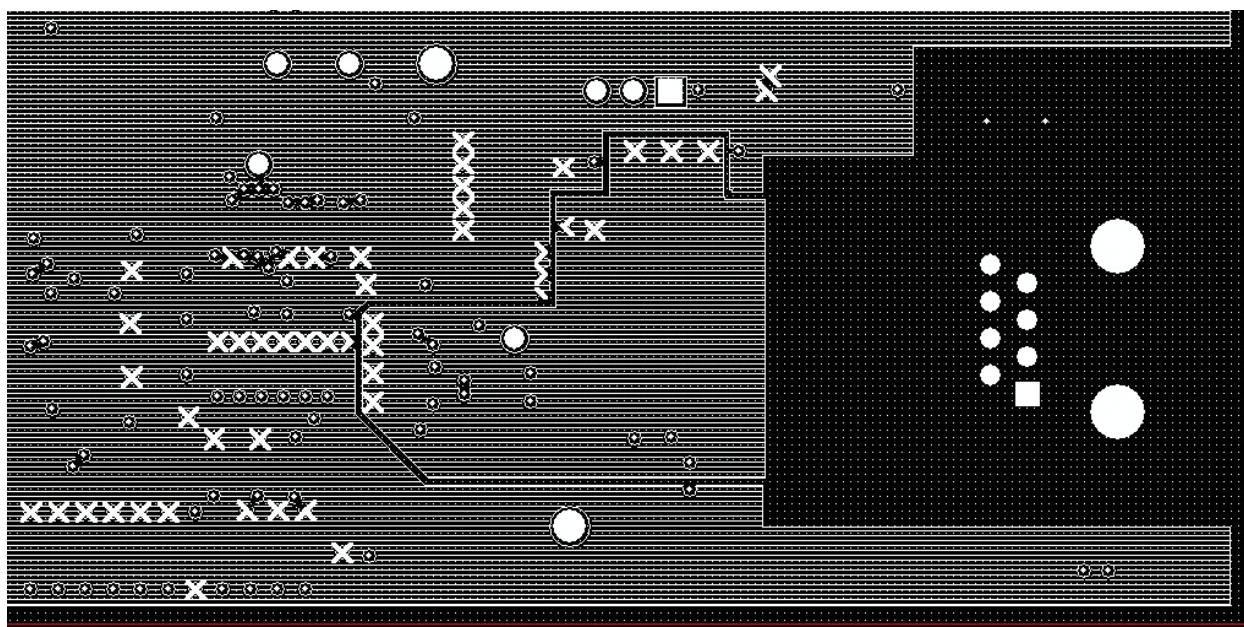


Figure 1.16 Layer 3 – Power Plane

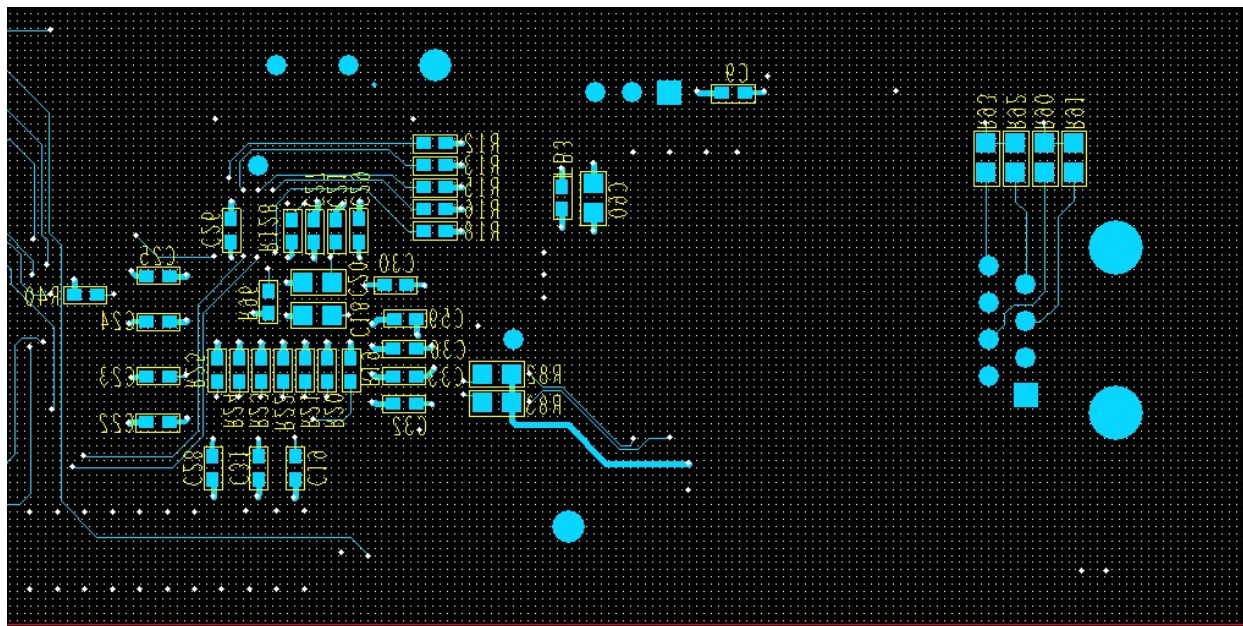


Figure 1.17 Layer 4 – Bottom Side Solder

1.18 PCB Design Considerations

1.18.1 Component Layout

Component placement can affect signal quality, emissions, and proper operation. This section provides guidelines for component placement. Careful component placement can:

- Minimize trace length and routing to avoid problems related with electromagnetic interference (EMI), which

- could cause failure to meet applicable government test specifications.

Decoupling capacitors should be located as close to the power they are decoupling as possible. This will allow them to be routed with the shortest, widest trace possible. The use of vias in connecting the decoupling caps should be minimized.

Simplify the task of routing traces. By selecting the magnetics module carefully, for instance, the Ethernet traces can be routed easily and as efficiently as possible. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces and minimize the use of vias as much as possible.

Bulk capacitors may be located anywhere on the voltage plane they serve.

Minimizing the amount of space needed for the Ethernet LAN interface is important because other interfaces will compete for physical space on your PCB. Keeping all the circuitry in a small, tight loop will ensure that EMI radiation is kept to a minimum. The Ethernet LAN circuits need to be as close as possible to the RJ45 connector.

1.18.2 Power & Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation. The following guidelines will help to reduce circuit inductance in your design:

Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

Physically locate grounds between a signal path and its return. SMSC recommends using at least a four layer PCB for your design. This will allow you to construct one of the layers (usually layer 2) as a solid, contiguous ground plane. Then, trying to route as many signals as possible on layer 1, will ensure you of having a good solid “image” plane close to most of your signals. This will minimize the loop area and minimize EMI.

The digital ground plane should be cleared out under half of the magnetics. Run the digital ground plane up under the magnetics halfway on the LAN9118 side of the magnetics. The other side of the magnetics facing the RJ45 should be clear of any and all planes. The RJ45 connector should have chassis ground beneath it.

1.18.3 Decoupling

Decoupling capacitors remove RF energy generated from high frequency switching components. They provide a localized source of current to oppose a change in voltage for devices or components, and are particularly useful in reducing peak current surges from being propagated across the PCB.

Components that switch logic states must be RF decoupled. This is because the switching energy generated by logic components will be injected into the power distribution system. This switching energy will be transferred to other logic circuits or subsections as common-mode and/or differential mode RF noise. Typically, one selects a capacitor with a self resonant frequency in the range of 2 – 100 MHZ for circuits with edge rates of 2 nano seconds or less.

Typical multilayer PCBs are self resonant in the 150 – 300 MHZ range. Proper selection of decoupling capacitors, along with knowing the self-resonant frequency of the PCB assembly (acting as one large bulk capacitor) will provide enhanced EMI suppression of digital switching noise. Surface mount devices have a higher self-resonant frequency by up to two orders of magnitude. This higher self-resonant frequency is due to less lead length inductance. Aluminum electrolytic capacitors are ineffective for high frequency decoupling and are best suited for power supply subsystems or power line filtering.

In addition to bypassing, high frequency RF decoupling must always be provided in all clock generation areas. To do this, calculate the decoupling capacitance value to suppress RF switching noise for all significant clock harmonics. Choose a capacitor with a self-resonant frequency higher than the clock harmonics requiring suppression, generally considered to be the fifth harmonic of the original clock frequency. In addition to this selection criteria, one must be cognizant of the amount of energy the capacitor provides to the component for proper operation. Decoupling capacitors ideally should be able to supply all the DC current necessary during a state transition.

1.18.4 Electrical Isolation

The magnetics and PWB layout and plane voiding combine to provide high electrical isolation, and prevent arching to the analog and digital logic under extreme potential conditions induced or conducted on the Ethernet cable. These may include electrostatic discharge (ESD) and other conducted or induced transient voltages.

1.18.5 EMI

EMI produced by electrical equipment is classified according to its dominant mode of propagation, either as radiated emissions of energy through space (similar to television and radio signal transmission) or conducted emissions of energy along wires (similar to telephone signals and AC power transmission).

Three elements must be present for an EMI event to exist. These three elements are: noise source, propagation path, and susceptor.



Noise source on a PCB relates to frequency-generating circuits, component radiation within a plastic package, ground bounce, electrically-long trace lengths, poor impedance control, cable interconnects, and the like.

Propagation path refers to the medium that carries the RF energy, such as free space or a metallic interconnect.

Susceptor is the device which receives undesired RF interference. If one of these three elements is removed, an EMI event cannot exist. It is our task to determine which of the three is the easiest to eliminate. We have no control over the susceptor, as we generally do not know what the susceptor will be. Suppression affects noise source, and is the easiest of the three to implement.

In suppressing the noise source, there are several key areas of the board design that should be addressed. Keep the transmit & receive differential pairs as short as possible. Make sure they are matched in length as best as possible. Make sure they reside on top of a contiguous reference plane. Keep these traces away from any other high speed signals. Make sure these traces are terminated properly. Do not use vias (or minimize the use of vias) in these differential traces. Try to keep these two differential pairs separated from each other as best as possible.

Keep the crystal circuitry associated with the LAN9118 as small a loop as possible. Place the crystal, crystal caps and series resistor all on the top layer referenced to the layer 2 ground plane. Keep all other signals away from the crystal area of the PCB.

SMSC recommends using a multi-layer PCB construction for best EMI performance. Avoid using excessively fast logic elsewhere in your design.

By following these particular guidelines and using standard engineering guidelines, your LAN9118 design should have very good EMI characteristics and pass most standards.

1.18.6 Reducing ESR & ESL Parasitic Losses for Bypassing

Ideal capacitors have only a capacitance property and therefore have no power loss. Real-world capacitors, on the other hand, have intrinsic resistive and inductive parasitic elements that can cause power loss. These losses can be characterized by Equivalent Series Resistance (ESR) & Equivalent Series Inductance (ESL). The nominal capacitance value is represented by the element (C) and its Insulation Resistance and inherent leakage current is represented by the element (Rp). Lower intrinsic losses result in a higher capacitor quality factor (Q), a higher Self-Resonance Frequency (SRF), less self-heating, and better performance more closely approaching an ideal capacitor.

No longer is the designer restricted to SMT - Chip Aluminum Electrolytic (wet or solid-polymer) or Chip Tantalum

(solid-polymer or low ESR). The superior equivalent series resistance (ESR) and equivalent series inductance (ESL) / impedance and reliability of MLCCs (Multi Layer Ceramic Capacitor) can now be found in the higher capacitance values.

In choosing the 10uF bulk capacitors required for the VDD_CORE_1.8V & VDD_PLL_1.8V pins, be sure to review datasheets with respect to ESR & ESL for any tantalum capacitor considered. Realize that these MLCCs may afford a cheaper and more effective solution due to the large capacitance and low ESR required.

Resistive and inductive parasitic losses can be minimized by capacitor design to approach an ideal capacitor. Cost, package size, availability, and mechanical reliability during lead-free soldering processes are concerns when selecting capacitors. The on-chip LAN9118 regulators require a low ESR and ESL capacitors for stability. Wire bond, package lead, and PWB trace resistance and inductance will degrade regulator performance. The design engineer should minimize these parasitic losses contributed by the external traces and components. Both high frequency and bulk capacitors should be used. The SMSC recommended capacitor types, values and tolerances have performed well in validation testing with the component placement demonstrated in the sample design. Reduced trace length and increased trace thickness will improve bypass capacitors efficacy by reducing parasitic losses.

1.18.7 Differential Balanced Traces

Differential pairs in combination with the magnetics are used to improve signal integrity by reducing emissions and rejecting common mode induced noise. The impedance of these signals must be matched between the elements to ensure maximum power transfer and low losses including EMI. The design engineer is cautioned to calculate and match the 100-ohm differential impedance required for the PWB traces connecting the RJ45 connector to the magnetics and the magnetics to the LAN9118. To minimize EMI, these traces should also be kept short. There are several PWB design considerations that must be controlled to provide a uniform impedance. Some of these factors are PWB dielectric constant, trace width, height, thickness, and spacing from each other and from a reference plane and whether a solder mask is used and its thickness. These traces must be routed away from digital traces. The differential traces from the magnetics to the RJ45 connector do not run over a plane and hence their width and spacing will vary with respect to those run over an analog ground plane from the magnetics to the LAN9118 to keep a 100-ohm differential characteristic impedance.

1.19 Conclusion

Following the guidelines presented in this application note will ensure adequate performance from the LAN9118.

Note: Good design practice should also be followed for component placement, trace routing, impedance control and EMI radiation. Analog and digital partitioning are generally design specific, but following these guidelines will help ensure successful implementations.

1.20 Package Outline

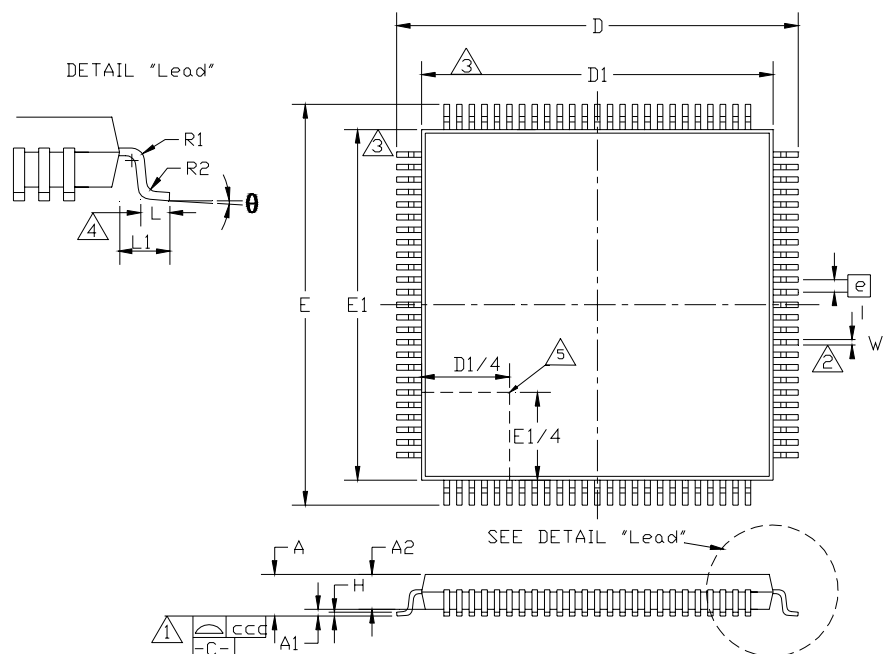


Figure 1.18 100 Pin TQFP Package Outline, 14X14X1.4 Body, 2 mm Footprint

Table 1.9 100 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0°	~	7°	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.

2 Revision History

NAME	REVISION LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Marcom	Rev. 1.6 (1-28-09)		Standard SMSC Formatting



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