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## PCB Layout Guide for MEC142x

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### INTRODUCTION

This application note provides information on design considerations for a printed circuit board (PCB) for the Microchip MEC142x family devices including the following:

- MEC1424, MEC1426, MEC1428

The design of the PCB requires care to provide good supply and ground paths; in addition, other design issues are addressed in this document.

The functional blocks in the MEC142x have different requirements for routing and external connections, which are also outlined in this application note.

Please see [References](#) for device-level information such as VTR power planes, and mechanical package information for the 128-Pin VTQFP, 144-Pin WFBGA, and the 128-Pin WFBGA.

This document includes the following topics:

- [General Layout Considerations on page 2](#)
- [Miscellaneous Considerations on page 10](#)
- [2-Wire Debug Interface \(ICSP\) on page 19](#)
- [Programmable Comparators on page 21](#)
- [How to set up ADC voltage states to distinguish PC model and pcb types on page 25](#)
- [MEC142x Shared SPI Flash Isolation Requirement on page 26](#)

### Audience

This document is written for a reader that is familiar with hardware design. The goal of this application note is to provide information about sensitive areas of the MEC142x PCB layout.

### References

The following documents should be referenced when using this application note. Please contact your Microchip representative for availability.

- Microchip MEC142x EVBs
- Microchip MPLAB ICD3 In-Circuit Debugger User's Guide (Doc#: DS51766B)
- PCI Local Bus Specification (see [www.pcisig.com](http://www.pcisig.com))
- I<sup>2</sup>C-bus specification and user manual, Rev. 6 - 4 April, 2014 or later (see [www.nxp.com/documents/user\\_manual/UM10204.pdf](http://www.nxp.com/documents/user_manual/UM10204.pdf))
- Intel, Enhanced Serial Peripheral Interface (eSPI) Specification (for Client Platform)

### Package Information

The MEC142x device is currently available in the following packages:

- MEC142x for 128-pin, VTQFP
- MEC142x for 144-pin, WFBGA
- MEC142x for 128-pin, WFBGA

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## GENERAL LAYOUT CONSIDERATIONS

This section describes layout considerations for the MEC142x devices. This includes the following topics:

- [Decoupling Capacitors on page 2](#)
- [32.768kHz Crystal Oscillator on page 6](#)
- [CAP Pins, AVSS/GND Connection on page 7](#)
- [BGA Package PCB Layout Considerations on page 7](#)

### Decoupling Capacitors

This section includes the following topics:

- [MEC142x VTQFP Capacitors on page 2](#)
- [MEC142x WFBGA Capacitors on page 4](#)

Decoupling capacitors should be placed as close to the chip as possible to keep series inductance low. When the capacitors are mounted on the bottom side of the PCB, the capacitors are connected to the ground plane from the bottom layer directly using the shortest path to the device. Each VTR pin should have a 0.1  $\mu\text{F}$  capacitor located as close to the pin as possible. Bypass capacitors should be placed close to the supply pins of the MEC142x with short and wide traces.

The MEC142x has an integrated voltage regulator to supply the core circuitry. Decoupling this regulator requires a critical capacitor of 1 $\mu\text{F}$  on the CAP pin. ESR of this 1 $\mu\text{F}$  capacitor, including the routing resistance, must be less than 100 mOhm.

Capacitors may carry large currents that generate magnetic fields, inducing noise on nearby traces. Sensitive traces such as the 32kHz crystal should be separated by at least five times the trace width from decoupling capacitors when possible.

Connecting decoupling caps to power and ground planes using two vias per pad will reduce series inductance.

- [FIGURE 1: on page 3](#) shows decoupling for the MEC142x 128-pin VTQFP.
- [FIGURE 2: on page 4](#) shows decoupling for the MEC142x 144-pin WFBGA.
- [FIGURE 3: on page 5](#) shows decoupling for the MEC142x 128-Pin WFBGA.

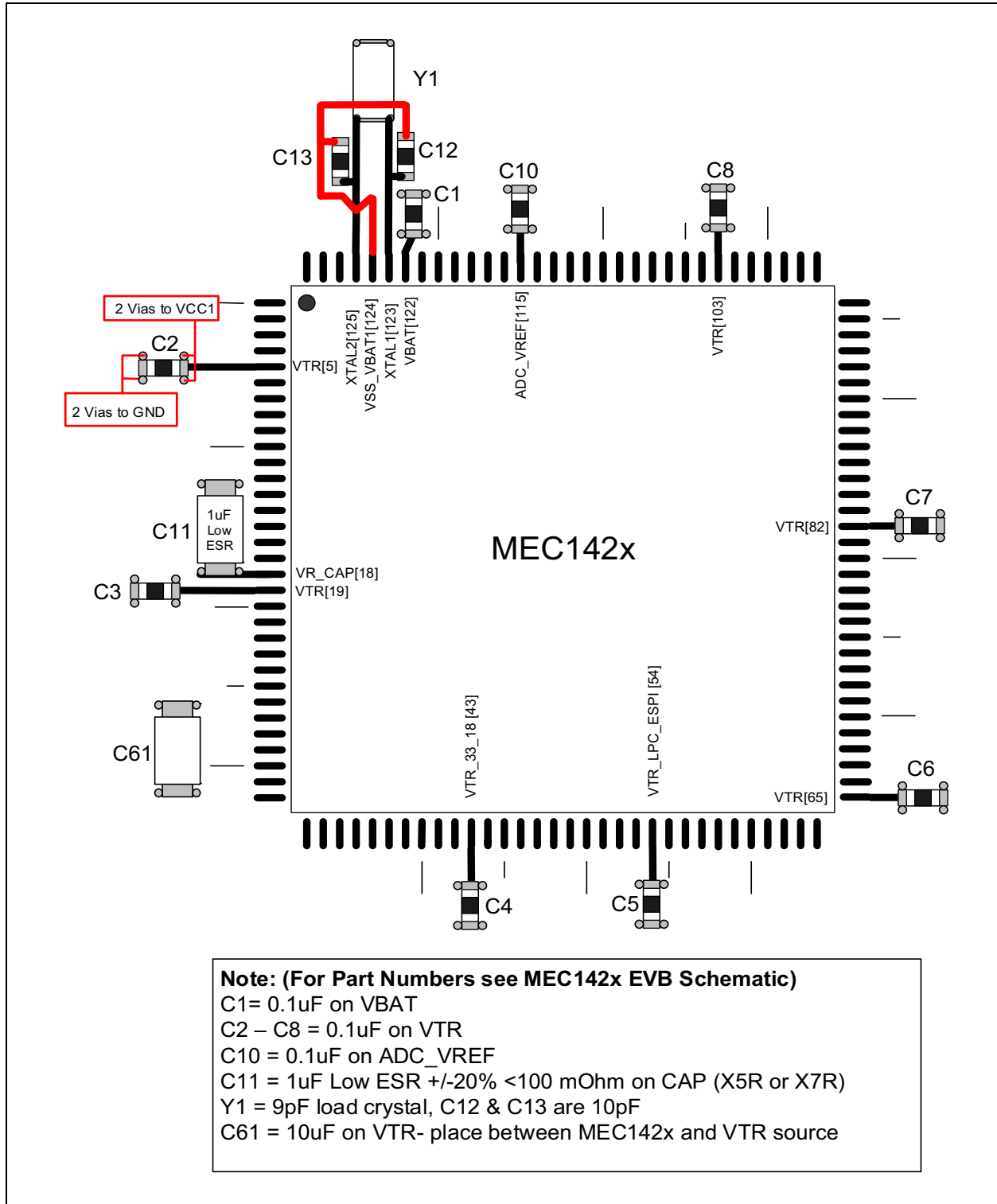
The VTR pin decoupling capacitors can use any typical 16V 10% Ceramic. Also see the MEC142x EVB Schematics and Bill of Materials.

### MEC142X VTQFP CAPACITORS

- [Figure 1](#) shows decoupling for the MEC142x 128-pin VTQFP package.

<b>Note:</b> The capacitors can use any typical 16V 10% ceramic.
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**FIGURE 1: MEC142X DECOUPLING IN 128-PIN VTQFP PACKAGE**



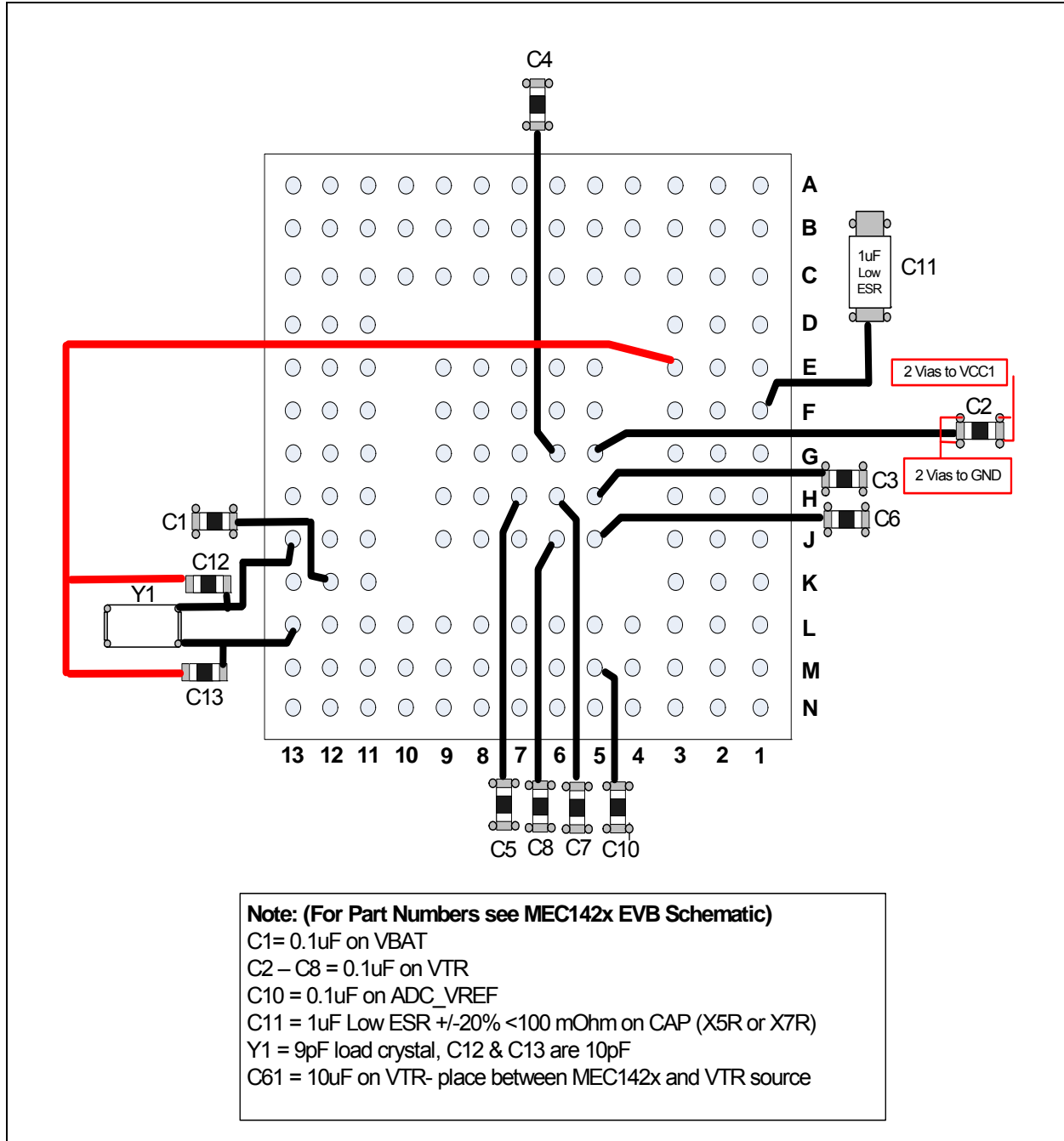
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## MEC142X WFBGA CAPACITORS

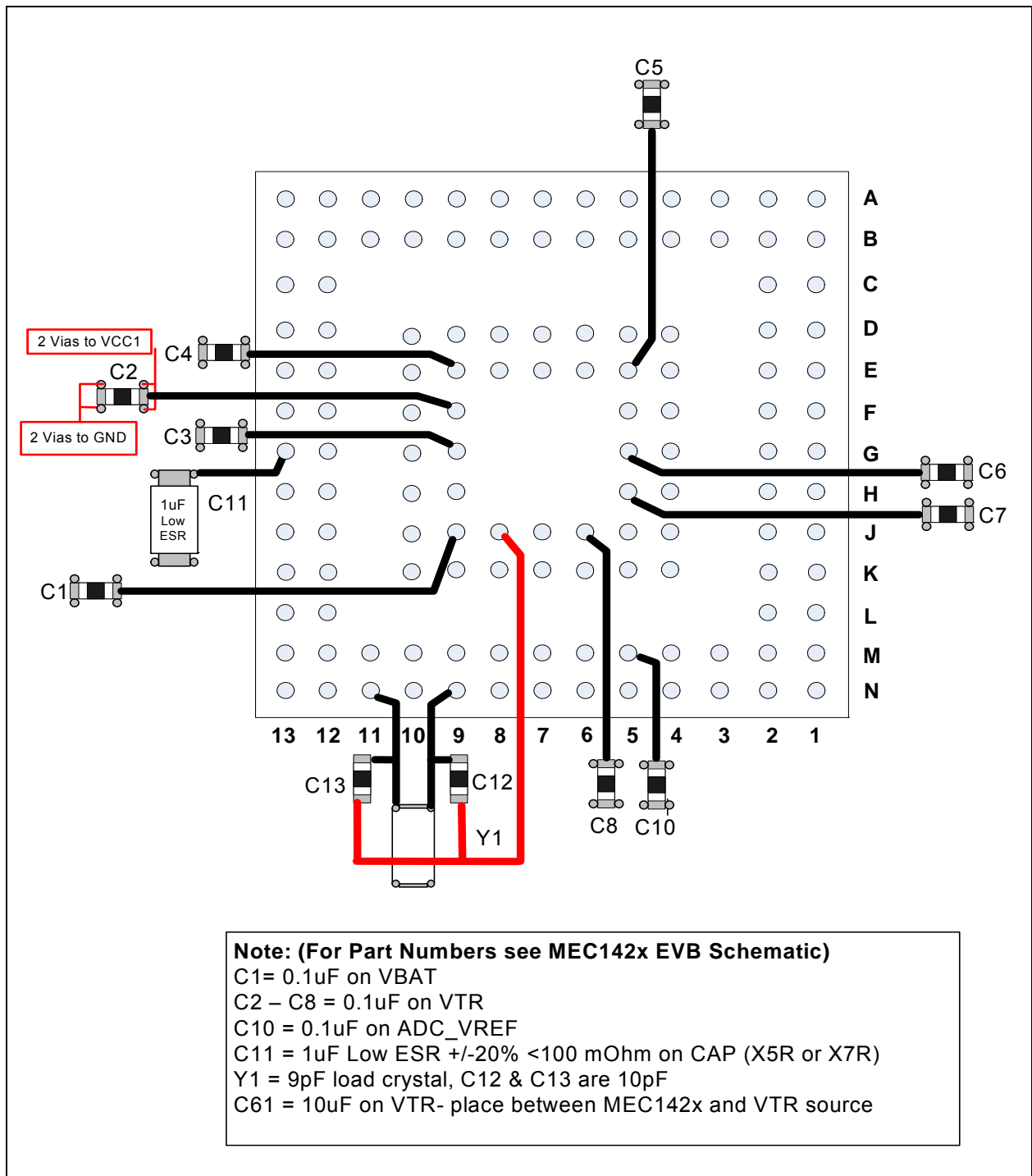
Figure 2 shows decoupling for the MEC142x 144-pin WFBGA package. And Figure 3 shows decoupling for the MEC142x 128-pin WFBGA package.

The capacitors can use any typical 16V 10% ceramic.

**FIGURE 2: MEC142X DECOUPLING IN 144-PIN WFBGA PACKAGE**



**FIGURE 3: MEC142X DECOUPLING IN 128-PIN WFBGA PACKAGE**



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## 32.768kHz Crystal Oscillator

This section describes specific layout and design considerations for the 32.768kHz crystal oscillator; this can be used to source the internal 32kHz clock domain, in lieu of the silicon oscillator or an external pin. The crystal implementation is required to support the RTC function within the MEC142x.

### 32.768KHZ CRYSTAL OSCILLATOR LAYOUT

The MEC142x 32kHz crystal oscillator is designed to generate an synchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5  $\mu$ W typical), stability and minimum jitter using a general purpose parallel resonant 32kHz crystal. For a suggested part number, please see the MEC142x EVB schematic (see [References](#)).

This unique low power crystal oscillator drive circuit means that a standard inverter crystal layout should not be used. The design has been characterized to allow a variation of 4pF to 18pF on each pin. Based on the following load capacitance calculation, Microchip recommends 10pf load capacitors with a crystal that has a 9pf CI rating. Other than these capacitors, no additional external components are required for normal operation of the clock circuit.

$$\text{Effective Load Capacitance} = C1 = \frac{[C11 + Cpin\_xtal2][C12 + Cpin\_xtal1]}{C11 + Cpin\_xtal2 + C12 + Cpin\_xtal1} + Cbrd$$

Where:

- C12 is the cap from pin XTAL1 to ground.
- C13 is the cap from pin XTAL2 to ground.
- Cpin\_xtal2 is the pin capacitance of pin XTAL2. This is estimated to be 5pf ([Note 1](#)).
- Cpin\_xtal1 is the pin capacitance of pin XTAL1. This is estimated to be 3pf ([Note 1](#)).
- Cbrd is estimated at 1.5pF.

**Note 1:** At the time of publication, the MEC142x silicon has not been characterized. Please check with your Microchip FAE for final pin capacitance values after silicon validation is complete. Any variation from the estimates provided here could change the crystal CI value requirement.

### CRYSTAL ACCURACY

The accuracy of the 32kHz input translates directly into accuracy of the internal clock and the functions in the MEC142x using the 32kHz: 32KHZ\_OUT, week timer, hibernation timers, and so forth.

The accuracy, with regard to actual error in time can be illustrated as such: +/-1ppm of error in frequency corresponds to 32.768 kHz x 1ppm x 10<sup>-6</sup> = +/-0.032768 Hz. This translates into ~1  $\mu$ sec/sec or ~+/-0.086 sec/day.

Based on customer RTC accuracy timer requirements, Microchip recommends using a +/-20ppm crystal. This would equal approximately +/-2 sec/day, other factors discounted.

For arguments sake, it is safe to say that stray capacitance is difficult to calculate exactly. So, as an exercise in completeness, this calculation describes the effect of each picofarad of additional capacitance over/under the crystal C<sub>load</sub> value:

$$\text{ppm/pF} = \frac{C_1 \times 10^6}{2(C_0 + C_L)^2}$$

where C<sub>0</sub> is the shunt capacitance, C<sub>1</sub> is the motional capacitance and C<sub>L</sub> is the load capacitance of the chosen crystal (these numbers can be found in the crystal data sheet). For example, using a crystal with C<sub>0</sub> = 0.8pF, C<sub>1</sub> = 0.0019pF, C<sub>L</sub> = 12.5pF, we get a shift of 5.37ppm/pF. So, in terms of time, each pF of added/subtracted capacitance is approximately 5.37 x 0.086 = +/-462 msec/day for this particular crystal.

This example is meant to illustrate the magnitude of the potential error. In practice, slight capacitance mismatch does not equate to many seconds a day.

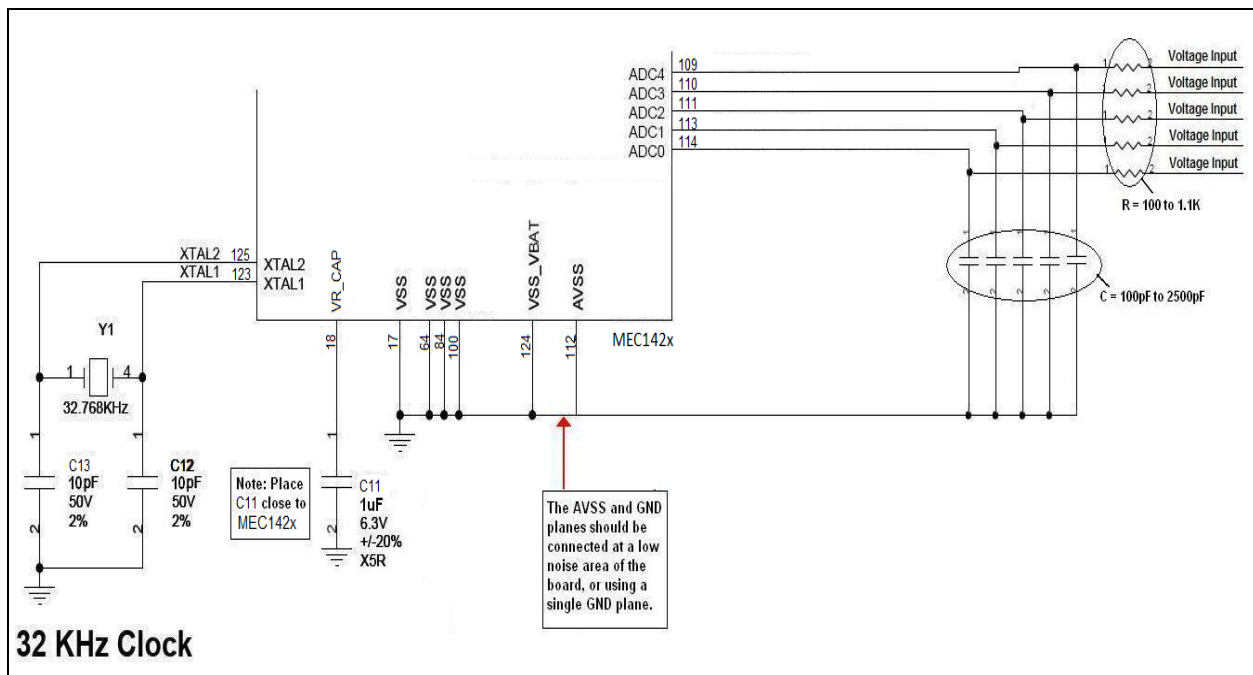
## SINGLE ENDED CLOCKING

An external clock source (maximum voltage of 3.3V) may be applied to the XTAL2 pin if the XOSEL bit in Clock Enable Register configures as a single-ended 32.768 kHz clock input (SUSCLK). The XTAL1 pin should be left floating. If an external clock source is used, the designer must ensure that the source is available in all desired power states in which the EC will be active.

## CAP Pins, AVSS/GND Connection

The recommended filtering for the CAP pin on the MEC142x is shown in Figure 4, for VTQFP connections. The filtering components shown should be close to the device and away from noise sources.

**FIGURE 4: VTQFP CAP PIN REFERENCE AND AVSS DIRECTLY CONNECTED TO GND**



## BGA Package PCB Layout Considerations

The MEC142x devices have BGA lead-free RoHS-Compliant package as follows:

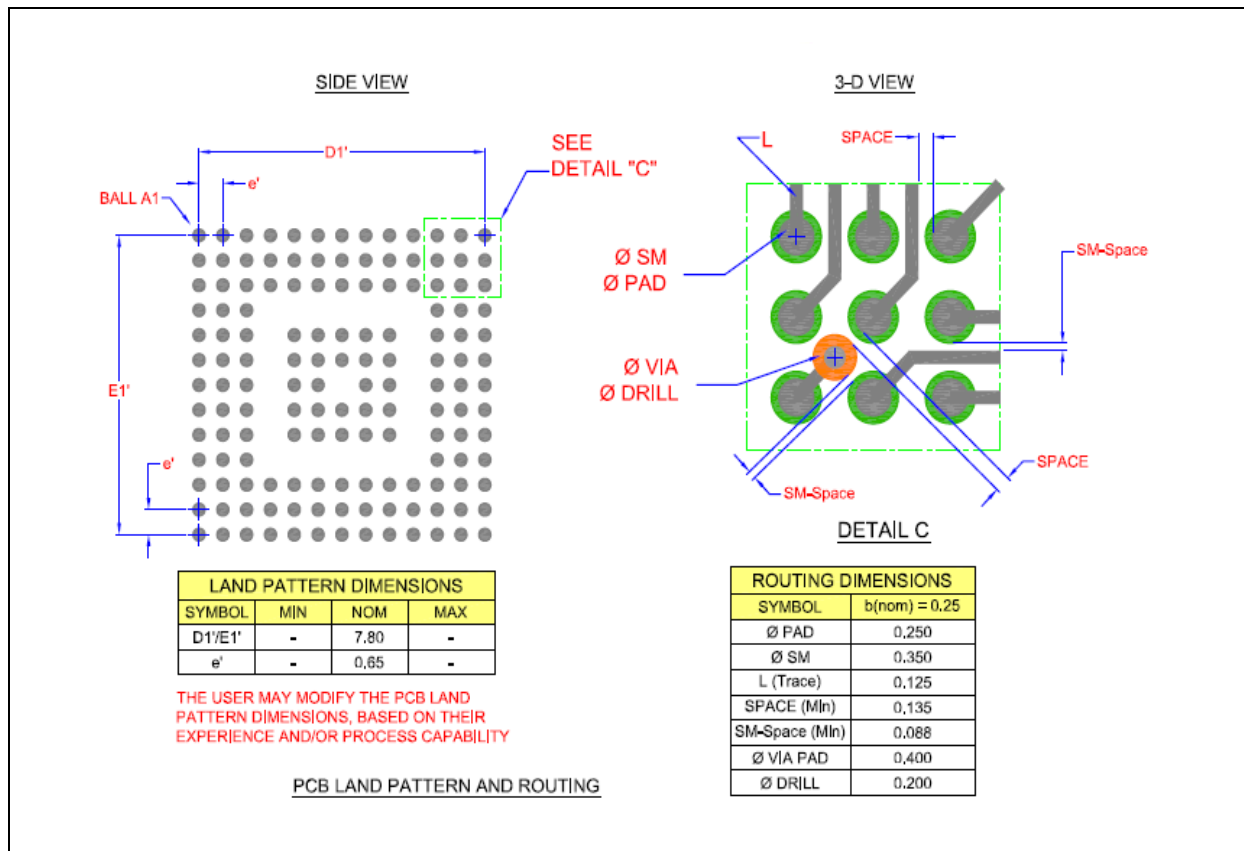
- 128-pin WFBGA Lead-free RoHS Compliant Package (see Figure 6)
- 144-pin WFBGA Lead-free RoHS Compliant Package (see Figure 5)

**Note:** Please refer to the latest data sheet for most up-to-date PCB LAND pattern information.

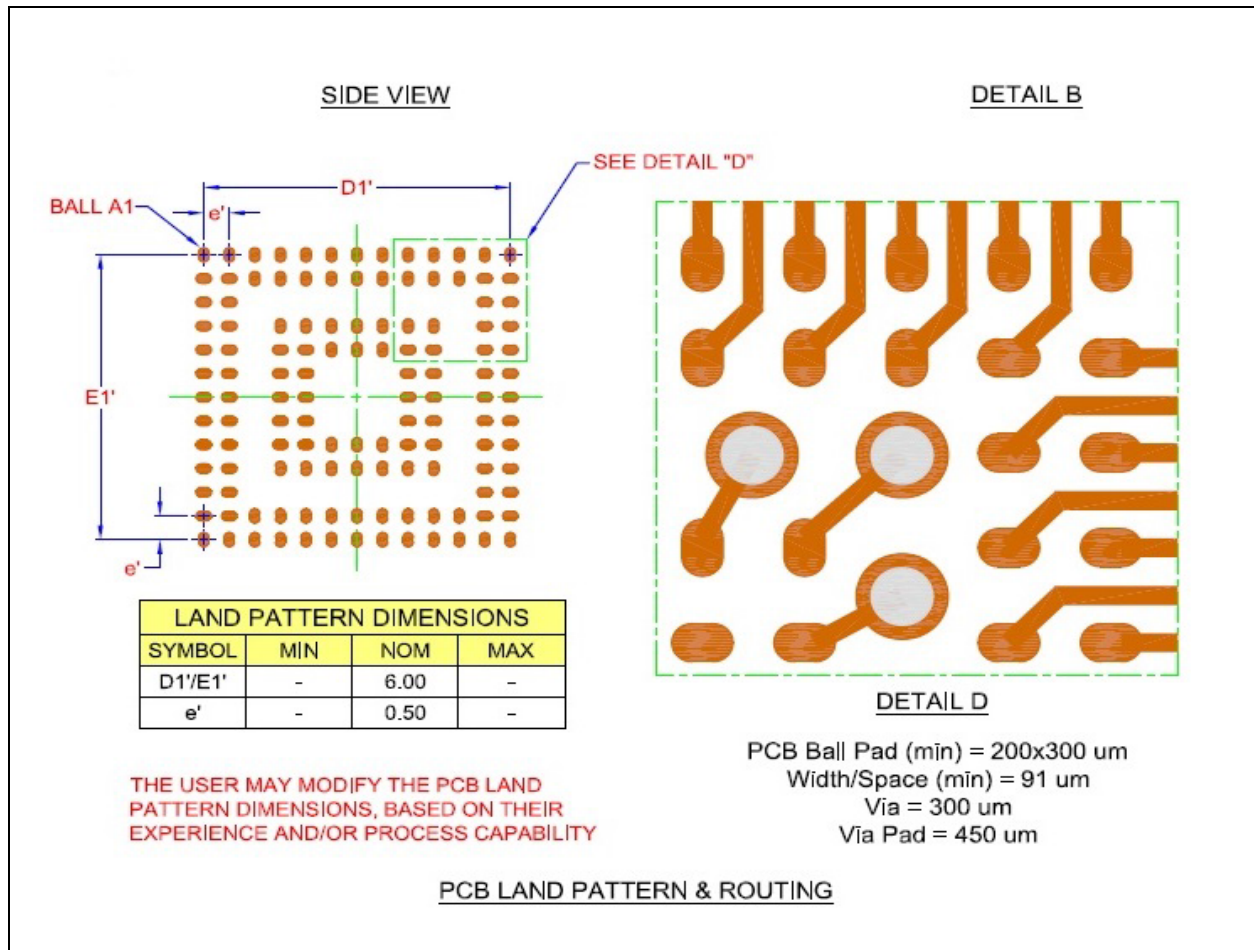
The following list summarizes BGA routing guidelines, but it is understood that final layout is process- dependent and your design should reflect your needs:

- Through-hole vias technology is not recommended for pitches less than 0.8mm (unless the ball matrix is depopulated in the center)
- NSMD ball pads for pitches 0.8mm – 0.4mm
- Solder Mask to be 1:1 scale of the land size, when routing 0.5mm pitch ball pads
- $\mu$ Vias – next generation PCB technology for tighter pitches
- Eliminate through-hole vias
- Increase routing density & enhance electrical performance
- Decrease routing layers
- Provide fan-out solutions for multiple layers (stacked Vias)

**FIGURE 5: LAND PATTERN DIMENSIONS, 144-WFBGA, 0.65MM BALL PITCH**



**FIGURE 6: LAND PATTERN DIMENSIONS 128-WFBGA**



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## MISCELLANEOUS CONSIDERATIONS

This section covers a variety of layout topics:

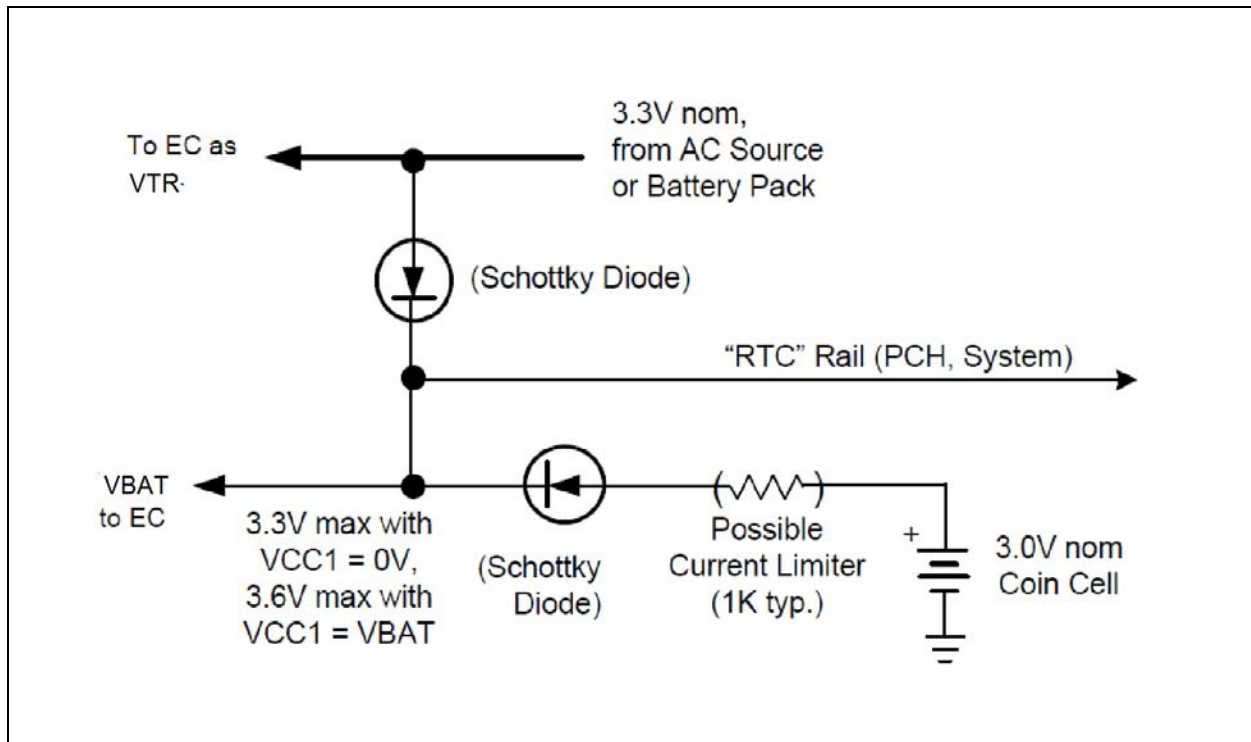
- [Battery Circuit on page 10](#)
- [LPC Interface on page 11](#)
- [eSPI Interface on page 11](#)
- [PS/2 Interface on page 12](#)
- [EOS Considerations on page 12](#)
- [ADC Input Layout Requirement for Regular Sampling on page 13](#)
- [SPI Flash Interface on page 14](#)
- [1MHz Pullup Resistor Requirement on page 18](#)
- [5V Tolerant Pins on page 18](#)
- [1.8V Capability on page 18](#)

### Battery Circuit

Please see the Power Sources section of the MEC142x Data Sheet.

For the battery circuitry requirement, VBAT must always be present if VTR is present. The following circuit is recommended to fulfill this requirement.

**FIGURE 7: RECOMMENDED BATTERY CIRCUIT**



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## LPC Interface

The firmware must configure the GPIO Pin Control Registers for the LPC alternate function, configure the LPC Base Address Register, and activate the LPC block.

### VTR\_LPC\_ESPI POWER PIN

The LPC Interface Signals require the VTR\_LPC\_ESPI power pin to be connected to the 3.3V VTR rail. Please also configure the VTR\_LPC\_ESPI\_SEL18 bit 3 at Power Regions Voltage Control Register (0xFC48) accordingly.

### HOST RESET SELECT

The platform reset signal that will be used to assert nSIO\_RSET is determined by the POWER RESET CONTROL Register (80148h) Bit 1 = 0 - LRESET# pin.

### LAD[3:0] /LFRAME#/ LDRQ#/SERIRQ

The AC and DC specifications for these signals are set the same as defined for AD[31:0] in Section 4.2.2 of the “*PCI Local Bus Specification, Rev 2.1*”. That section contains the specifications for the 3.3V signaling environment. LAD[3:0] must go high during the TAR phase. The last device driving the LAD[3:0] is responsible to drive the signals high during the first clock of the TAR phase. During the 2nd clock, LAD[3:0] is floated and maintained high by weak pullup resistors (approximately 100 k  $\Omega$ ). These pullups are not included in the MEC142x, but may be included in the chipset.

### OTHER SIGNALS

All the other LPC I/F signals are connected to other PCI signals that are already present in the system. The MEC142x use 3.3V signaling for all LPC signals, including the PCI Reset and Clock, therefore the system must drive these signals at 3.3V signaling levels.

## eSPI Interface

The firmware must configure the GPIO Pin Control Registers for the eSPI alternate function, configure the eSPI I/O Component Base Address Register, and activate the eSPI block.

### VTR\_LPC\_ESPI POWER PIN

The eSPI Interface signals require the VTR\_LPC\_ESPI power pin to be connected to the 1.8V rail. Please also configure the VTR\_LPC\_ESPI\_SEL18 bit 3 at Power Regions Voltage Control Register (0xFC48) accordingly.

### HOST RESET SELECT

The platform reset signal that will be used to assert nSIO\_RSET is determined by the POWER RESET CONTROL Register (80148h) Bit 1 = 1 - eSPI\_PLTRST# pin.

### OTHER SIGNALS

All the eSPI I/F signals are connected to other eSPI signals that are already present in the system. The MEC142x use 1.8V signaling for all eSPI signals. Please refer to the Intel Skylake Ultrabook Platform U-Series RVP Customer Reference Board Schematic, Microchip MEC142x Evaluation Board Schematic, and reworks instruction for detailed information.

Few design notes as below:

- LPC\_AD0\_ESPI\_IO0, LPC\_AD1\_ESPI\_IO1, LPC\_AD2\_ESPI\_IO2, LPC\_AD3\_ESPI\_IO3, LPC\_FRAME\_ESPI\_CS#, and LPC\_CLK\_0\_ESPI\_CLK signals have 15 ohm series resistor close to each chipset pin and another 15 ohm series resistor close to the MEC142x for eSPI mode.
- GPP\_C5/SML0ALERT# (Intel Skylake chipset pin W1) is used as ping pin to determine either LPC mode (Low) or eSPI mode (High).

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## PS/2 Interface

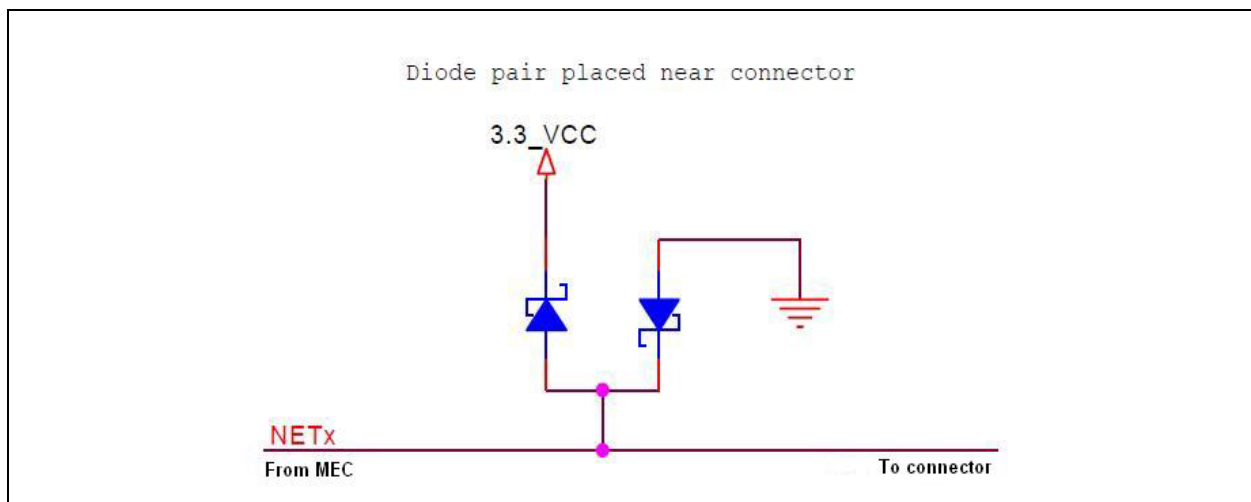
The routing of the PS/2 interface is also not critical, except that it should not be routed next to rapidly switching signals. The Clock and Data pins are Open Drain and require pullup resistors. A small 10 - 100pF (typ) capacitor to ground and 4.7k $\Omega$  (typ) pullups are recommended. The power pin of the PS/2 pin should be decoupled with a capacitor that is large enough to adequately filter the supply to PS/2 devices. Unused PS/2 clock and data pins should be pulled up to VTR with a 10k $\Omega$  (typ) resistor.

**Note:** The PS/2 Interface is not 5V tolerant.

## EOS Considerations

For SMBus signals that terminate external to the main system board (for example, Smart Battery) the designer should take care in protecting these signals from EOS (Note 1:) and ESD (Note 2:). Please refer to the SMBus 2.0 specification, section 3.1.2.2 for appropriate guidelines. The specification recommends a series protection resistor and an optional ESD transorb on these nets. In addition to the SMBus specification recommendation, past experience shows that using 2 high speed diodes on each SMBus trace (instead of the transorb in the SMBus spec) is an effective way to improve immunity to EOS and ESD events. A Schottky diode pair is a good example. Figure 8 shows the suggested circuit implementation for each net that goes to a connector.

**FIGURE 8: SCHOTTKY DIODE PAIR EXAMPLE**



It should also be noted that any other signal that goes to an external connector should also be considered for EOS/ESD susceptibility. For instance, an ID pin (tied to a GPIO) that might seem benign, but is routed near high voltage sources could suffer transient EOS events. A similar protection scheme should be considered for these nets.

- Note 1:** EOS is defined as damage to the part caused by the application of voltages (to any pin) beyond the power supply rails, usually forward biasing internal protection diodes and resulting in high levels of current flow. This typically induces open failures by damaging the metal inside the part. EOS is typically a low voltage, high current situation.
- 2:** ESD is the applied reverse bias to the PN junction -- heat due to power dissipation melts the silicon in the part. ESD is typically a high transient voltage spike with low current situation.

## ADC Input Layout Requirement for Regular Sampling

ADC has a large internal resistance.

Every ADC input terminal has a gate switch.

This gate switch is protected by diodes.

It is natural for diodes have leakage current.

At sampling time: (Gate switch closed)

Input voltage is charged and sampled at sample point A.

Sampling time is affected by RC time constant defined by internal resistor and internal capacitor.

In continuous mode, the sampling time is too fast for sample point A to discharge sampled value. In this case, glitch will not be observed.

In one shot mode or in long report mode, the sampling time is long enough for point A to discharge sampled value.

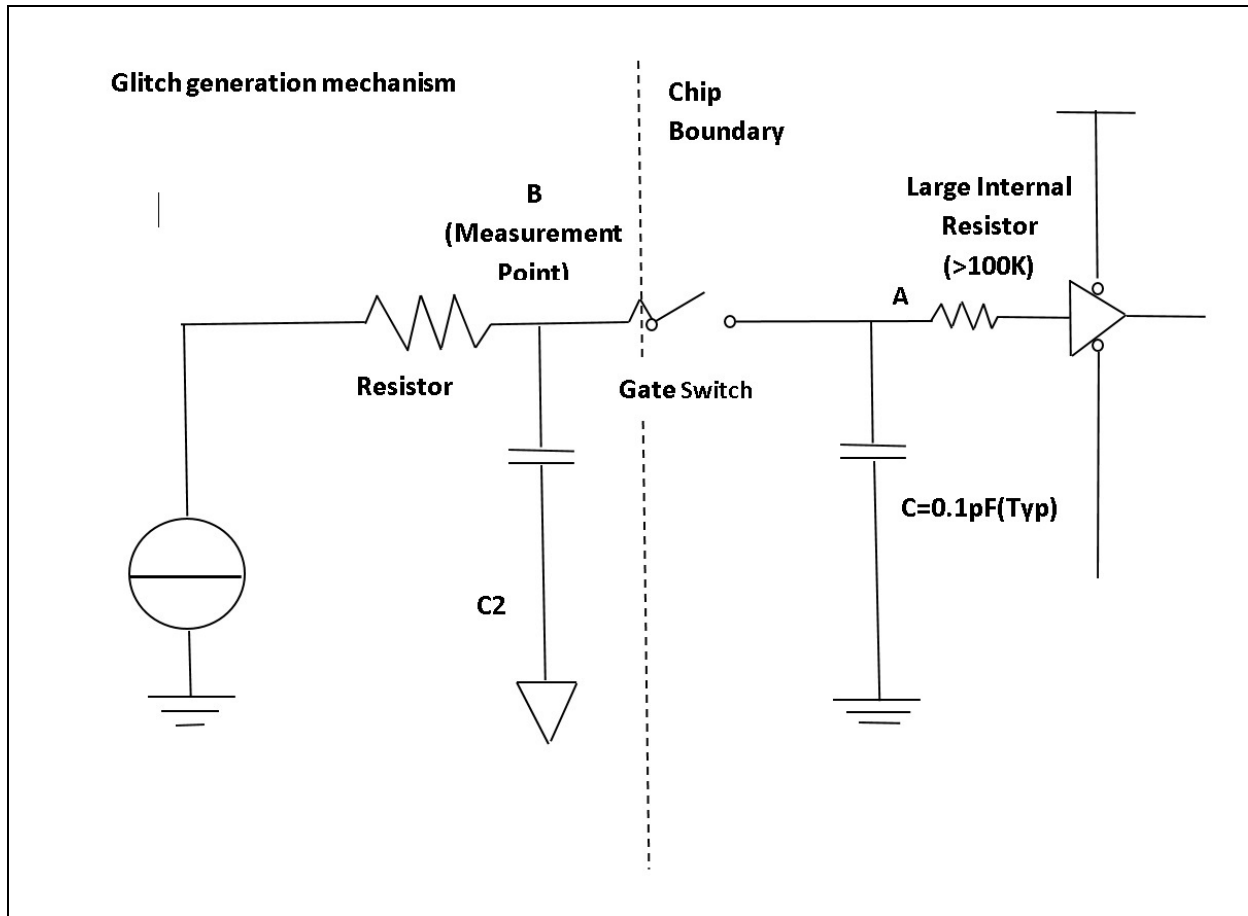
In this case, glitch will be observed on the next sampling point.

If an external capacitor with value between 0.1 $\mu$ F and 0.01 $\mu$ F (point C2) is placed on the input terminal, the charged value at point A will be kept as it is instead of discharging it and then glitch will not be observed.

For high sampling frequencies, it is recommend to set the cut off frequency of the R/C at  $\frac{1}{2}$  of the ADC sampling frequency / 10.

Please also refer to the white paper at [ww1.microchip.com/downloads/en/AppNotes/00699b.pdf](http://ww1.microchip.com/downloads/en/AppNotes/00699b.pdf) for more information.

FIGURE 9: ADC INPUT LOW PASS FILTER



## SPI Flash Interface

The MEC142x SPI flash interface enables the host and embedded controller (EC) access to an external SPI flash device. The MEC142x PCS documentation has more details on signal implementation (see [References on page 1](#)). This section describes specific PCB layout design considerations to setup this feature.

The standard set of SPI flash signals are designated with “SHD\_” for shared connections, for example, SHD\_SCLK; for details, see [Shared SPI Flash Interface on page 15](#). MEC142x has an added set of signals for connection to another SPI flash device as private, protected data; these signals are designated with “PVT\_,” for example, PVT\_SCLK; for details, see [Private SPI Flash Interface on page 17](#). The Private SPI can be used as a crisis recovery interface as it shares pins with the keyboard interface. MEC142x has a third SPI interface as a general SPI interface labeled as “SPI\_,” for example, SPI\_CLK.

**Note:** The SHD SPI Flash Interface of MEC142x support both 1.8V & 3.3V depends on VTR\_33\_18 power pin setting. The PVT SPI Flash Interface of MEC142x support 3.3V ONLY. Please refer to data sheet for more information.

TABLE 1: SPI INTERFACE SIGNALS

Generic Pin Signal Name	Pin Signal Function name	MEC142x Pin Number	Pin Function Signal Description
SPICLK	SHD_SCLK	32	Shared SPI Clock
	PVT_SCLK	15	Private SPI Clock
IO0	SHD_IO0 / SHD_MOSI	28	Shared SPI Data I/O 0
	PVT_IO0 / PVT_MOSI	16	Private SPI Data I/O 0
IO1	SHD_IO1 / SHD_MISO	29	Shared SPI Data I/O 1
	PVT_IO1 / PVT_MOSI	2	Private SPI Data I/O 1
IO2	SHD_IO2	30	Shared SPI Data I/O 2
	PVT_IO2	24	Private SPI Data I/O 2
IO3	SHD_IO3	31	Shared SPI Data I/O 3
	PVT_IO3	23	Private SPI Data I/O 3
SPI_CS#	SHD_CS#	27	Shared SPI Chip Select
	PVT_CS#	14	Private SPI Chip Select

### BOOT ROM STRAP OPTION

- If the CR\_STRAP pin is connected to ground the Boot ROM will load the SPI Flash image from the SPI Flash located on the Private SPI Interface (PVT\_xxxx).
- If this pin is pulled high, which is the normal operation for the Key Scan Interface, the Boot ROM will load the SPI Flash image from the Shared Flash Interface (SHD\_xxxx) or the eSPI Flash channel as selected by the Boot Source Select Strap (BSS\_STRAP) on the GPIO123/SHD\_CS0# pin.

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI (Crisis Recovery mode)
1	0	Use eSPI Flash Channel (eSPI MAFS mode)
	1	Use Shared SPI (includes eSPI SAFS mode)

### PRIMARY RAILS GOOD STRAP

The Primary Rails Good Strap option (PRG\_STRAP) is implemented on GPIO135/SHD\_IO2[PRG\_STRAP]. This strap is used for booting from the eSPI flash channel using Master Attached Flash Sharing (MAFS).

### VOLTAGE LEVEL STRAP

The Voltage Level Strap option (VL\_STRAP) is implemented on GPIO117/TFDP\_CLK/UART\_TX[VL\_STRAP].

The VL\_STRAP pin is used to indicate to the boot ROM what the voltage level is on the pins in the region that is powered by the VTR\_33\_18 supply. This pin must be pulled up to 3.3V (VTR) to indicate the region is at 3.3V; and pulled low to indicate the region is 1.8V.

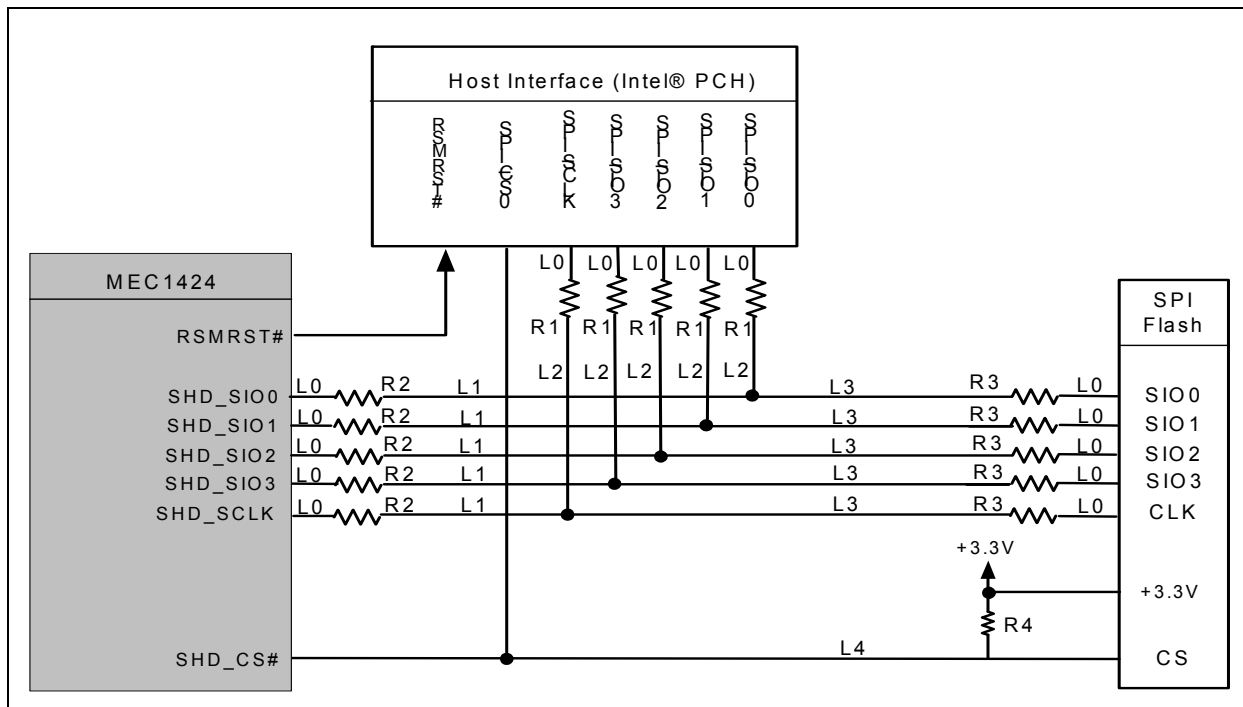
### SHARED SPI FLASH INTERFACE

Shared SPI Flash Implementation:

Figure 10 is a topology for implementing a single MEC142x SPI flash for shared SPI flash devices. See Table 2 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

**Note:** In order for the Core Logic to be controlled by the RSMRST# signal, the PCH Primary Power Rails are required to be powered along with the EC. Otherwise, the isolation circuit will be needed in the Shared SPI implementation.

**FIGURE 10: MEC142X TOPOLOGY FOR SHARED SPI FLASH DEVICE**



**TABLE 2: MEC142X SHARED SPI FLASH DEVICE SPECIFICATIONS**

	Description	Spec
L0	Connection between MEC142x, Host/PCH, or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	PCB trace from the MEC142x termination resistor to the PCB trace connection from the SPI flash and Host/PCH.	L1 = L2 = L3 These trace connections can equal 1-inch up to 5-inches. See Note 3:
L2	PCB trace from the Host/PCH termination resistor to the PCB trace connection from the SPI flash and MEC142x.	
L3	PCB trace from the SPI flash termination resistor to the PCB trace connection from the MEC142x or Host/PCH.	
L4	PCB trace from Host/PCH or MEC142x to SPI flash for chip select.	L4 = L1 + L3 + (2 x L0) or L4 = L2 + L3 + (2 x L0) +/- 0.100 inches.
R1	These resistors are between the PCB trace and the Host/PCH.	25 ohm, see Note 1., 2:
R2	These resistors are between the PCB trace and the MEC142x.	15 ohm, see Note 1., 2:
R3	These resistors are between the PCB trace and the SPI flash.	15 ohm, see Note 1., 2:
R4	Pull-high resistor to +3.3V for SPI CS connections; between the MEC142x or Host/PCH and the SPI flash device. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

**Note 1:** The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC142x (-0.3V min. to  $V_{CC1}+0.3V$  max).

**2:** Resistor recommendations are based on testing with 180nm PCH and SPI flash drivers. Any change to a driver would require a change to the related termination resistors, see also Note 1.:

**3:** L1, L2, L3 must be equal to each other. For example, if L1 = 2-inches, then L3 must be 2-inches.

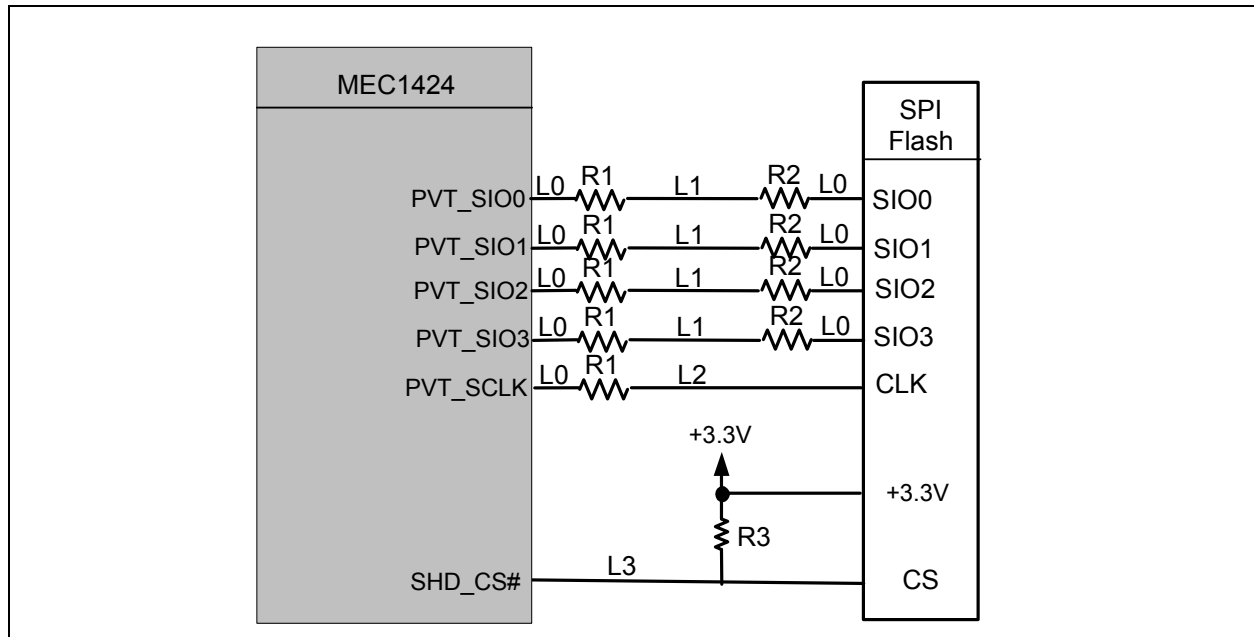
## PRIVATE SPI FLASH INTERFACE

**Note:** Either Shared SPI or Private SPI interface can support a dedicated SPI chip. The Private SPI is targeted for use as a crisis recovery option since it is muxed with keyscan pins.

Private SPI Flash Implementation:

Figure 11 is a topology for implementing the MEC142x SPI flash for a single private SPI flash device. See Table 3 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

**FIGURE 11: MEC142X TOPOLOGY FOR PRIVATE SPI FLASH DEVICE**



**TABLE 3: MEC142X PRIVATE SPI FLASH DEVICE SPECIFICATIONS**

	Description	Spec
L0	Connection between MEC142x or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	The PCB trace between terminating resistors on the IO lines.	1-inch to 10-inch
L2	The PCB trace from MEC142x or R1 resistor to SPI flash.	1-inch to 10-inch
L3	PCB trace from MEC142x to SPI flash for chip select.	L3 = L0 + L1
R1	These resistors are between the trace and the MEC142x.	25 ohm, see <a href="#">Note</a> :
R2	This resistor is on the IO lines between the SPI flash and trace.	45 ohm, see <a href="#">Note</a> :
R3	This is a Pull-High resistor (to +3.3V) for SPI CS connections. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

**Note:** The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC142x (-0.3V min. to  $V_{CC1} + 0.3V$  max).

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## SPI FLASH IMPLEMENTATION RECOMMENDATIONS

The following recommendations are for both Shared and Private SPI Flash Implementations.

- The MEC142x SPI memory interface has serial flash device compatibility requirements that are defined in the MEC142x PCS. Please make sure the selected SPI flash meets these requirements.
- SPI\_CLK must be 20mils spacing from any other high frequency (>1GHz) signal.
- The SPI flash parts should support operating at 8.5MHz for the ROM code loader, and up to 33MHz clock speed in RAM code loading.
- The designer should follow the SPI interface host design guidelines.
- IBIS models are available to aid in simulating the SPI system topology.
- The chip select CS# signals should have weak pullup resistors to the same power rail as the SPI flash. The pullup resistor value should meet the rise time requirements of the SPI flash.
- EC firmware must configure the MEC142x SPI memory interface to disable mode, which will tri-state the SPI memory interface from MEC142x to the SPI flash, before releasing the RSMRST# signal.
- This configuration requires that the PCH tri-state its SPI flash pins when RSMRST# is asserted.
- The characteristic impedance of the PCB trace should be 50 ohms +/-15% at 50MHz operating frequency.
- Within the SPI flash device, Schmitt trigger inputs are assumed on both the clock line and IO data lines.
- Within the Intel PCH, a Schmitt trigger input is assumed on the IO data lines.
- The output drivers for the SPI flash chip select pins should be programmed as open-drain using the GPIO Pin Control registers.
- The SPI Data IO traces should be length-matched to the CLK lines within 0.100-inch.
- Signal Integrity should be checked for each SPI part on your BOM.

## SPI FLASH EXTERNAL PROGRAMMER

The SPI Flash on either Shared or Private SPI Flash interface must be programmed externally using a suitable programmer, such as Dediprog's SF100 (<http://www.dediprog.com/pd/spi-flash-solution/sf100>).

Provisions for a programming header on each SPI flash are recommended if the SPI is not socketed.

## 1MHz Pullup Resistor Requirement

Please refer to the I<sup>2</sup>C-bus specification and user manual as indicated in [References on page 1](#) for more information.

## 5V Tolerant Pins

There are no 5V tolerant pins on the MEC142x.

## 1.8V Capability

Please refer to the MEC142x Data Sheet section 2.6 for more information.

**Note:**

- The LPC Interface Signals require the VTR\_LPC\_ESPI power pin to be connected to the 3.3V VTR rail. The eSPI Interface signals require the VTR\_LPC\_ESPI power pin to be connected to the 1.8V rail. The GPIO signals on these pins may operate at either 1.8V or 3.3V. Please also configure the VTR\_LPC\_ESPI\_SEL18 bit 3 at Power Regions Voltage Control Register (0xFC48) accordingly.
- The SMB00 to SMB04 Ports have the option to be configured for either 3.3V or 1.8V signaling. This selection is determined by the GPIO alternate function mux.

## 2-WIRE DEBUG INTERFACE (ICSP)

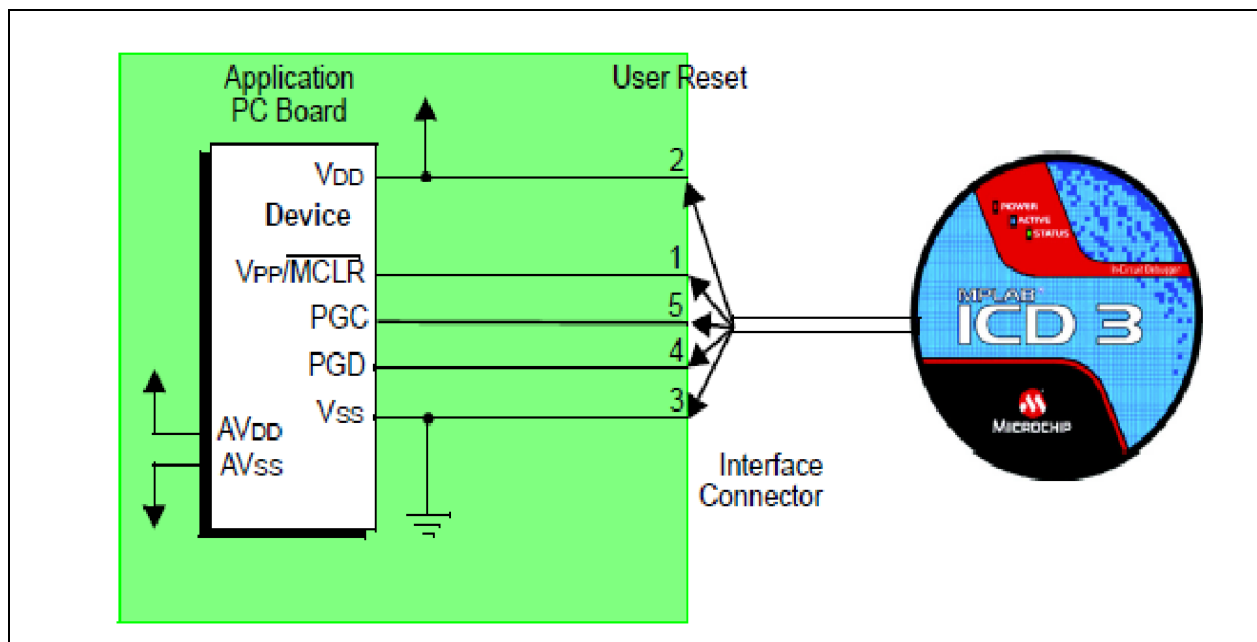
Please refer to the Microchip ICD User Manual as indicated in the section [References on page 1](#) for more information.

- [Figure 12](#) shows the standard recommended target circuitry.
- [Figure 13](#) shows the circuits that will prevent the debugger from functioning.

**TABLE 4: ICSP INTERFACE SIGNALS**

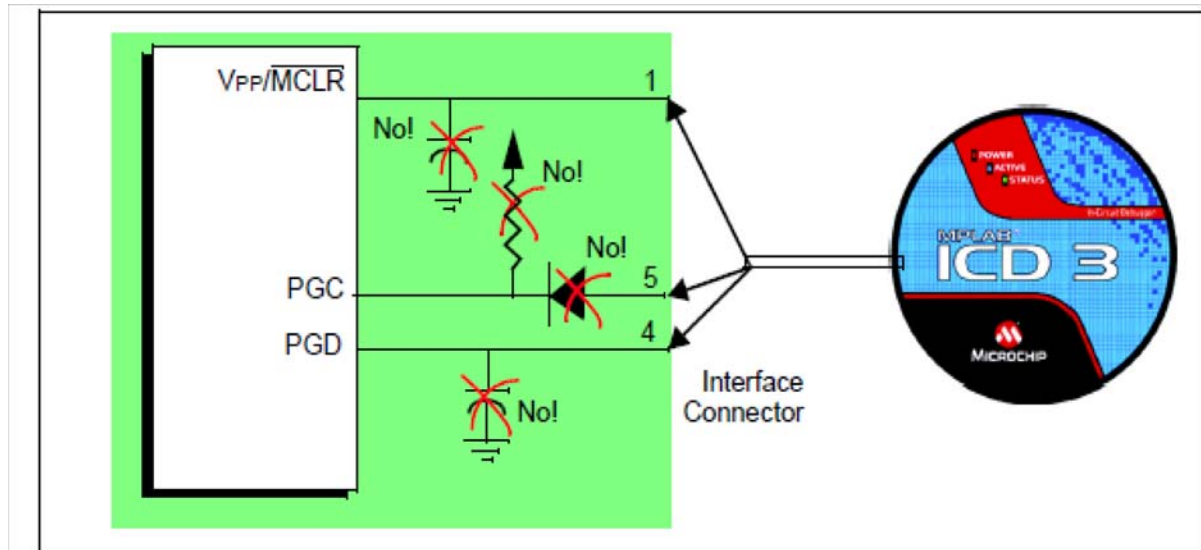
Pin Signal Function name	MEC142x Pin Number	Pin Function Signal Description
ICSP_MCLR	87	ICSP Master Clear <b>Note:</b> This pin requires external 10K pulled high to avoid floating.
ICSP_CLOCK	101	ICSP Clock (shown as PGC in <a href="#">Figure 12</a> )
ICSP_DATA	102	ICSP Data (shown as PGD in <a href="#">Figure 12</a> )

**FIGURE 12: STANDARD CONNECTION TARGET CIRCUITRY**



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FIGURE 13: IMPROPER CIRCUIT COMPONENTS



Specifically, these guidelines must be followed:

- Do not use pull-ups on PGC/PGD – they will disrupt the voltage levels, since these lines have 4.7 k $\Omega$  pull-down resistors in the debugger.
- Do not use capacitors on PGC/PGD – they will prevent fast transitions on data and clock lines during programming and debug communications.
- Do not use capacitors on  $\overline{MCLR}$  – they will prevent fast transitions of  $V_{PP}$ . A simple pull-up resistor is generally sufficient.
- Do not use diodes on PGC/PGD – they will prevent bidirectional communication between the debugger and the target device.

## PROGRAMMABLE COMPARATORS

MEC142x has two programmable comparators.

Figure 5 shows the comparators signals information.

Figure 14 show the comparators alternate circuitry in single supply operation.

See the additional information that can be used as reference.

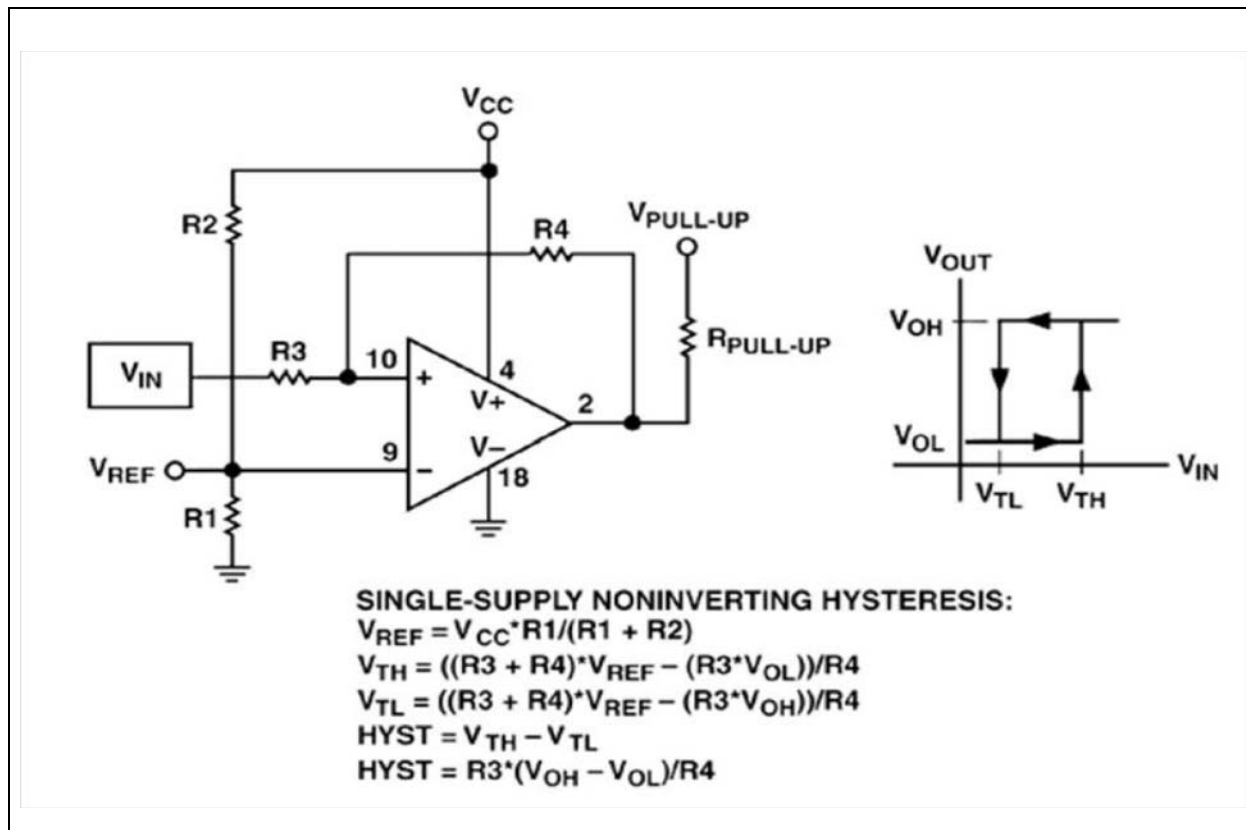
- Hysteresis is implemented externally by implementing feedback resistor circuit on VOUT to VIN pin.
- Input voltage range (VIN) from 0 to 3.63V.
- Input threshold range may come from VREF pin or from internal DAC that is configurable from 0 to 3.63V.

**TABLE 5: COMPARATORS SIGNALS**

Pin Signal Function name	MEC142x Pin Number	Pin Function Signal Description
GPIO165/CMP_VREF0	25	Comparator 0 Voltage Reference
GPIO020/CMP_VIN0	20	Comparator 0 Voltage Input
GPIO124/CMP_VOUT0	85	Comparator 0 Voltage Output
GPIO166/CMP_VREF1	26	Comparator 1 Voltage Reference
GPIO021/CMP_VIN1	21	Comparator 1 Voltage Input
GPIO120/CMP_VOUT1	83	Comparator 1 Voltage Output

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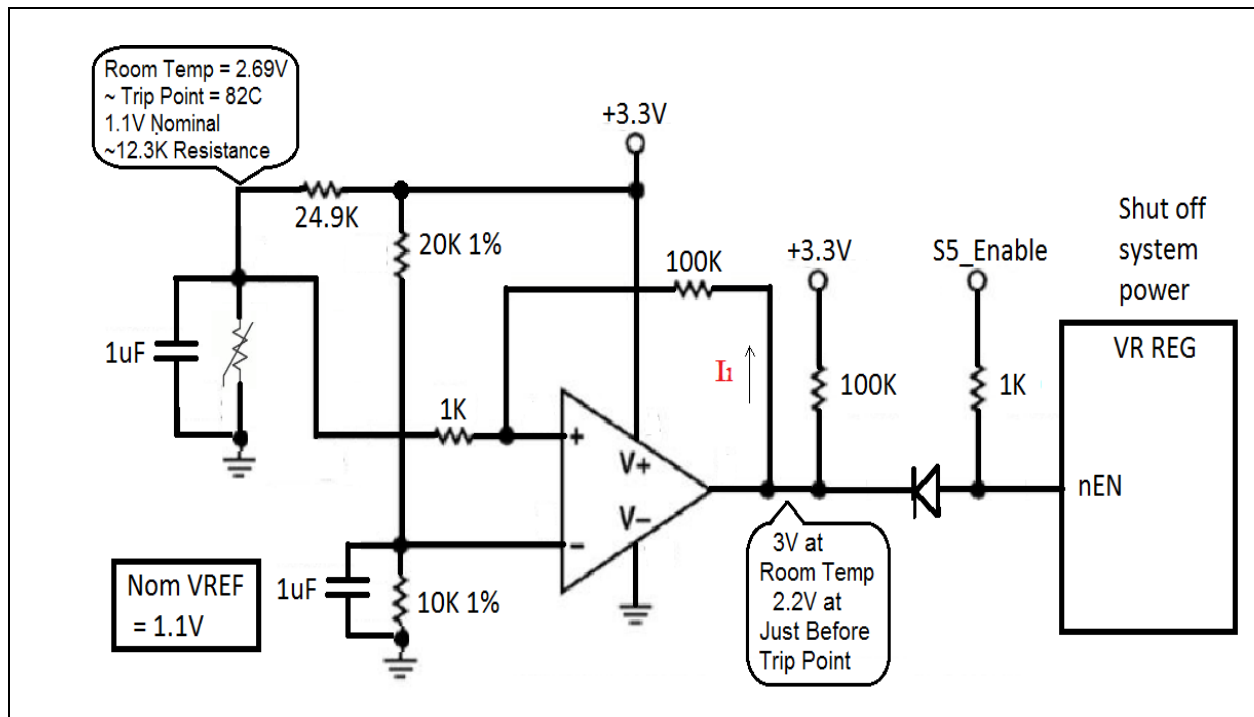
FIGURE 14: COMPARATORS IN SINGLE-SUPPLY OPERATION



## Thermistor Application

This section shows the calculation of the nominal hysteresis for the circuitry shown in [FIGURE 15: THERMISTOR APPLICATION EXAMPLE](#) on page 23.

FIGURE 15: THERMISTOR APPLICATION EXAMPLE



## COMPARATOR VOLTAGE OUTPUT CALCULATION

Use Kirchoff's Voltage Law with assumption  $I_2 = 0$ , ideal condition with some small leakage in uAmps region.

**EQUATION 1: AT ROOM TEMP**

$$-3.3V + I_1 (100K) + I_1 (100K) + I_1 (1K) + 2.69V = 0$$

$$I_1 (201K) = 0.66V$$

$$I_1 = 3.3\mu\text{Amps}$$

$$100K \times 3.3\mu\text{Amps} = 0.3V$$

$$3.3V - 0.3V = 3V \text{ at Room Temperature}$$

**EQUATION 2: JUST BEFORE TRIP POINT**

$$-3.3V + I_1 (100K) + I_1 (100K) + I_1 (1K) + 1.1V = 0$$

$$I_1 (201K) = 2.2V$$

$$I_1 = 11\mu\text{Amps}$$

$$100K \times 11\mu\text{Amps} = 1.1V$$

$$3.3V - 1.1V = 2.2V \text{ at Just Before Trip Point}$$

## 0.0.1 HYSTERESIS CALCULATION

**EQUATION 3: JUST BEFORE TRIP POINT**

$$-2.2V + I_1(100K) + I_1(1K) + 1.1V = 0$$

$$I_1 (101K) = 1.1V$$

$$I_1 = 11\mu\text{Amps}$$

$$V_{IN} = 11\mu\text{Amps} (1K) + 1.1V = 1.111V$$

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## EQUATION 4: AFTER TRIP POINT

$$1.1V = 100K / 101K (V_{IN})$$

$$V_{IN} = 1.089$$

As the results, the hysteresis is +/- 11mV, total 22mV between 1.111V to 1.089V.

## CONCLUSION

- Based on the 100K and 1K external feedback resistor values chosen, the nominal is +/- 11m and the total of 22mV hysteresis.
- The output of the comparator is ~3V at room temperature.
- The output of the open drain comparator at just before trip point is 2.2V, which is still high enough based on fact of the circuitry.
- Trip point at ~ 82C, based on a typical 100K NTC Thermistor resistance numbers from the thermistor data sheet.

## HOW TO SET UP ADC VOLTAGE STATES TO DISTINGUISH PC MODEL AND PCB TYPES

This section provides general guidelines regarding how to use the ADC input to distinguish the PC models and PCB types in the design as follows:

1. Ensure choosing resistor values taking into account the effects of the ADC input impedance (refer to MEC142x Data Sheet for more information).
2. Make sure the tolerance of the large resistors are taken into account.
3. Final calculated voltages taking into account of the ADC input impedance and Resistor tolerance should give the designer a range of voltages for each resistor set, then make sure there is enough voltage separation to distinguish (accounting for anticipated system noise and accuracy of ADC input resolution), recommends a minimum of 250mV between ADC steps for a robust design.
4. Adjust resistor (such as lower value of resistors used, or use a better tolerance if needed) if step 3 is not satisfactory.

### Reference Example

This section shows the calculation and suggestion based on the above guideline.

#### IDEALIZED CASE

	Pull Down	Pull Up	Ideal Voltage Divider	Gap
1	100K	10K	3V	0.199V
2	100K	17.8K	2.801V	0.203V
3	100K	27K	2.598V	0.197V
4	100K	37.4K	2.402V	0.2V
5	100K	49.9K	2.201V	0.2V
6	100K	64.9K	2.001V	0.193V
7	100K	82.5K	1.808V	0.214V
8	100K	107K	1.594V	0.295V
9	100K	154K	1.299V	0.199V
10	100K	200K	1.100V	

#### IDEALIZED CASE WITH 3 MOHM INPUT IMPEDANCE

	Pull Down	Pull Up	Ideal Voltage Divider	Gap
1	96.774K	10K	2.991V	0.204V
2	96.774K	17.8K	2.787V	0.207V
3	96.774K	27K	2.58V	0.2V
4	96.774K	37.4K	2.38V	0.203V
5	96.774K	49.9K	2.177V	0.202V
6	96.774K	64.9K	1.975V	0.194V
7	96.774K	82.5K	1.781V	0.214V
8	96.774K	107K	1.567V	0.294V
9	96.774K	154K	1.273V	0.197V
10	96.774K	200K	1.076V	

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WITH 1% RESISTORS TOLERANCE - WORST CASE ANALYSIS

Actual Pull Down with 3 Mohm Input	
99%	95.83736689K
100%	96.77419355K
101%	97.71041599K

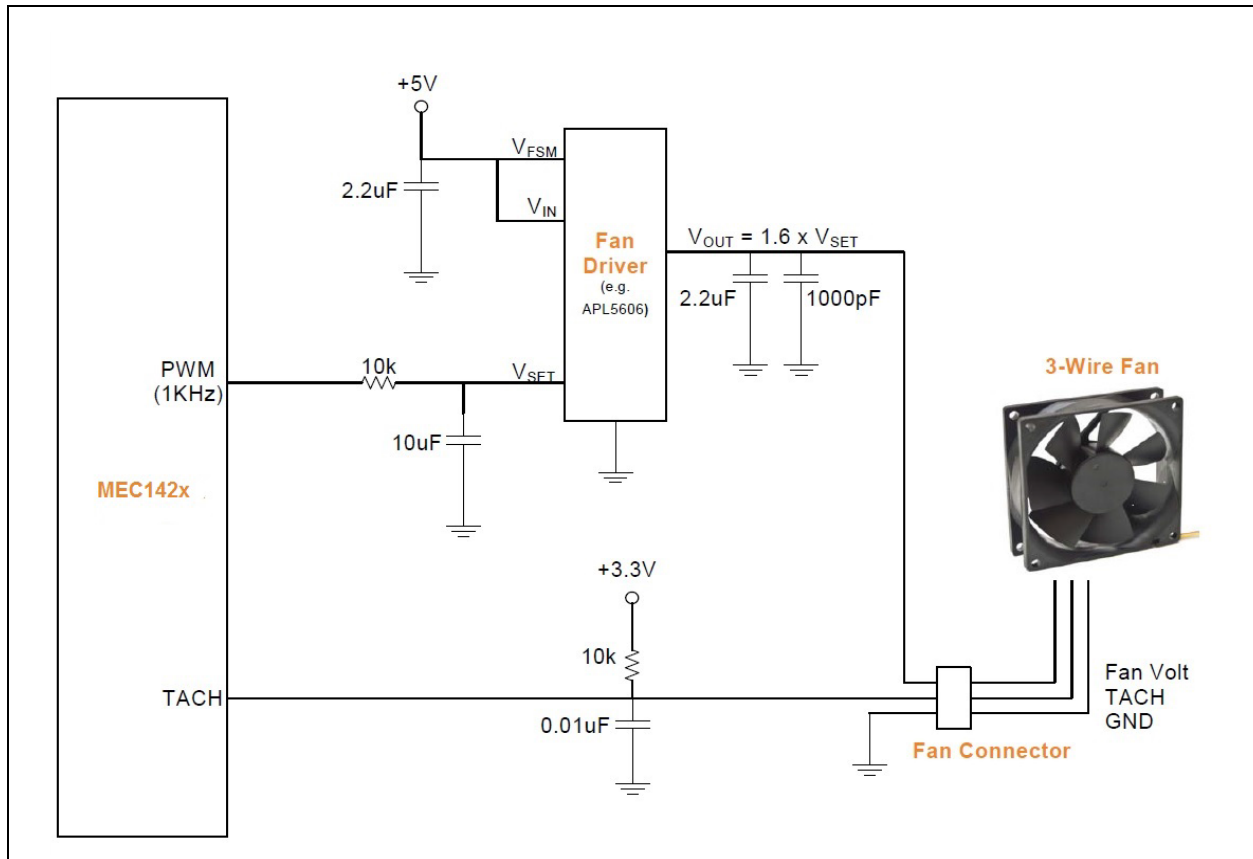
Low Side			High Side			
101% Pull Down w/ 3 Mohm	Low Side Pull Up (99%)	High Side Voltage	99% Pull Down w/ 3 Mohm	High Side Pull Up (101%)	Low Side Voltage	GAP
97.71K	9.9K	2.996V	95.837K	10.1K	2.985V	0.19V
97.71K	17.622K	2.796V	95.837K	17.978K	2.779V	0.188V
97.71K	26.73K	2.591V	95.837K	27.27K	2.569V	0.176V
97.71K	37.026K	2.393V	95.837K	37.774K	2.367V	0.175V
97.71K	49.401K	2.192V	95.837K	50.399K	2.163V	0.172V
97.71K	64.251K	1.991V	95.837K	65.549K	1.96V	0.162V
97.71K	81.675K	1.797V	95.837K	83.325K	1.765V	0.182V
97.71K	105.93K	1.583V	95.837K	108.07K	1.551V	0.262V
97.71K	152.46K	1.289V	95.837K	155.54K	1.258V	0.168V
97.71K	198K	1.09V	95.837K	202K	1.062V	

## PWM CONTROLLED 3-WIRE FAN

Pulse Width Modulation (PWM) modules, which produce basically digital waveforms, can be used in many applications as a more efficient and lower power alternative to the traditional 8 bit Digital-to-Analog (D/A) converters using only two inexpensive filter components. A wide variety of microcontroller applications that exist today are better served by utilizing a PWM generated analog output as opposed to an 8 bit D/A converter. One application where using a high resolution PWM has value vs. a traditional 8 Bit DAC is in driving the 3-wire voltage controlled fan in a PC.

The typical schematic of a 3 wire fan drive is shown in [Figure 16](#) by PWM.

**FIGURE 16: 3-WIRE FAN DRIVE BY PWM WITH R/C FILTER**



**Note:** The DAC should be remained disabled to save ~1mA power.

Please refer to the “AN2137 - PWM Controlled Fan fro MEC140x/MEC141x” for more information.

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## MEC142X SHARED SPI FLASH ISOLATION REQUIREMENT

The MEC142x uses the GPIO123/SHD\_CS0#[BSS\_STRAP] pin as a strap to determine the boot source (eSPI Flash channel or shared SPI).

There is a new requirement to put isolation on the board if the Shared SPI flash is used so that the SPI\_CS# is detected high while RSMRST# is low.

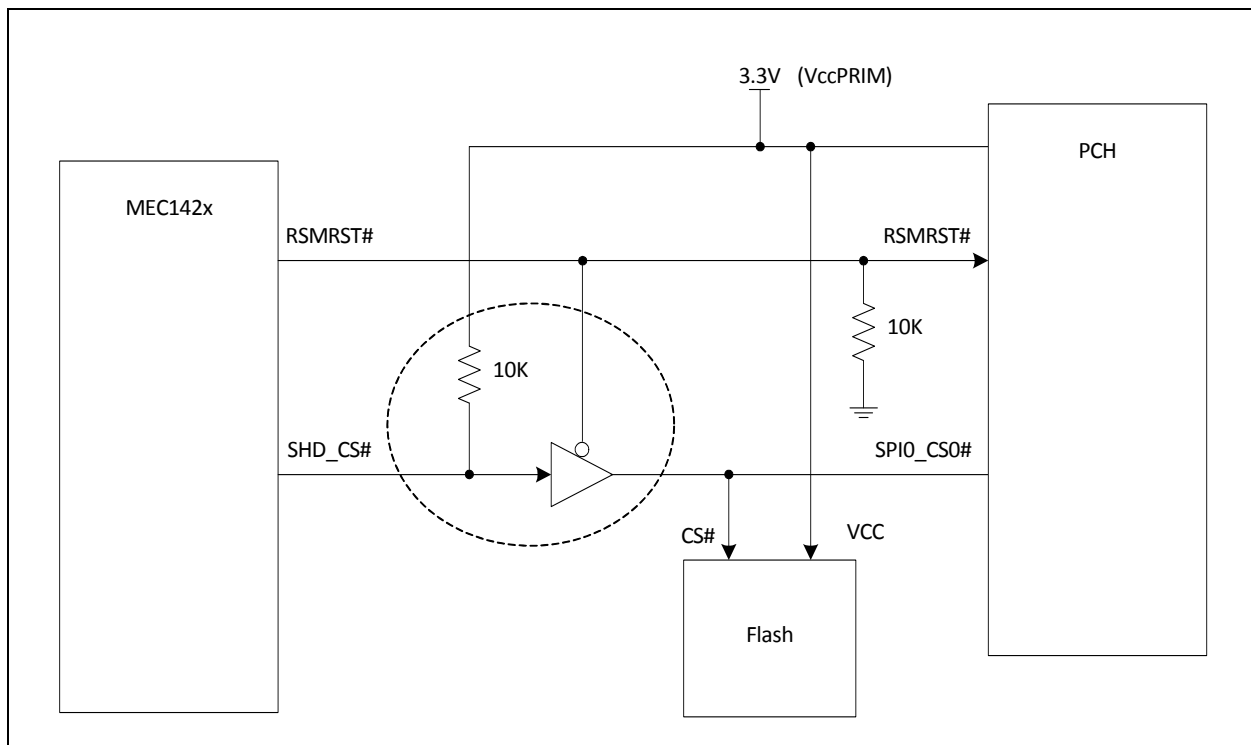
This requirement is due to the following information in the current Intel PCH device specification regarding the SPI0\_CS0# pin:

SPI0\_CS0# is pulled low instead of high (internally in the PCH).

The “pull” strength is about 1K ohms.

One example of a recommended isolation circuit requires an external tri-state buffer, so that the pull-up for the strap can be of reasonable strength. One possible buffer is the 74LVC1G125 which has a small propagation delay that will not impact the timing of the existing Boot ROM code.

The buffer and pull-up on the SHD\_CS# pin is shown in the figure below.



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**APPENDIX A: APPLICATION NOTE REVISION HISTORY****TABLE A-1: REVISION HISTORY**

Revision	Section/Figure/Entry	Correction
DS00002407B (03-09-18)	<a href="#">ADC Input Layout Requirement for Regular Sampling on page 13</a>	Section modified, Figure 9, "ADC Input Low Pass Filter" updated
	Added new section - <a href="#">MEC142x Shared SPI Flash Isolation Requirement on page 28</a>	
DS00002407A (03-20-17)	All	Initial Release

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