TC1044S

Charge Pump DC-to-DC Voltage Converter

Features

- Converts +5V Logic Supply to ±5V System
- Wide Input Voltage Range (1.5V to 12V)
- Efficient Voltage Conversion (99.9%)
- Excellent Power Efficiency (98%)
- Low Power Consumption 80 µA @ V_{IN} = 5V
- Low Cost and Easy to Use – Only Two External Capacitors Required
- RS-232 Negative Power Supply
- Available in 8-Pin Small Outline (SOIC) and 8-Pin Plastic DIP Packages
- Improved ESD Protection up to 10 kV
- No External Diode Required for High Voltage Operation
- Frequency Boost Raises F_{OSC} to 45 kHz

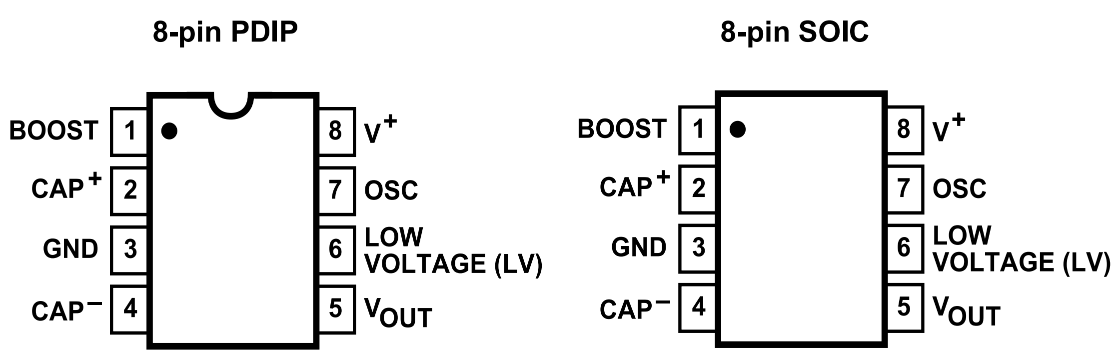
General Description

The TC1044S is a pin-compatible upgrade to the Industry standard TC7660 charge pump voltage converter. It converts a +1.5V to +12V input to a corresponding –1.5V to –12V output using only two low cost capacitors, eliminating inductors and their associated cost, size and EMI. Added features include an extended supply range to 12V, and a frequency boost pin for higher operating frequency, allowing the use of smaller external capacitors.

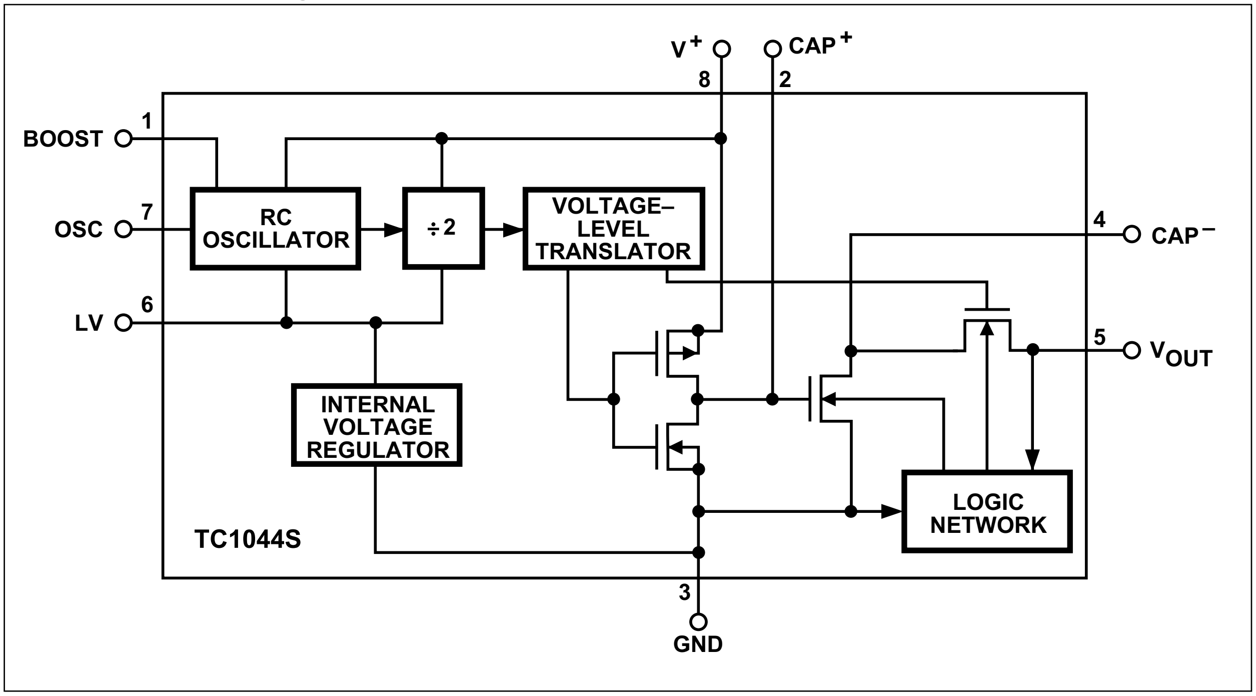
The on-board oscillator operates at a nominal frequency of 10 kHz. Frequency is increased to 45 kHz when pin 1 is connected to V^+. Operation below 10 kHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground (with pin 1 open).

The TC1044S is available in both 8-pin DIP and 8-pin small outline (SOIC) packages in commercial and extended temperature ranges.

Package Types



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage .... +13V
LV, Boost and OSC Inputs
Voltage (Note 1)........ –0.3V to (V^+ + 0.3V) for V^+ < 5.5V
.... (V^+ –5.5V) to (V^+ + 0.3V) for V^+ > 5.5V
Current Into LV (Note 1) .... 20 µA for V^+ > 3.5V
Output Short Duration (V_{SUPPLY} ≤ 5.5V)........ Continuous
Lead Temperature (Soldering, 10 sec)........ +300°C
Package Power Dissipation (T_A ≤ 70°C) (Note 1)
8-Pin Plastic DIP .... 730 mW
8-Pin SOIC .... 470 mW
Operating Temperature Range
C Suffix........ 0°C to +70°C
E Suffix........ –40°C to +85°C
Storage Temperature Range .... –65°C to +150°C

† Notice: Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = +25°C, V^+ = 5V, C_{OSC} = 0, Test Circuit (Figure 2-1), unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Current	I^+	—	80	160	µA	R_L = ∞
		—	—	180		0°C < T_A < +70°C
		—	—	180		–40°C < T_A < +85°C
		—	—	200		–55°C < T_A < +125°C
Supply Current (Boost Pin = V^+)	I^+	—	—	300	µA	0°C < T_A < +70°C
		—	—	350		–40°C < T_A < +85°C
		—	—	400		–55°C < T_A < +125°C
Supply Voltage Range, High	V^+_{H2}	3	—	12	V	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV Open
Supply Voltage Range, Low	V^+_{L2}	1.5	—	3.5	V	Min ≤ T_A ≤ Max, R_L = 10 kΩ, LV to GND
Output Source Resistance	R_{OUT}	—	60	100	Ω	I_{OUT} = 20 mA
		—	70	120		I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C
		—	70	120		I_{OUT} = 20 mA, –40°C ≤ T_A ≤ +85°C
		—	105	150		I_{OUT} = 20 mA, –55°C ≤ TA ≤ +125°C
		—	—	250	Ω	V^+ = 2V, I_{OUT} = 3 mA, LV to GND 0°C ≤ T_A ≤ +70°C
		—	—	400		–55°C ≤ T_A ≤ +125°C

Note 1: Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the TC1044S.
2: Derate linearly above 50°C by 5.5 mW/°C.
3: Switching frequency is one-half internal oscillator frequency.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: T_A = +25°C, V^+ = 5V, C_{OSC} = 0, Test Circuit (Figure 2-1), unless otherwise indicated.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Oscillator Frequency	F_{OSC}	—	10	—	kHz	Pin 7 open; Pin 1 open or GND
		—	45	—		Boost Pin = V^+
Switching Frequency (**Note 3**)	F_{SW}	—	5	—	kHz	Pin 7 open; Pin 1 open or GND
		—	22.5	—		Boost Pin = V^+
Power Efficiency	P_{EFF}	96	98	—	%	R_L = 5 kΩ; Boost Pin Open
		95	97	—		$T_{MIN} < T_A < T_{MAX}$; Boost Pin Open
		—	88	—		Boost Pin = V^+
Voltage Conversion Efficiency	$V_{OUT}E_{FF}$	99	99.9	—	%	$R_L = \infty$
Oscillator Impedance	Z_{OSC}	—	1	—	MΩ	V^+ = 2V
		—	100	—	kΩ	V^+ = 5V

Note 1: Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TC1044S.

2: Derate linearly above 50°C by 5.5 mW/°C.

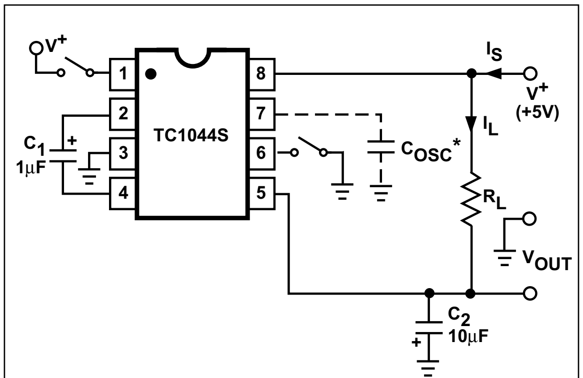
3: Switching frequency is one-half internal oscillator frequency.

2.0 CIRCUIT DESCRIPTION

The TC1044S contains all the necessary circuitry to implement a voltage inverter, with the exception of two external capacitors, which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 2-2, which shows an idealized voltage inverter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The four switches in Figure 2-2 are MOS power switches; S_1 is a P-channel device, and S_2, S_3, and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the TC1044S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.



***NOTE:** For large values of C_{OSC} (>1000 pF), the values of C_1 and C_2 should be increased to 100 µF.

FIGURE 2-1: *TC1044S Test Circuit.*

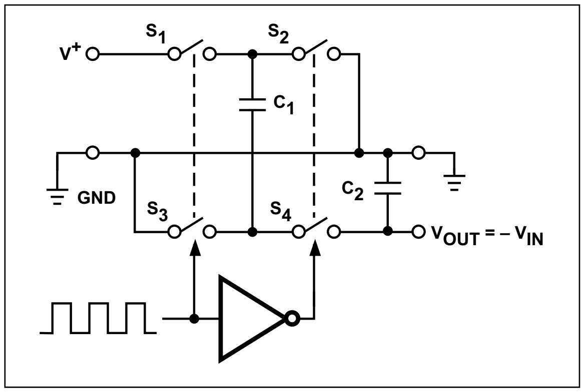


FIGURE 2-2: *Idealized Charge Pump Inverter.*

The voltage regulator portion of the TC1044S is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the “LV” pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

2.1 Theoretical Power Efficiency Considerations

In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TC1044S approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs. The energy lost is defined by:

EQUATION 2-1:

$$E = \frac{1}{2}C_1(V_1^2 - V_2^2)$$

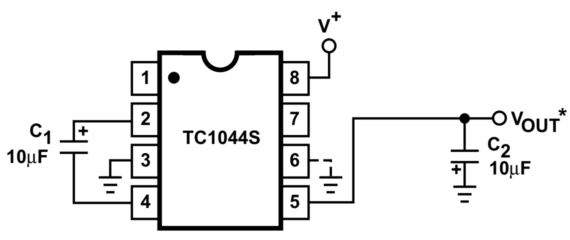
V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2-2) compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

2.2 Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V^+ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the TC1044S and the + terminal of C_2 must be connected to GND.

2.3 Simple Negative Voltage Converter

Figure 2-3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.



*NOTE: $V_{OUT} = -V^+$ for $1.5V \le V^+ \le 12V$

FIGURE 2-3: *Simple Negative Converter.*

The output characteristics of the circuit in Figure 2-3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of –10 mA and a supply voltage of +5V, the output voltage would be –4.3V.

The dynamic output impedance of the TC1044S is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only ½ of the cycle, the equation is:

EQUATION 2-2:

$$X_C = \frac{2}{2\pi f \cdot C_1} = 3.18\Omega$$

Where:

f = 10 kHz

C_1 = 10 µF

2.4 Paralleling Devices

Any number of TC1044S voltage converters may be paralleled to reduce output resistance (Figure 2-4). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

EQUATION 2-3:

$$R_{OUT} = \frac{R_{OUT}(of\ TC1044S)}{n(number\ of\ devices)}$$

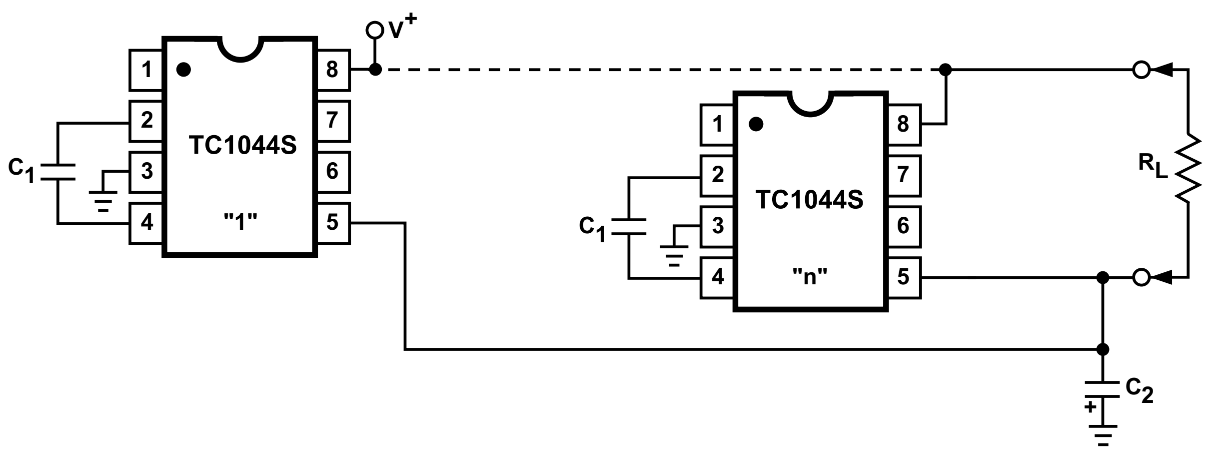


FIGURE 2-4: *Paralleling Devices Lowers Output Impedance.*

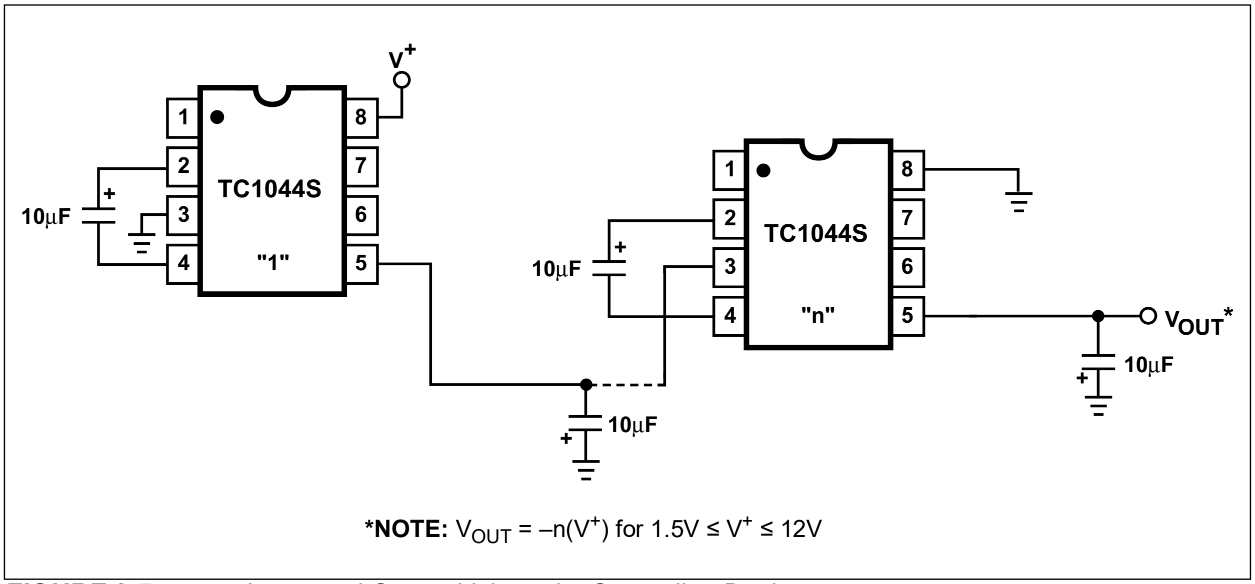


FIGURE 2-5: Increased Output Voltage by Cascading Devices.

2.5 Cascading Devices

The TC1044S may be cascaded as shown (Figure 2-5) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

EQUATION 2-4:

$$V_{OUT} = -n(V_{IN})$$

Where *n* is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TC1044S R_{OUT} values.

2.6 Changing the TC1044S Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, frequency boost pin may be connected to V^+ to increase oscillator frequency to 45 kHz from a nominal of 10 kHz for an input supply voltage of 5.0 volts. The oscillator may also be synchronized to an external clock as shown in Figure 2-6. In order to prevent possible device latch-up, a 1 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

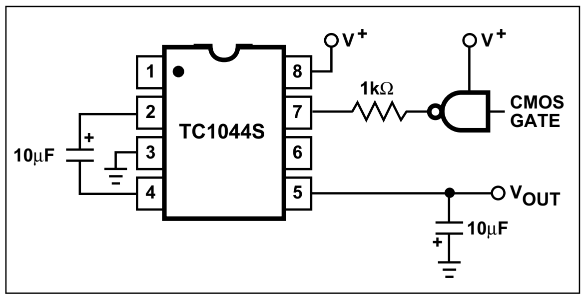


FIGURE 2-6: External Clocking.

It is also possible to increase the conversion efficiency of the TC1044S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 2-7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 µF to 100 µF).

2.7 Positive Voltage Multiplication

The TC1044S may be employed to achieve positive voltage multiplication using the circuit shown in Figure 2-8. In this application, the pump inverter switches of the TC1044S are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage

(V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) – (2V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60Ω.

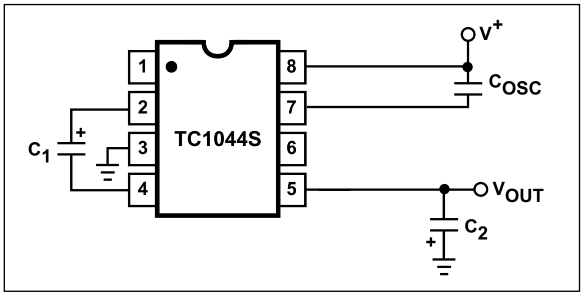


FIGURE 2-7: *Lowering Oscillator Frequency.*

2.8 Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 2-9 combines the functions shown in Figure 2-3 and Figure 2-8 to simultaneously provide negative voltage conversion and positive voltage multiplication. This approach would be, for example, suitable for generating +9V and –5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

2.9 Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 2-10 shows a TC1044S transforming –5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switchdrive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 2-9, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 2-9 would never turn ON), or else the diode and resistor shown dotted in Figure 2-10 can be used to “force” the internal regulator ON.

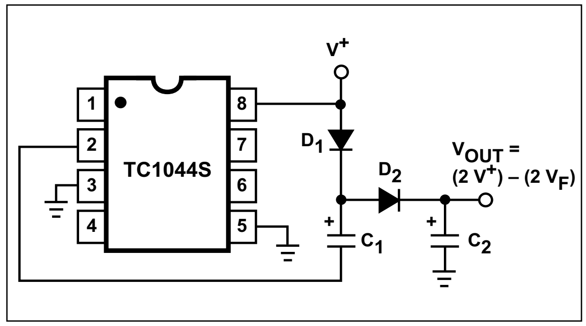


FIGURE 2-8: *Positive Voltage Multiplier.*

2.10 Voltage Splitting

The same bidirectional characteristics used in Figure 2-10 can also be used to split a higher supply in half, as shown in Figure 2-11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 2-5, +15V can be converted (via +7.5V and –7.5V) to a nominal –15V, though with rather high series resistance (~250Ω).

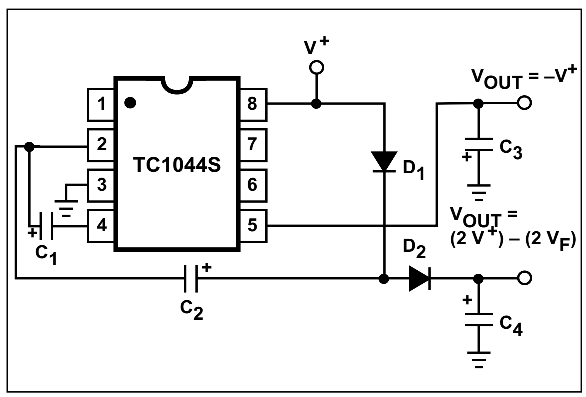


FIGURE 2-9: *Combined Negative Converter and Positive Multiplier.*

2.11 Negative Voltage Generation for Display ADCs

The TC7106 is designed to work from a 9V battery. With a fixed power supply system, the TC7106 will perform conversions with input signal referenced to power supply ground.

2.12 Negative Supply Generation for 4½ Digit Data Acquisition System

The TC7135 is a 4½ digit ADC operating from ±5V supplies. The TC1044S provides an inexpensive –5V source. (See AN16 and AN17 for TC7135 interface details and software routines.)

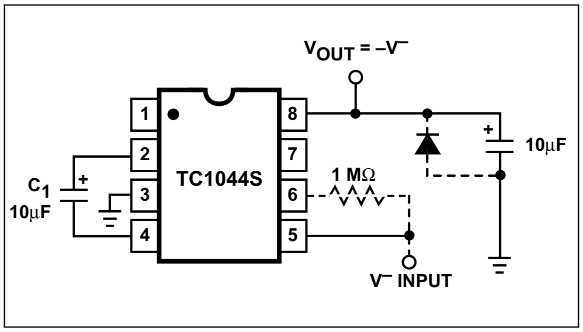


FIGURE 2-10: *Positive Voltage Conversion.*

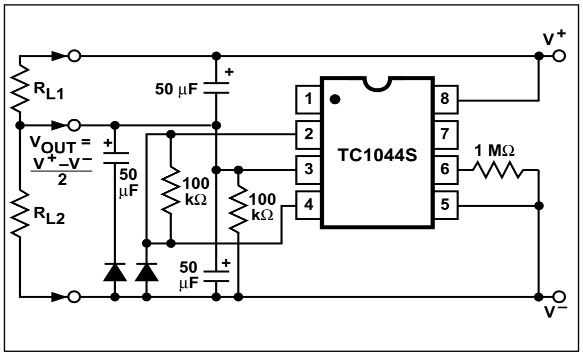


FIGURE 2-11: *Splitting a Supply in Half.*

3.0 TYPICAL CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

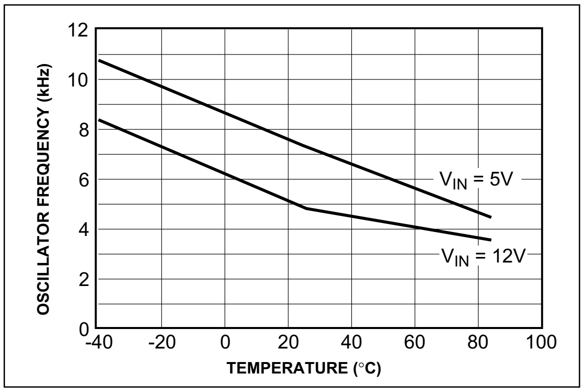


FIGURE 3-1: *Unloaded Oscillator Frequency vs. Temperature.*

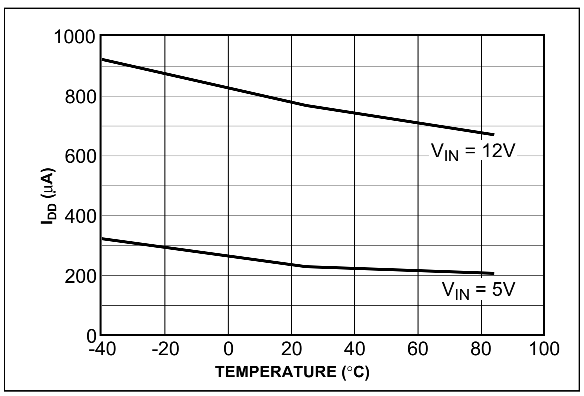


FIGURE 3-2: *Supply Current vs. Temperature (with Boost Pin = V_{IN}).*

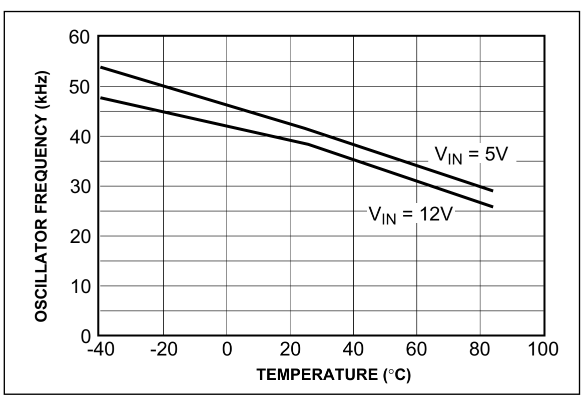


FIGURE 3-3: *Unloaded Oscillator Frequency vs. Temperature (with Boost Pin = V_{IN}).*

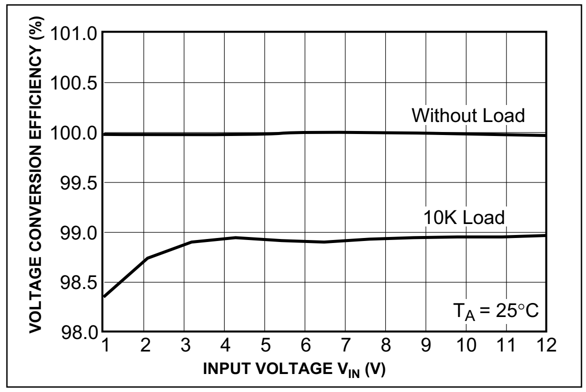


FIGURE 3-4: *Voltage Conversion.*

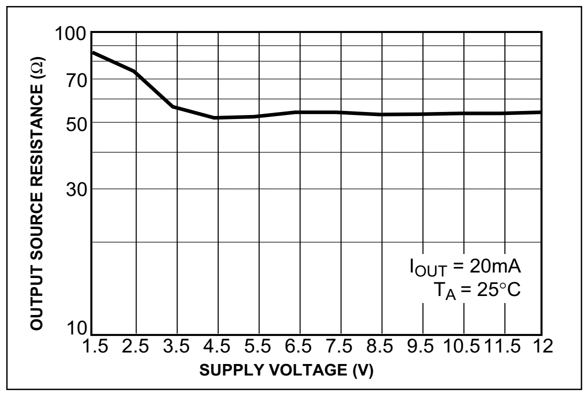


FIGURE 3-5: *Output Source Resistance vs. Supply Voltage.*

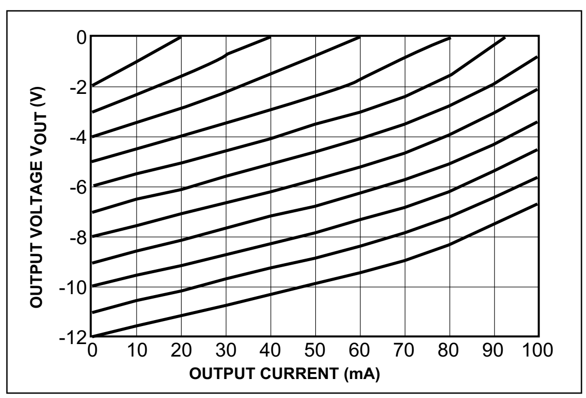


FIGURE 3-6: *Output Voltage vs. Output Current.*

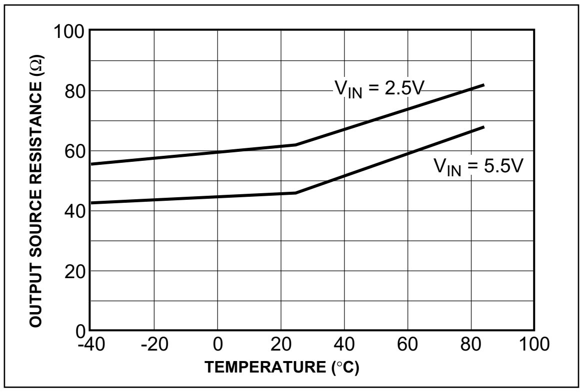


FIGURE 3-7: *Output Source Resistance vs. Temperature.*

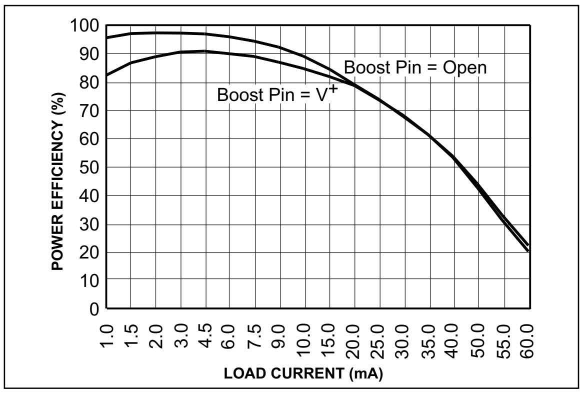


FIGURE 3-8: *Power Conversion Efficiency vs. Load.*

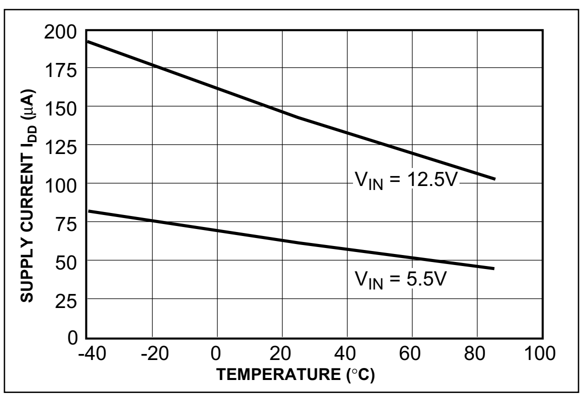
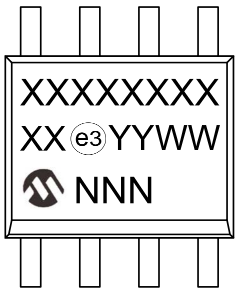


FIGURE 3-9: *Supply Current vs. Temperature.*

4.0 PACKAGING INFORMATION

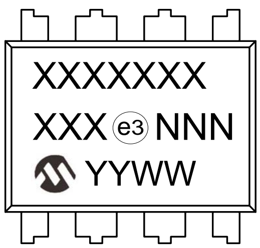
4.1 Package Marking Information

8-Pin SOIC*

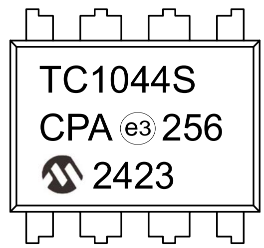


Example

8-Pin PDIP*



Example

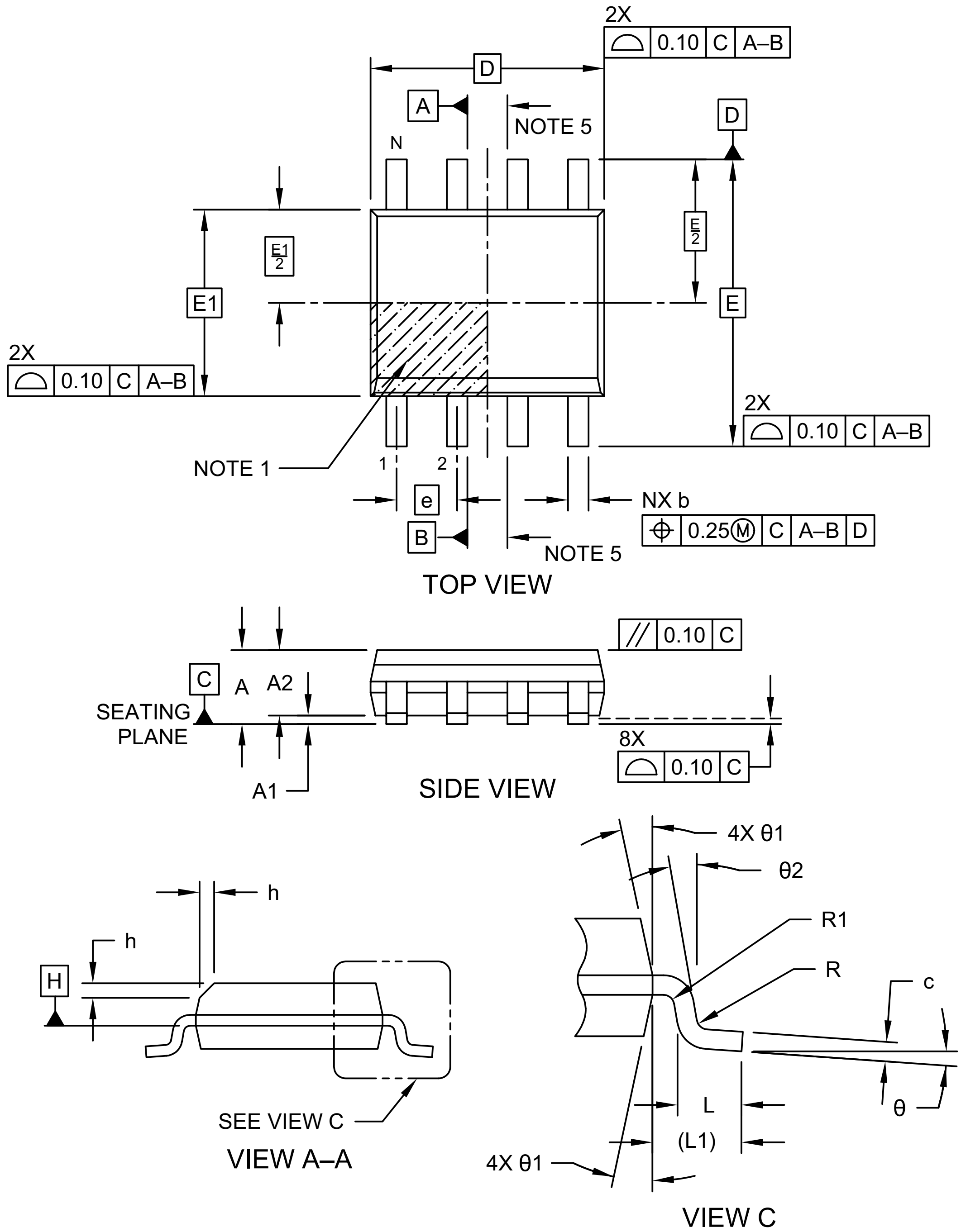


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

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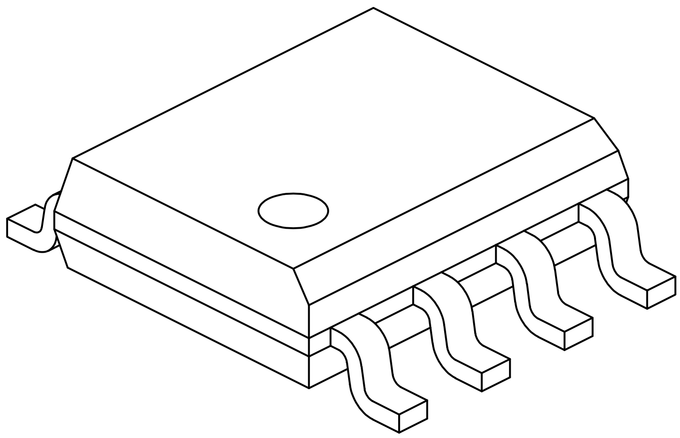


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

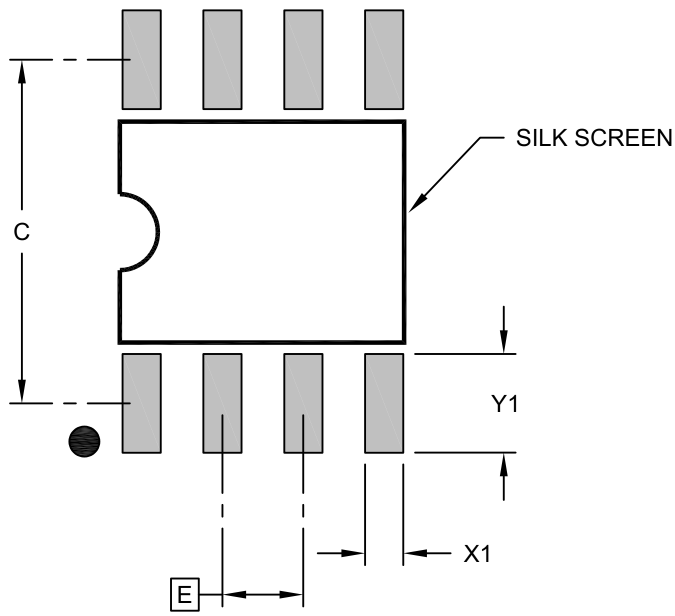
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

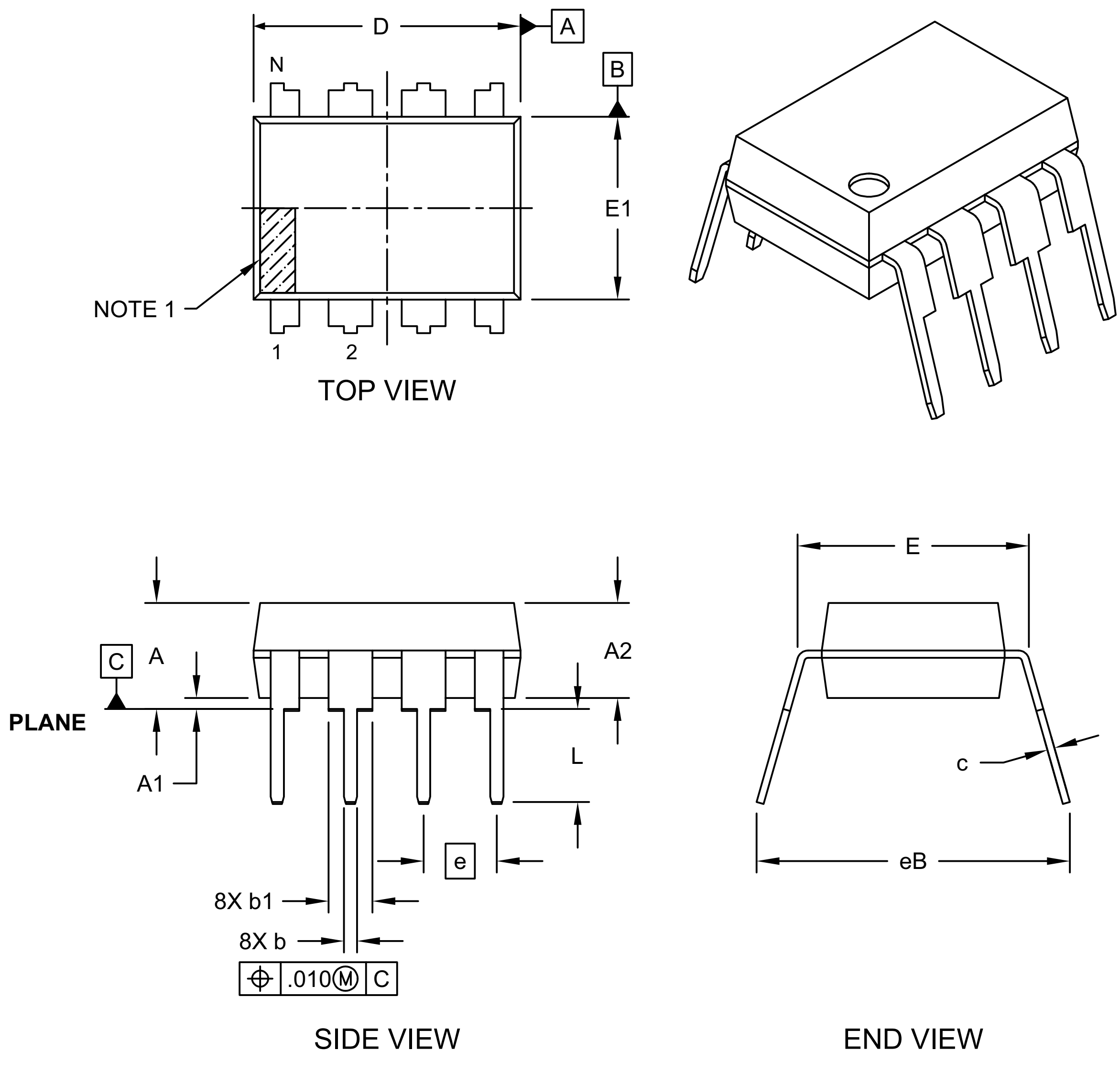
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP]
Atmel Legacy Package

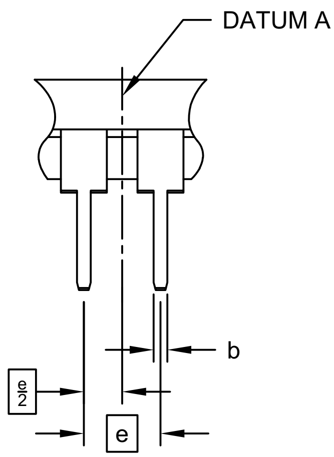
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



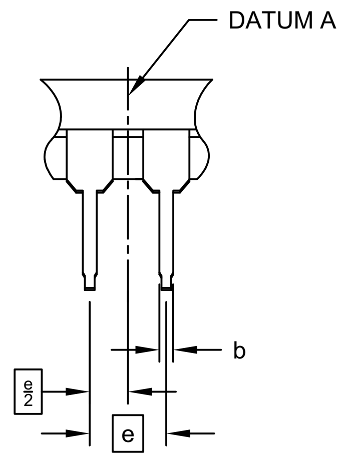
Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 1 of 2

8-Lead Plastic Dual In-Line (C4X) - 300 mil Body [PDIP]
Atmel Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



ALTERNATE LEAD DESIGN
(NOTE 5)



	Units	INCHES		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-C4X Rev G Sheet 2 of 2

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (March 2025)

- Added parameter “Switching Frequency” to **Table “Electrical Characteristics”**.
- Updated the Package Outline Drawings and Package Marking Information in **Section 4.0 “Packaging Information”**.
- Added **Section “Product Identification System”**.
- Added **Appendix A: “Revision History”**.
- Minor changes throughout the text.

Revision A (2001)

- Initial release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	XXX
Device	Operating Temperature Range	Package Options	Media Type

Device:	TC1044S	=	Charge Pump DC-to-DC Voltage Converter
Temperature Range:	C	=	0°C to +70°C
	E	=	–40°C to +85°C (Extended)
Packages:	PA	=	8-pin PDIP, Lead (Pb)-free/RoHS-compliant Package
	OA	=	8-pin SOIC, Lead (Pb)-free/RoHS-compliant Package
Media Type:	Blank	=	Tube, 60 per Tube (PDIP option only)
	Blank	=	Tube, 100 per Tube (SOIC option only)
	713	=	Tape and Reel, 3300 per Reel

Examples:

a) TC1044SCPA: Charge Pump DC-to-DC Voltage Converter, 0°C to +70°C Operating Temp. Range, 8-pin PDIP, Lead (Pb)-free/RoHS-compliant Package, 60 per Tube

b) TC1044SCOA: Charge Pump DC-to-DC Voltage Converter, 0°C to +70°C Operating Temp. Range, 8-pin SOIC, Lead (Pb)-free/RoHS-compliant Package, 100 per Tube

c) TC1044SEOA: Charge Pump DC-to-DC Voltage Converter, –40°C to +85°C Operating Temp. Range, 8-pin SOIC, Lead (Pb)-free/RoHS-compliant Package, 100 per Tube

d) TC1044SEPA: Charge Pump DC-to-DC Voltage Converter, –40°C to +85°C Operating Temp. Range, 8-pin PDIP, Lead (Pb)-free/RoHS-compliant Package, 60 per Tube

e) TC1044SEOA713: Charge Pump DC-to-DC Voltage Converter, –40°C to +85°C Operating Temp. Range, 8-pin SOIC, Lead (Pb)-free/RoHS-compliant Package, 3300 per Reel

f) TC1044SCOA713: Charge Pump DC-to-DC Voltage Converter, 0°C to +70°C Operating Temp. Range, 8-pin SOIC, Lead (Pb)-free/RoHS-compliant Package, 3300 per Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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