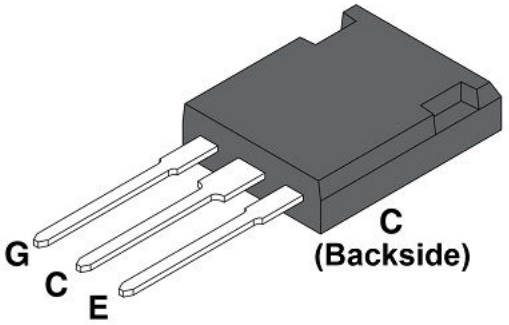
1200 V, 35 A Power MOS 7™ PT IGBT with SiC Diode

APT35GP120B2SC20

Product Overview

1200 V, 22 A at 100 kHz Power MOS 7 punch-through (PT) IGBT with co-packaged, anti-parallel SiC diode, T-MAX®



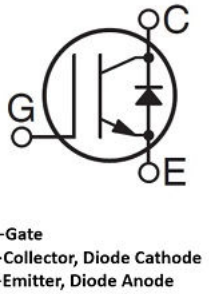


Table 1. Ordering Information

Catalog Part Number (CPN)	Package	Packing Media	Qualification
APT35GP120B2SC20	T-MAX	Tube	Industrial

Features

- Low conduction loss and saturation voltage
- Low gate charge
- Ultrafast tail current shutoff
- No reverse recovery
- High operating frequency
- Reverse-bias safe operating area (RBSOA) rated
- RoHS compliant
- Zero E_{on} switching loss from co-packaged, anti-parallel diode

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1. Device Specifications: IGBT

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device. T_C = 25 °C unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{CES}	Collector-emitter voltage	1200	V
V_{GE}	Gate-emitter voltage	±30	
I_{C1}	Continuous collector current (T_C = 25 °C)	96	A
I_{C2}	Continuous collector current (T_C = 110 °C)	46	
I_{CM}	Pulsed collector current[1] (T_C = 150 °C)	140	
RBSOA	Reverse-bias safe operating area (T_J = 150 °C, 960 V)	140	A
P_D	Total power dissipation	543	W

Note:

1. Repetitive rating: Pulse width and case temperature are limited by the maximum junction temperature.

1.2 Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$R_{\Theta JC}$	Junction-to-case thermal resistance (IGBT)		0.21	0.23	°C/W
$R_{\Theta JC}$	Junction-to-case thermal resistance (diode)		0.65	0.95	
T_J, T_{STG}	Operating and storage junction temperature	–55		150	°C
T_L	Lead temperature for 10 seconds			300	
Wt	Package weight		6.2		g

1.3 Electrical Performance

The following table shows the static characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	V_{GE} = 0 V, I_C = 450 µA	1200			V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	3	4.5	6	
$V_{CE(on)}$	Collector-emitter on voltage	V_{GE} = 15 V, I_C = 35 A		3.3	3.9	
		V_{GE} = 15 V, I_C = 35 A, T_J = 125 °C		3.0		
I_{CES}	Collector cut-off current[1]	V_{CE} = 1200 V, V_{GE} = 0 V			450	µA
		V_{CE} = 1200 V, V_{GE} = 0 V, T_J = 125 °C			3000	
I_{GES}	Gate-emitter leakage current	V_{GE} = ±20 V			±100	nA

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Note:

1. I_{CES} includes both IGBT and diode leakages.

The following table shows the dynamic characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{GE} = 0 V, V_{CE} = 25 V, ƒ = 200 kHz		2433		pF
C_{res}	Reverse transfer capacitance			39		
C_{oes}	Output capacitance			564		
V_{GEP}	Gate-to-emitter plateau voltage	V_{GE} = 15 V, V_{CE} = 600 V, I_C = 25 A		7.5		V
Q_G	Total gate charge[1]			150		nC
Q_{GE}	Gate-emitter charge			21		
Q_{GC}	Gate-collector ("Miller") charge			60		
RBSOA	Reverse-bias safe operating area	T_J = 150 °C, R_G = 5 Ω, V_{GE} = 15 V, V_{CE} = 960 V, L = 100 µH	140			A
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, V_{GE} =15 V, I_C = 35 A, R_G = 4.3 Ω, T_J = 25 °C		16		ns
t_r	Current rise time			20		
$t_{d(off)}$	Turn-off delay time			95		
t_f	Current fall time			40		
E_{on}	Turn-on switching energy[2]			750		µJ
E_{off}	Turn-off switching energy[3]			680		
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, V_{GE} = 15 V, I_C = 25 A, R_G = 5 Ω, T_J = 125 °C		16		ns
t_r	Current rise time			20		
$t_{d(off)}$	Turn-off delay time			145		
t_f	Current fall time			75		
E_{on}	Turn-on switching energy[2]			750		µJ
E_{off}	Turn-off switching energy[3]			1745		

Notes:

1. See MIL-STD-750 Method 3471.
2. E_{on} is the clamped inductive turn-on-energy of this device; there is no contribution to E_{on} from the SiC diode. (See Figures 1-22, 1-23.)
3. E_{off} is the clamped inductive turn-off energy measured in accordance with JEDEC standard JESD24-1. (See Figures 1-22, 1-24.)

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1.4 Typical Performance Curves: IGBT

Data for performance curves are characterized, not 100% tested.

Figure 1-1. Output Characteristics

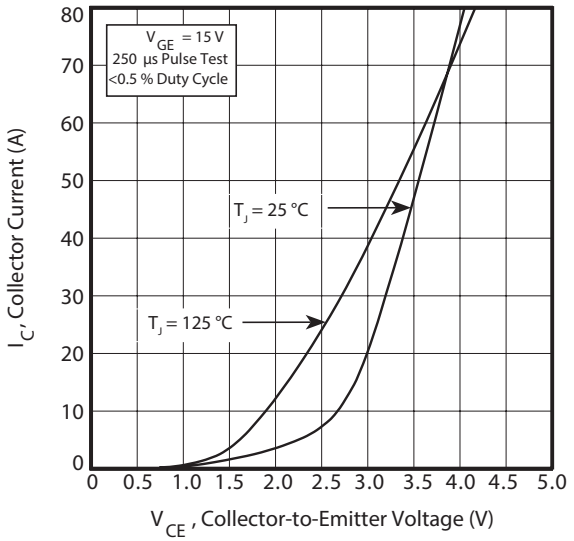

Figure 1-2. Output Characteristics

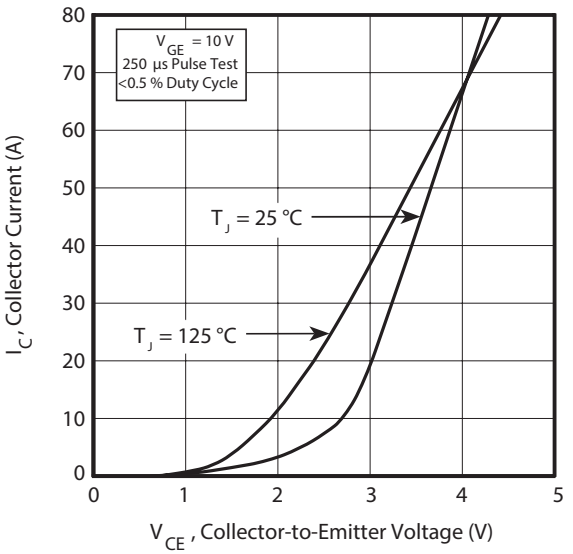

Figure 1-3. Transfer Characteristics

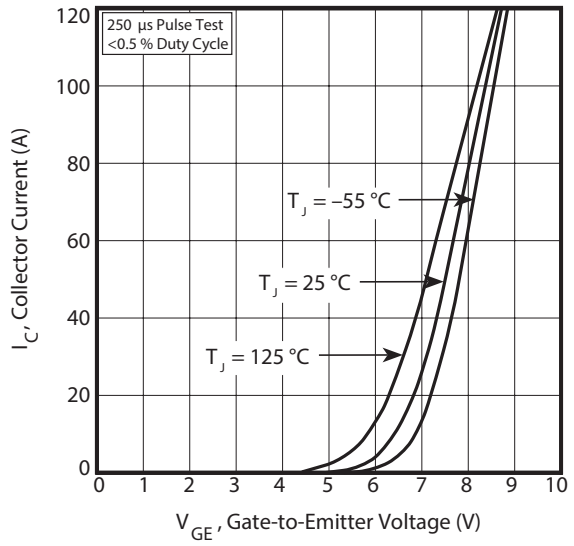

Figure 1-4. Gate Charge

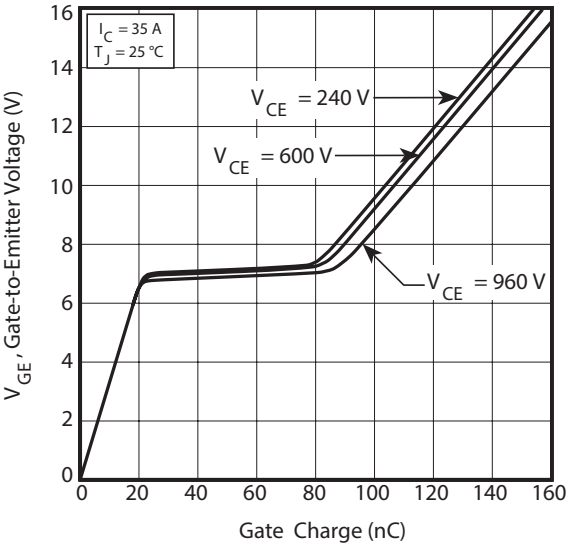

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Figure 1-5. On-State Voltage vs. Gate-to-Emitter Voltage

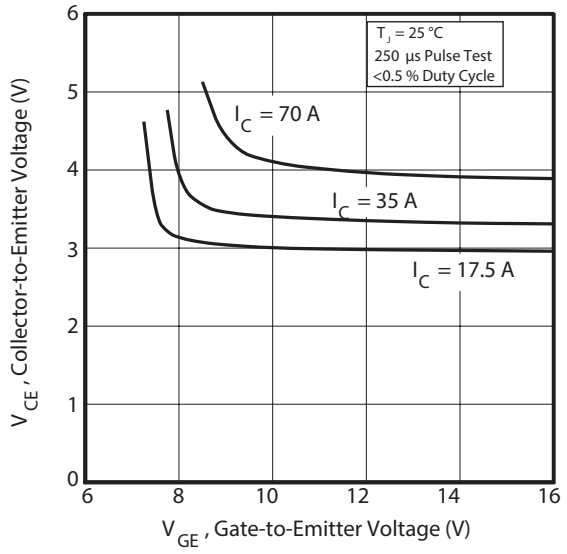

Figure 1-6. On-State Voltage vs. Junction Temperature

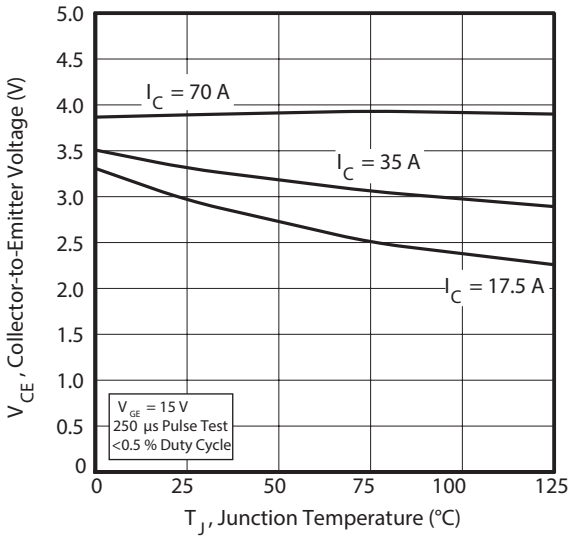

Figure 1-7. Breakdown Voltage vs. Junction Temperature

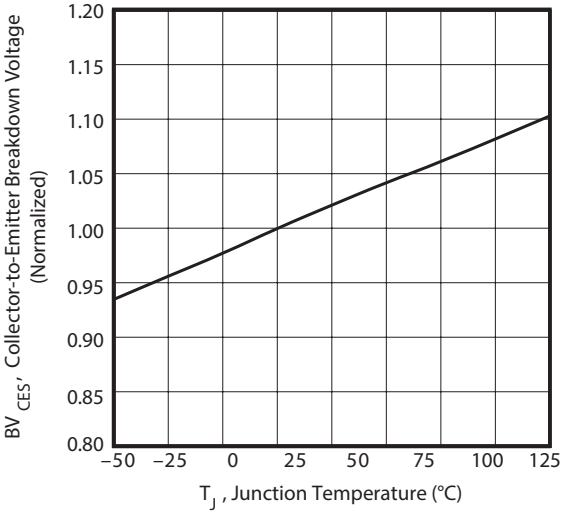

Figure 1-8. DC Collector Current vs. Case Temperature

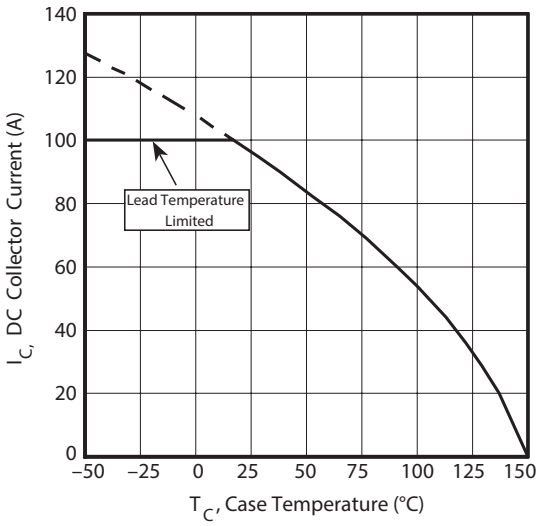

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Figure 1-9. Turn-On Delay Time vs. Collector Current

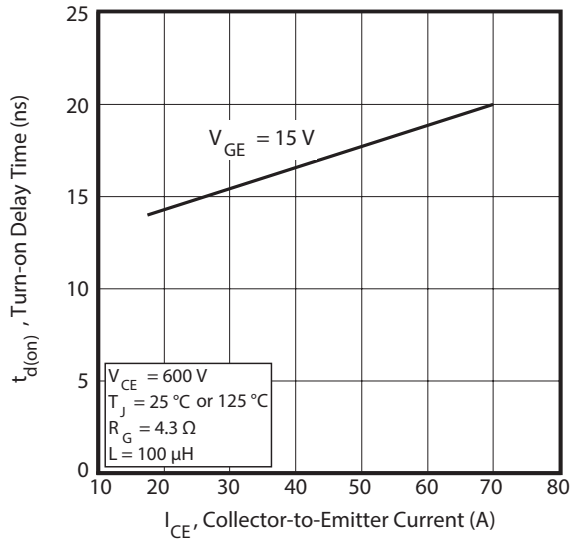

Figure 1-10. Turn-Off Delay Time vs. Collector Current

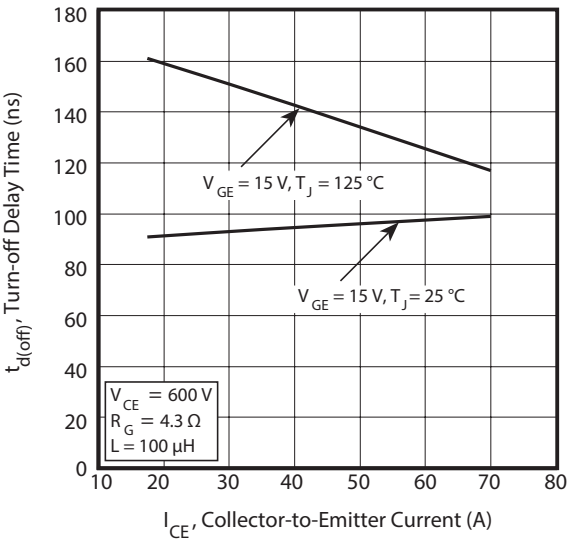

Figure 1-11. Current Rise Time vs. Collector Current

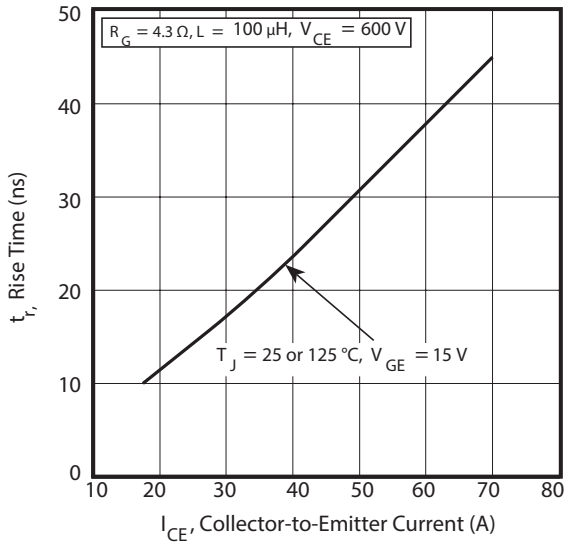

Figure 1-12. Current Fall Time vs. Collector Current

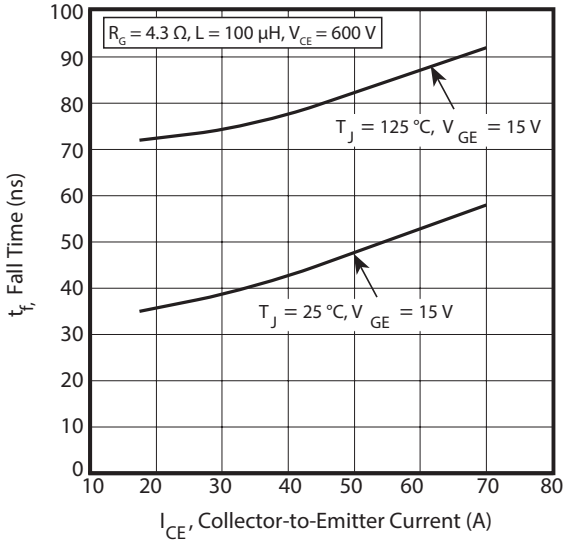

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Figure 1-13. Turn-On Energy Loss vs. Collector Current

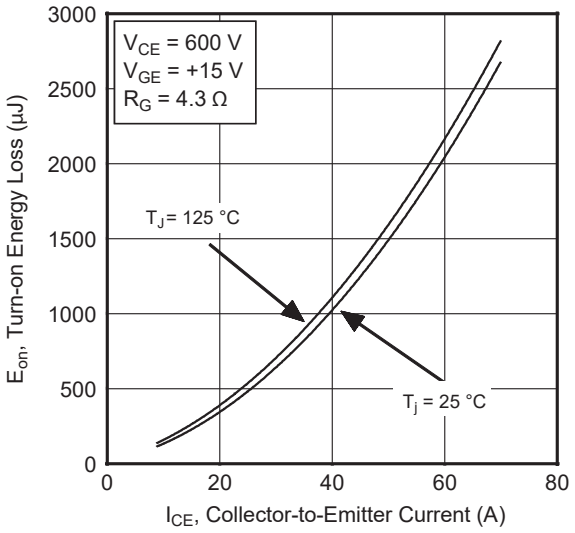

Figure 1-14. Turn-Off Energy Loss vs. Collector Current

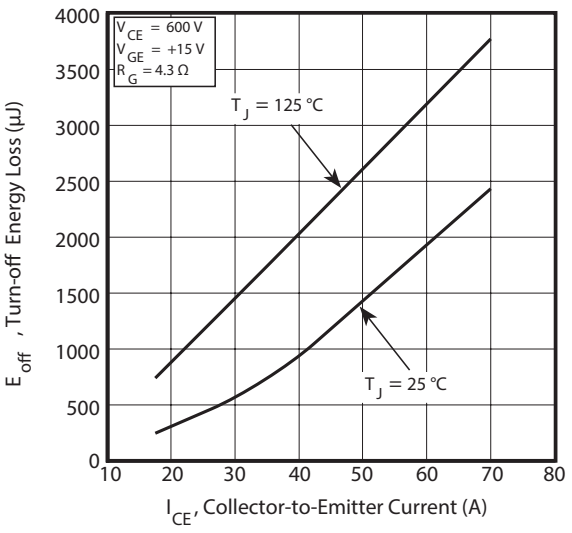

Figure 1-15. Switching Energy Losses vs. Gate Resistance

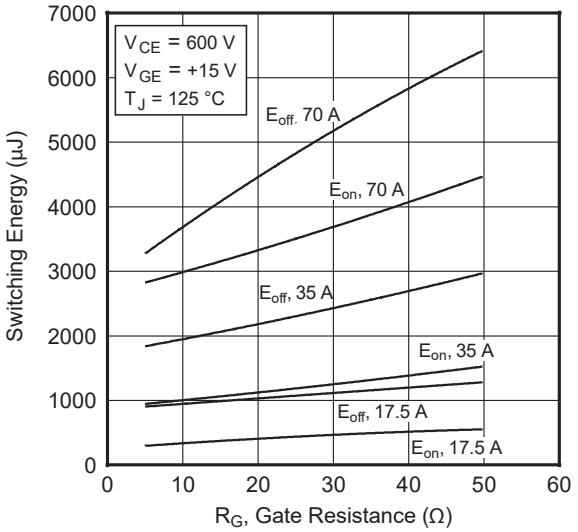

Figure 1-16. Switching Energy Losses vs. Junction Temperature

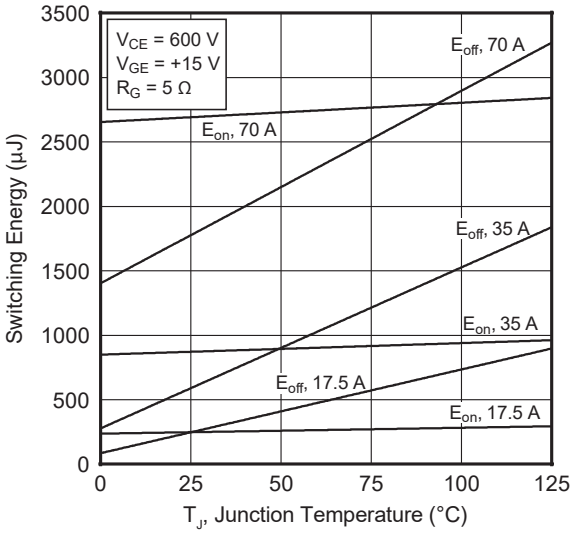

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Figure 1-17. Capacitance vs. Collector-To-Emitter Voltage

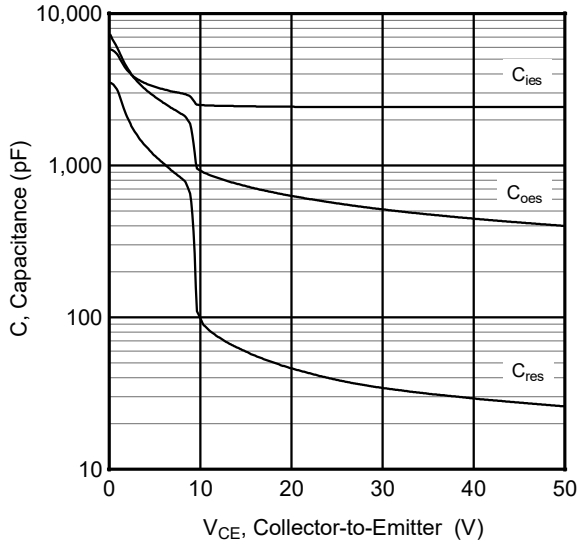

Figure 1-18. Reverse-bias Safe Operating Area

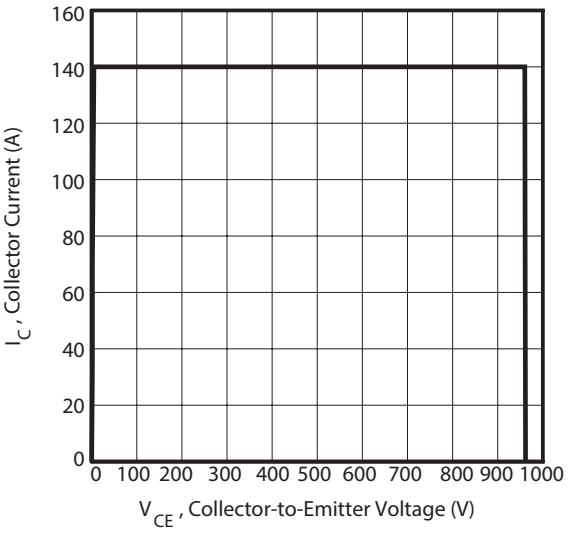

Figure 1-19. Maximum Transient Thermal Impedance

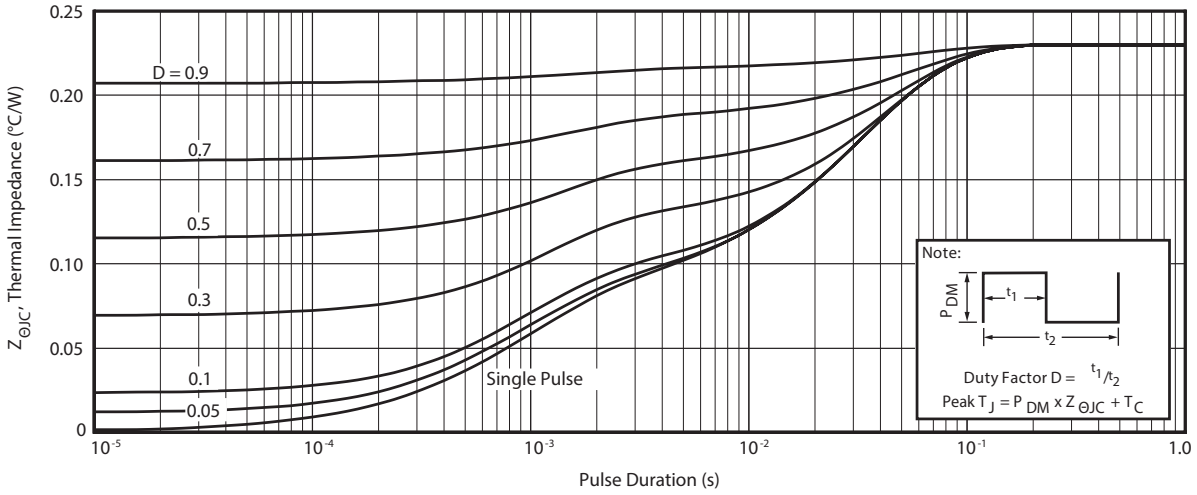

Figure 1-20. Transient Thermal Impedance Model

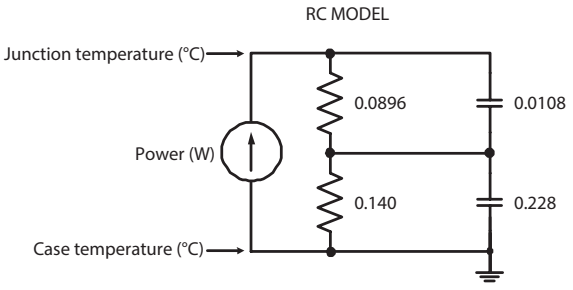

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Figure 1-21. Operating Frequency vs. Collector Current

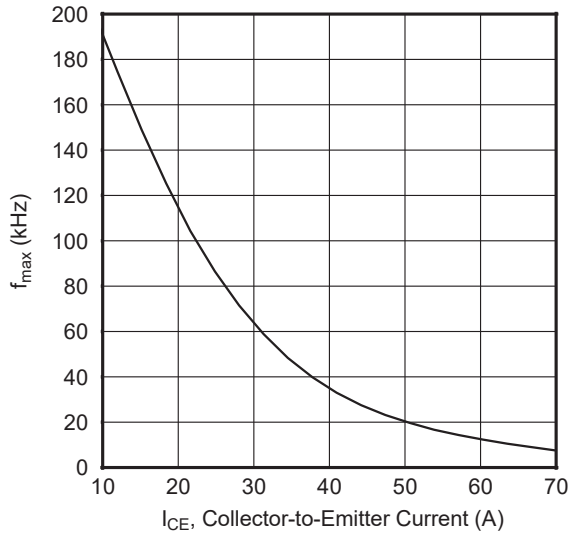


Figure 1-22. Inductive Switching Test Circuit

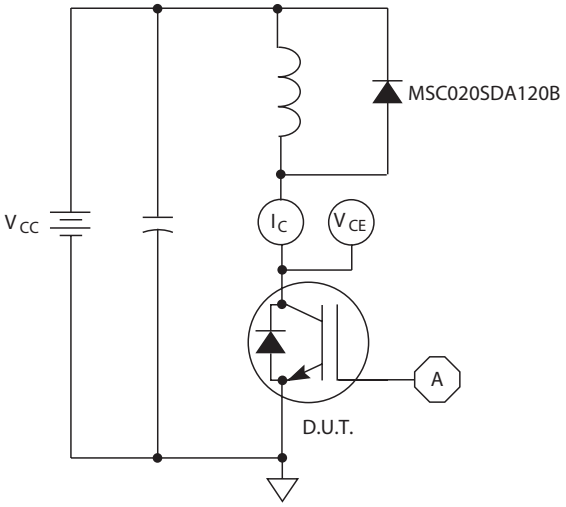


Figure 1-23. Turn-on Switching Waveforms and Definitions

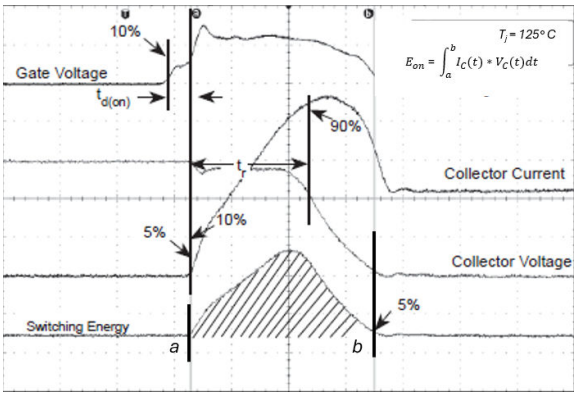
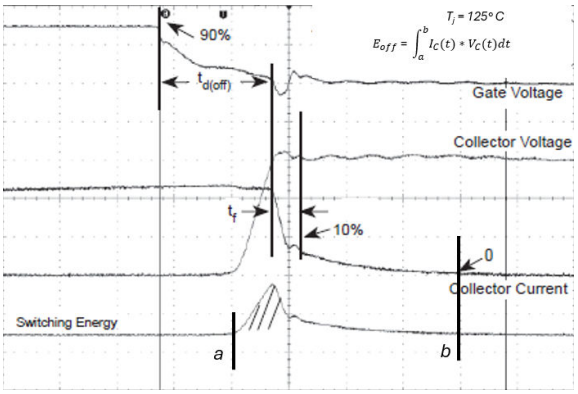


Figure 1-24. Turn-off Switching Waveforms and Definitions



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2. Device Specifications: Zero-Recovery SiC Anti-Parallel Diode

This section shows the specifications of the co-packaged, anti-parallel diode.

2.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the anti-parallel diode. T_C = 25 °C unless otherwise specified.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_F	Maximum DC forward current (T_C = 25 °C)	49	A
	Maximum DC forward current (T_C = 135 °C)	22	
	Maximum DC forward current (T_C = 145 °C)	18	
I_{FRM}	Repetitive peak forward surge current (t_p = 8.3 ms, half sine wave)	64	
I_{FSM}	Non-repetitive forward surge current (t_p = 8.3 ms, half sine wave)	115	
P_{TOT}	Total power dissipation (T_C = 25 °C)	186	W
	Total power dissipation (T_C = 110 °C)	80	

2.2 Electrical Performance

The following table shows the static characteristics of the anti-parallel diode.

Table 2-2. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
V_F	Forward voltage	I_F = 20 A, T_C = 25 °C		1.5	1.8	V
		I_F = 20 A, T_C = 175 °C		2.0		

2.3 Typical Performance Curves

Data for performance curves are characterized, not 100% tested.

Figure 2-1. Maximum Transient Thermal Impedance

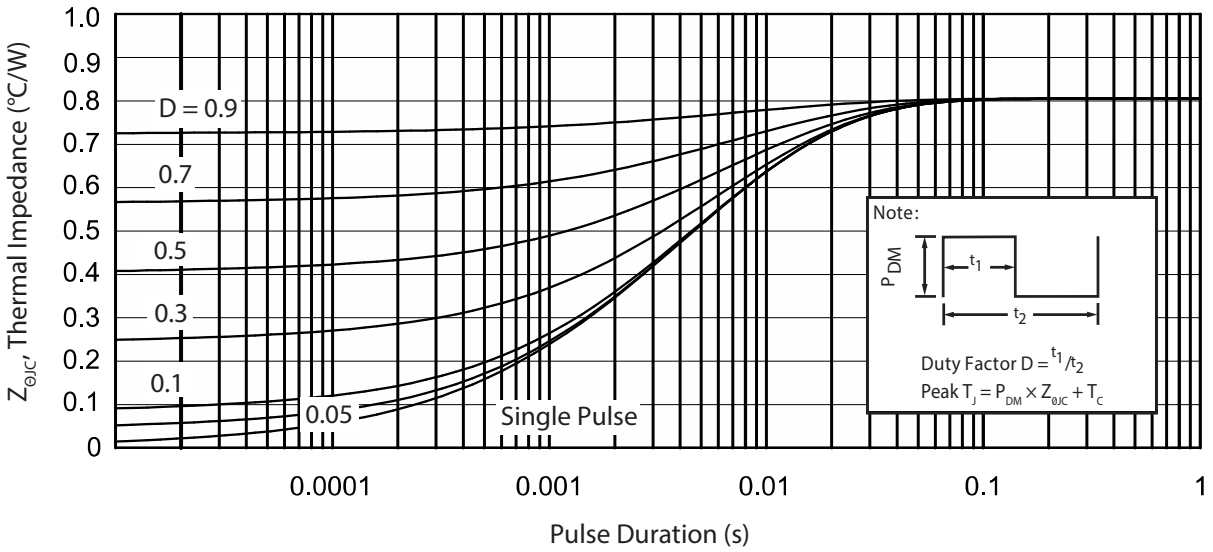

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Figure 2-2. Forward Current vs. Forward Voltage

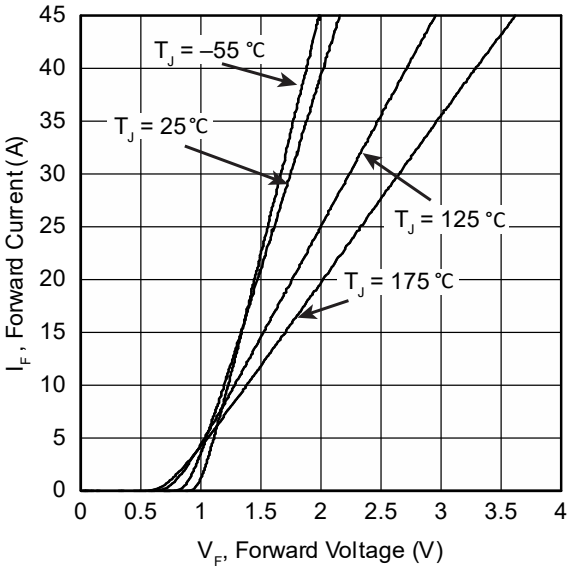


Figure 2-3. Max. Forward Current vs. Case Temp.

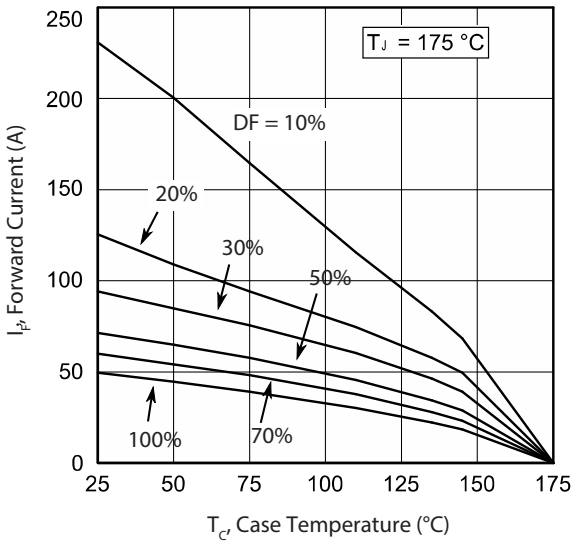


Figure 2-4. Max. Power Dissipation vs. Case Temp.

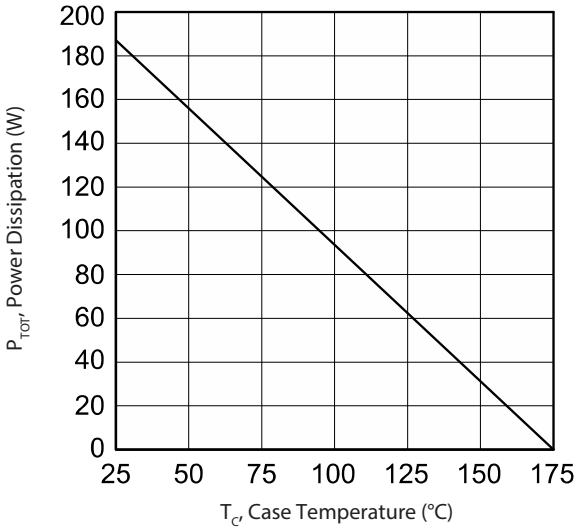
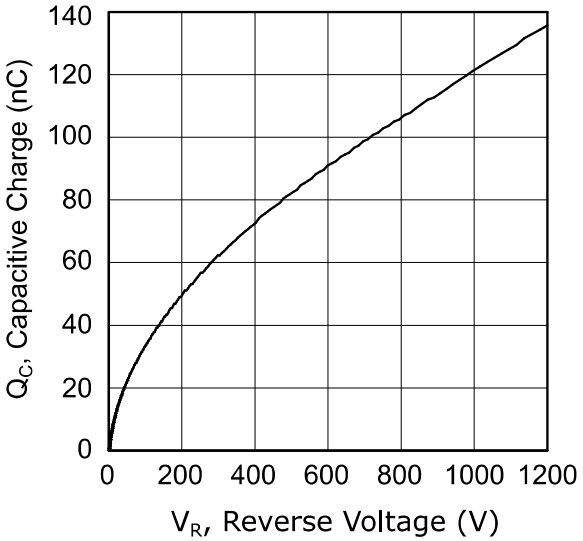


Figure 2-5. Total Capacitive Charge vs. Reverse Voltage



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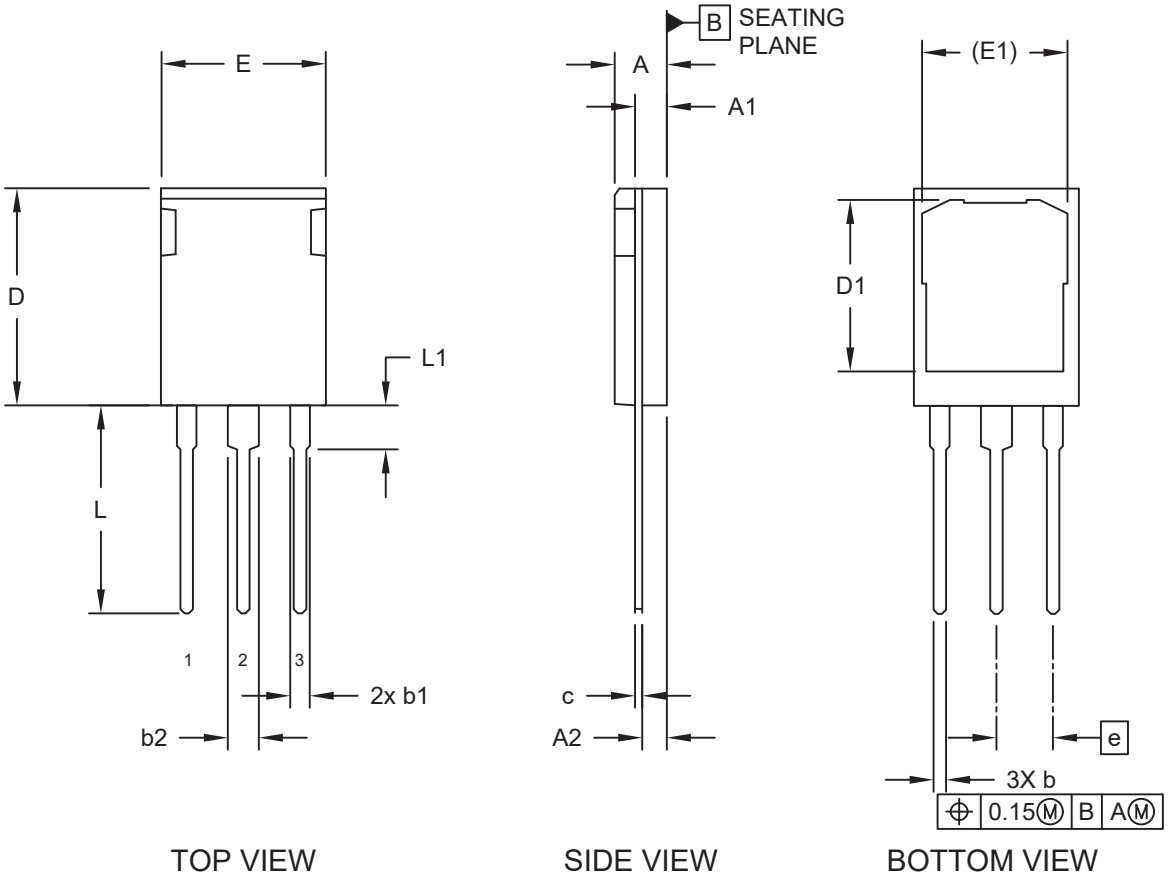
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the T-MAX package outline of this device.

Figure 3-1. Package Outline Drawing



The following table shows the T-MAX dimensions and should be used in conjunction with the package outline drawing.

Table 3-1. T-MAX Dimensions

Dimension Limits		Dimensions (mm)	
		Min.	Max.
Number of leads	N	3	
Pitch	e	5.44 BSC	
Overall height	A	4.70	5.31
Tab height	A1	1.50	2.49
Seating plane to lead	A2	2.21	2.59
Lead width	b	1.02	1.40
Lead shoulder width (×2)	b1	1.65	2.41
Lead shoulder width	b2	2.87	3.38
Lead thickness	c	0.41	0.79

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Table 3-1. T-MAX Dimensions (continued)

Dimension Limits		Dimensions (mm)	
		Min.	Max.
Lead length	L	19.81	20.32
Lead shoulder length	L1	3.99	4.50
Molded body length	D	20.80	21.46
Thermal pad length	D1	16.25	17.65
Total width	E	15.49	16.26
Thermal pad width	E1	13.10	14.50

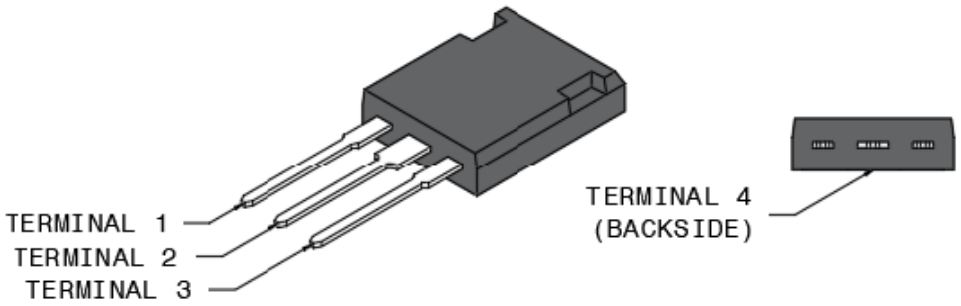
Note:

1. Dimensioning and tolerancing per ASME Y14.5M.

3.2 Terminal Pinout

The following figure illustrates the terminal pinout of this device.

Figure 3-2. Terminal Pinout



The following table shows the electrical signal terminal pinout of this device.

Table 3-2. Electrical Signal Terminal Pinout

Terminal	Definition
TERMINAL 1	Gate
TERMINAL 2	Collector, Diode Cathode
TERMINAL 3	Emitter, Diode Anode
TERMINAL 4	Collector, Diode Cathode

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4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	03/2025	Document created.

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- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

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