VSC8531

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip VSC8531 product family. It is meant to help customers achieve first-pass design success. These checklist items should be followed when utilizing the VSC8531 in a new design. A summary of these items is provided in Section 12.0, "Hardware Checklist Summary". Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet Signals"
- Section 5.0, "Clock Circuit"
- Section 6.0, "Configuration for System Application"
- Section 7.0, "Digital Interface"
- Section 8.0, "Management Interface"
- Section 9.0, "Startup"
- Section 10.0, "Configuration Pins (Strapping Options)"
- Section 11.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The VSC8531 implementor should have the following documents on hand:

- *VSC8531-01 Data Sheet*
- *VSC8531-02 Data Sheet*
- Other related documents found at www.microchip.com/VSC8531
- *ENT-AN0098 Magnetics Guide*

2.2 Pin Check

- Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- A single ground reference as a system ground is used for all ground pins. Use one continuous ground plane to ensure a low-impedance ground path and a continuous ground reference for all signals.
- A chassis ground is necessary between the magnetics and RJ45 connector at line side for better EMI and ESD.

3.0 POWER

Table 3-1 shows the power supply pins for VSC8531.

TABLE 3-1: POWER SUPPLY PINS

Pin Name	Pin Number	Description	Comment
VDD25A	1	2.5V power for GPHY analog port channel A, B, C, and D	Analog, use ferrite bead
VDD25A	5	2.5V power for GPHY analog port channel A, B, C, and D	
VDD25A	8	2.5V power for GPHY analog port channel A, B, C, and D	
VDD1A	2	1.0V analog core power	Analog, use ferrite bead
VDD1A	13	1.0V analog core power	
VDD1A	47	1.0V analog core power	
VDD1	14	1.0V digital core power	Digital, no ferrite bead
VDD1	24	1.0V digital core power	
VDDMAC	15	1.5V, 1.8V, 2.5V, or 3.3V RGMII/RMII™ MAC power	Digital, no ferrite bead
VDDMAC	19	1.5V, 1.8V, 2.5V, or 3.3V RGMII/RMII MAC power	
VDDMAC	27	1.5V, 1.8V, 2.5V, or 3.3V RGMII/RMII MAC power	
VDDIO	37	2.5V or 3.3V general I/O power	Digital, no ferrite bead
VDDMDIO	32	1.2V, 1.5V, 1.8V, 2.5V, or 3.3V power for SMI pins	Digital, no ferrite bead

3.1 Current Requirements

- Ensure that the voltage regulators and power distribution are designed to adequately support these current requirements for each power rail. Refer to Table 3-2. In system design, the current values in the table need an additional margin of at least 30%.

TABLE 3-2: MAXIMUM RAIL CURRENTS

Power Rail	Voltage	Maximum Current
VDD25A	2.5V	150 mA
VDD1A	1.0V	25 mA
VDD1	1.0V	90 mA
VDDMAC	1.5V, 1.8V, 2.5V, and 3.3V	65 mA (3.3V)
VDDIO/VDDMDIO	3.3V (maximum)	5 mA

3.2 Power Supply Planes

- The VSC8531 requires three power rails: 3.3V (or other VDDMAC voltage), 2.5V, and 1.0V. It may also require two power rails when using 2.5V for VDDMAC and VDDIO/VDDMDIO. The filtered analog 1.0V and 2.5V supplies should not be shorted to any other digital supply at the package or PCB level. See Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering".
- The most important PCB design and layout considerations are as follows:
  - Ensure that the return plane is adjacent to the power plane (without a signal layer in between).
  - Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Try to maximize the area of each power split on the power plane based on corresponding via coordinates for each rail to maximize coupling between each voltage rail and the return plane.
  - Minimize resistive drop while efficiently conducting away heat from the device using one-ounce copper cladding.

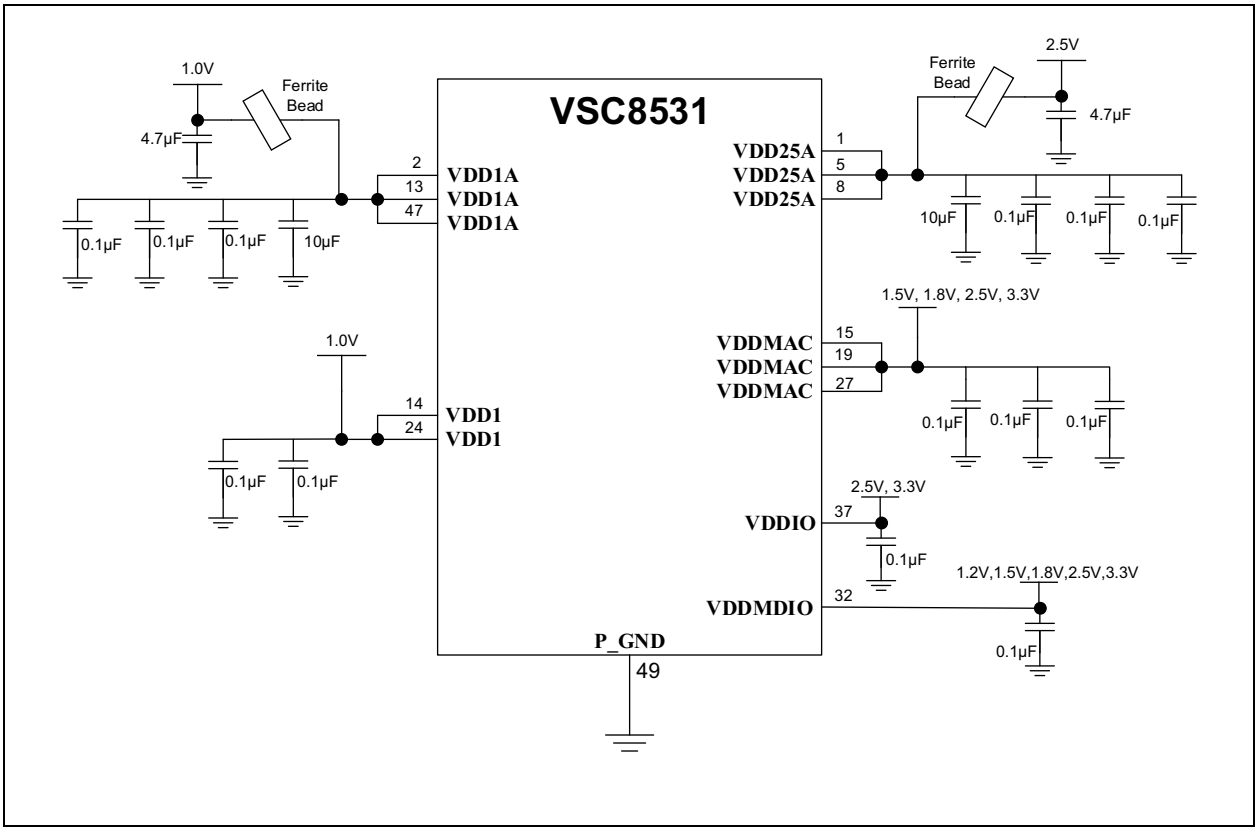
- Four-layer PCBs with only one designated power plane must adhere to proper design techniques to prevent random system events, such as CRC errors. Each power supply requires the lowest resistive drop possible to power pins of the device with correctly positioned local decoupling. For more information, see Section 3.4, "Decoupling Capacitors".
- Ferrite beads should be used over a series inductor filter whenever possible, particularly for high-density or high-power devices.

3.3 Power Circuit Connection and Analog Power Plane Filtering

- The analog power supplies are:
  - **VDD25A**
  - **VDD1A**
- A ferrite bead should be used to isolate each analog supply from the rest of the board. The bead should be placed in series between the bulk decoupling capacitors and local decoupling capacitors.
- Because all PCB designs yield unique noise coupling behavior, not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with 0Ω resistors once a thorough evaluation of system performance is completed.
- Ferrite beads are not recommended on digital supplies **VDD1**, **VDDMAC**, **VDDIO**, and **VDDMDIO**.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER SUPPLY CONNECTIONS AND LOCAL FILTERING



3.4 Decoupling Capacitors

- Bulk decoupling capacitors can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close as possible to the VSC8531's power pins for every pin.
- Make sure that enough bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail.
- If the VSC8531 device is on the top layer of the printed circuit board (PCB), the best location for local decoupling capacitors is on the bottom or underside of the PCB, directly under the device.

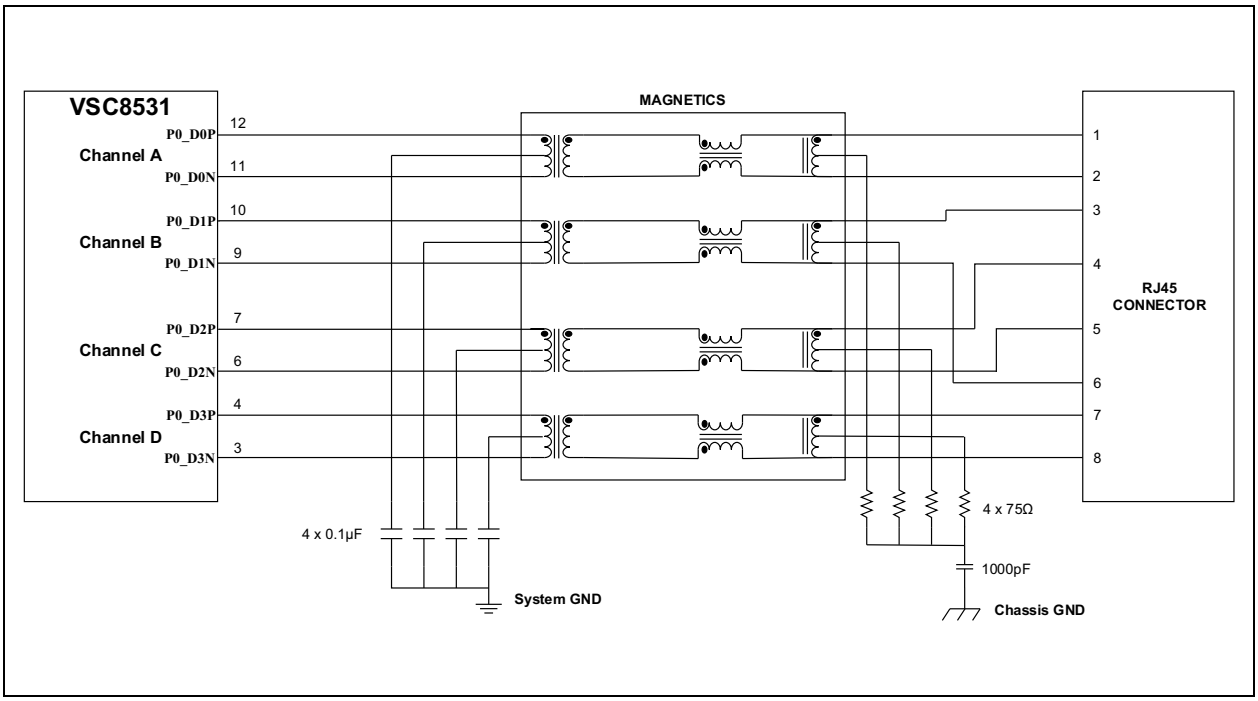
4.0 ETHERNET SIGNALS

4.1 10/100/1000 Mbps Interface Connection

- **P0_D0P** (pin 12): This pin is the transmit/receive positive connection from Pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D0N** (pin 11): This pin is the transmit/receive negative connection from Pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D1P** (pin 10): This pin is the transmit/receive positive connection from Pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D1N** (pin 9): This pin is the transmit/receive negative connection from Pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D2P** (pin 7): This pin is the transmit/receive positive connection from Pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D2N** (pin 6): This pin is the transmit/receive negative connection from Pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D3P** (pin 4): This pin is the transmit/receive positive connection from Pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **P0_D3N** (pin 3): This pin is the transmit/receive negative connection from Pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

For 10/100/1000 Mbps channel connection details, refer to Figure 4-1.

FIGURE 4-1: 10/100/1000 MBPS CHANNEL CONNECTIONS



4.2 10/100/1000 Mbps Magnetics Connection

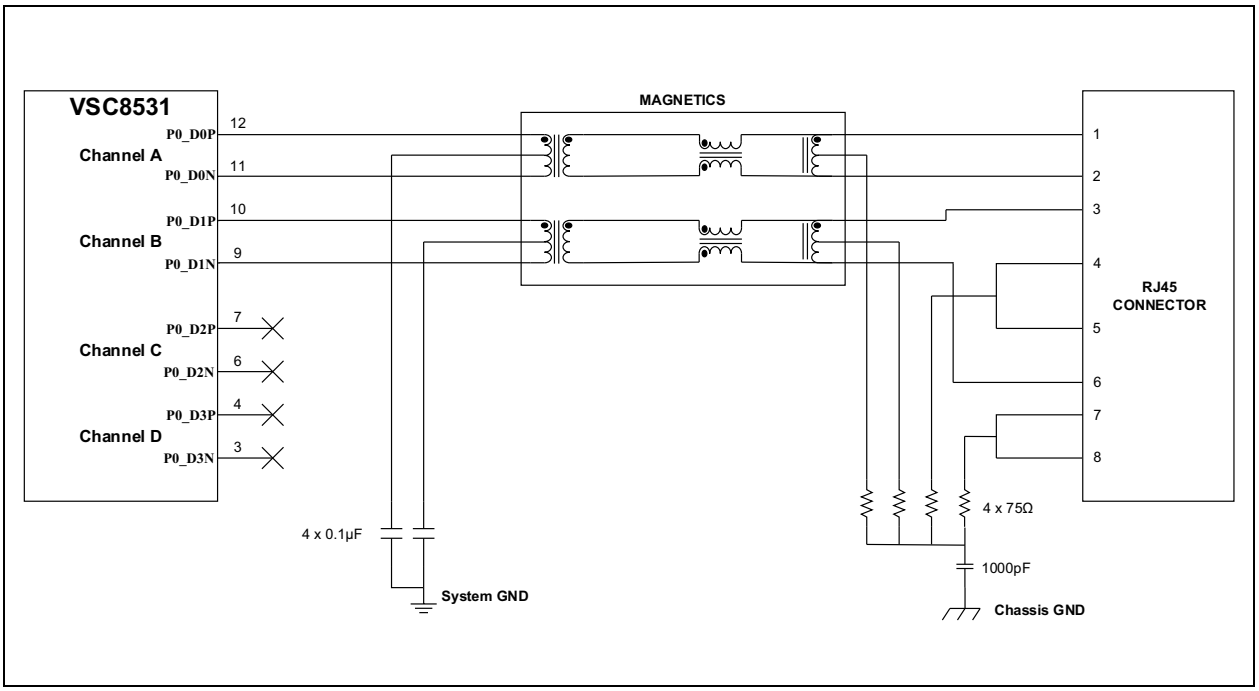
- The center tap connection on the VSC8531 side for Pair A channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8531 side for Pair B channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8531 side for Pair C channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8531 side for Pair D channel only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps from all four pairs of the magnetics should not be connected together. The reason is the Common-mode voltage can be different between pairs, especially for 10/100 operation. (Pairs A and B are active, while Pairs C and D are inactive.)
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by Pair A, Pair B, Pair C, and Pair D center taps.
- Only one 1000 pF, 2 kV capacitor or a ferrite bead to connect between the chassis ground and the system ground, it is shared by PHY 0, PHY 1, PHY 2, and PHY 3 for port 1, port 2, port 3, and port 4.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.6, "Other Considerations" for guidance on how chassis ground should be created from system ground.
- For the magnetics selection, please refer to *ENT-AN0098 Magnetics Guide* application note for the magnetics suggested guidelines.

4.3 10/100 Mbps Interface Connection

- For designs needing only a 10/100 Mbps connection, the 1000 Mbps capability should be removed. The following may be done to remove the 1000 Mbps advertisement for Auto-Negotiation:
  - Set Port Register 0x00, Bit [6,13] = '01' (100 Mbps) or '00' (10 Mbps) to remove the 1000 Mbps speed.
  - Set Port Register 0x09, Bits [9:8] = '00' to remove Auto-Negotiation advertisements for 1000 Mbps.
  - Write a '1' to Register 0x00, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.
- **P0_D0P** (pin 12): This pin is the transmit/receive positive connection from Pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **P0_D0N** (pin 11): This pin is the transmit/receive negative connection from Pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **P0_D1P** (pin 10): This pin is the transmit/receive positive connection from Pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **P0_D1N** (pin 9): This pin is the transmit/receive negative connection from Pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
- **P0_D2P** (pin 7): This pin can be left as NC (No Connect).
- **P0_D2N** (pin 6): This pin can be left as NC (No Connect).
- **P0_D3P** (pin 4): This pin can be left as NC (No Connect).
- **P0_D3N** (pin 3): This pin can be left as NC (No Connect).

For details on 10/100 Mbps channel connections, refer to Figure 4-2.

FIGURE 4-2: 10/100 MBPS CHANNEL CONNECTIONS



4.4 10/100 Mbps Magnetics Connection

- The center tap connection on the VSC8531 side for Pair A (transmit channel) only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center tap connection on the VSC8531 side for Pair B (receive channel) only connects a 0.1 µF capacitor to GND. No bias is needed.
- The center taps of the magnetics of the transmit and receive channels should not be connected together. The reason is that the Common-mode voltage can be different between pairs.
- The center tap connection on the cable side (RJ45 side) for Pair A should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for Pair B should be terminated with a 75Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both Pair A and Pair B center taps.
- MDI connections:
  - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to **P0_D0P** (pin 12) of the VSC8531.
  - Pin 2 of the RJ45 is TX- and should trace through the magnetics to **P0_D0N** (pin 11) of the VSC8531.
  - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to **P0_D1P** (pin 10) of the VSC8531.
  - Pin 6 of the RJ45 is RX- and should trace through the magnetics to **P0_D1N** (pin 9) of the VSC8531.
- MDIX connections:
  - Pin 3 of the RJ45 is TX+ and should trace through the magnetics to **P0_D1P** (pin 10) of the VSC8531.
  - Pin 6 of the RJ45 is TX- and should trace through the magnetics to **P0_D1N** (pin 9) of the VSC8531.
  - Pin 1 of the RJ45 is RX+ and should trace through the magnetics to **P0_D0P** (pin 12) of the VSC8531.
  - Pin 2 of the RJ45 is RX- and should trace through the magnetics to **P0_D0N** (pin 11) of the VSC8531.
- When using the VSC8531 device in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module (that is, the one where the two channels are identical) is required.

4.5 10/100 Mbps RJ45 Connection

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in Cat 5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. Therefore, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in Cat 5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. Therefore, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See Section 4.6, "Other Considerations" for guidance on how chassis ground should be created from system ground.

4.6 Other Considerations

Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor/ferrite bead far away from the VSC8531 device in PCB layout placement for better ESD.

5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections

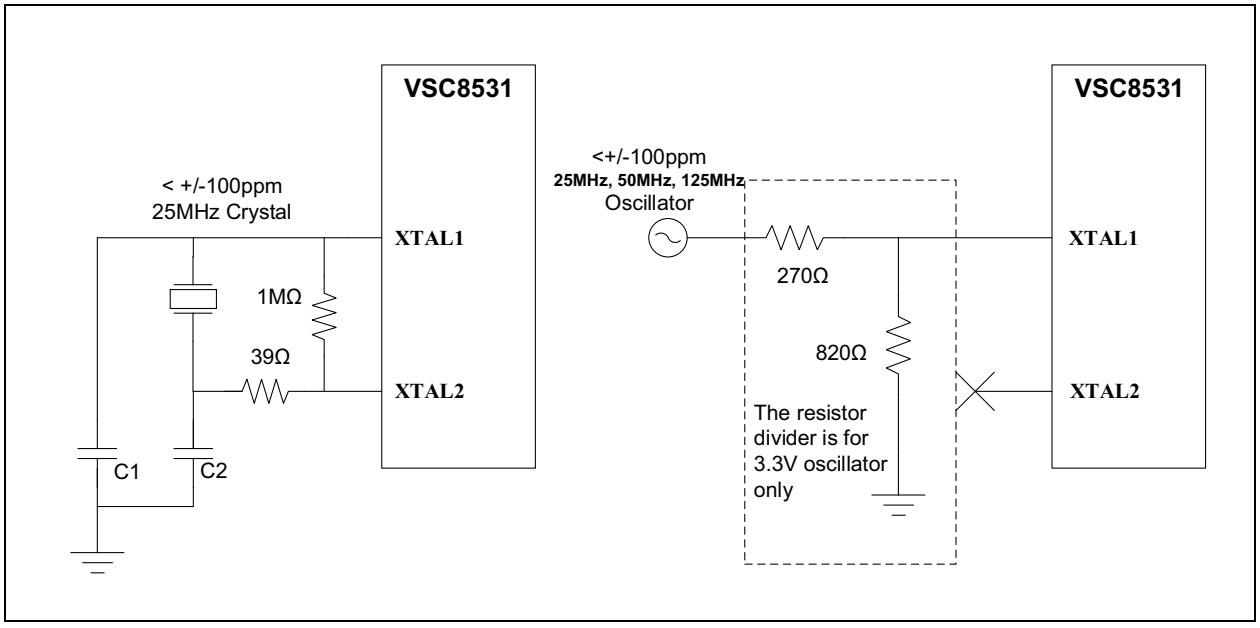
A 25 MHz (maximum –100 ppm) crystal or a 25 MHz, 50 MHz, or 125 MHz (maximum +/–100 ppm) oscillator or clock should be used as the device's clock source.

- **XTAL1** (pin 42): This is the clock circuit input for the VSC8531 device. This pin requires a capacitor to ground directly when a crystal is used. One side of the crystal connects to this pin.
- **XTAL2** (pin 43): This is the clock circuit output from the VSC8531. When a crystal is used, this pin connects to one side of the crystal pin that requires a capacitor to ground.
- Since every system design is unique, the capacitor values are system-dependent, based on the C_L specifications of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.
- Alternately, a 25 MHz, 50 MHz, or 125 MHz clock oscillator may be used to provide the clock source for the VSC8531. When using a single-ended clock source, it is better that **XTAL1** (pin 42) connects to a 2.5V oscillator. If using a 3.3V clock oscillator, designers need to use a resistor divider. **XTAL2** (pin 43) should be left floating as No Connect (NC). See Figure 5-1.
- An external 1 MΩ resistor between **XTAL1** and **XTAL2** pins is necessary for the VSC8531.
- The use of a crystal with a minimum drive level of 50-100 µW is recommended. A higher drive level is more preferable.
- **REFCLK_SEL0** (pin 41): Reference Clock mode/frequency select signal
- **REFCLK_SEL1** (pin 40): Reference Clock mode/frequency select signal
- The VSC8531 supports multiple reference clock input options through the strap pins [40, 41] of **REFCLK_SEL** [1:0] to allow maximum system level flexibility. See Table 5-1 for details on strap options.

TABLE 5-1: REFCLK FREQUENCY SELECTION

REFCLK_SEL [1:0]	Clock Components	Used Pins
00	25 MHz Crystal	**XTAL1** and **XTAL2** pins
01	25 MHz Oscillator	**XTAL1** pin
10	50 MHz Oscillator	**XTAL1** pin
11	125 MHz Oscillator	**XTAL1** pin

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS FOR VSC8531



6.0 CONFIGURATION FOR SYSTEM APPLICATION

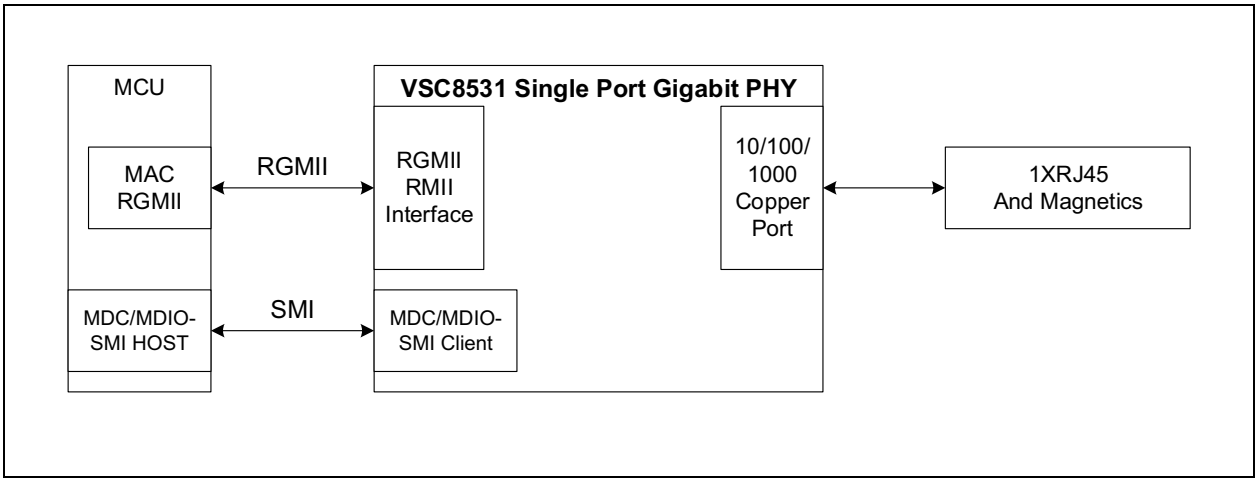
The VSC8531 applications have two categories:

- Design for Using RGMII Interface
- Design for Using RMII™ Interface

6.1 Design for Using RGMII Interface

- Set signal E pin 21 **RX_CTL** = 0 by default or using an external pull-down resistor to configure the RGMII/RMII interface to RGMII mode.
- Use an MDC/MDIO-SMI interface that can access all MIIM registers for this GPHY. See Figure 6-1.

FIGURE 6-1: DIAGRAM EXAMPLE FOR USING RGMII INTERFACE TO MAC RGMII



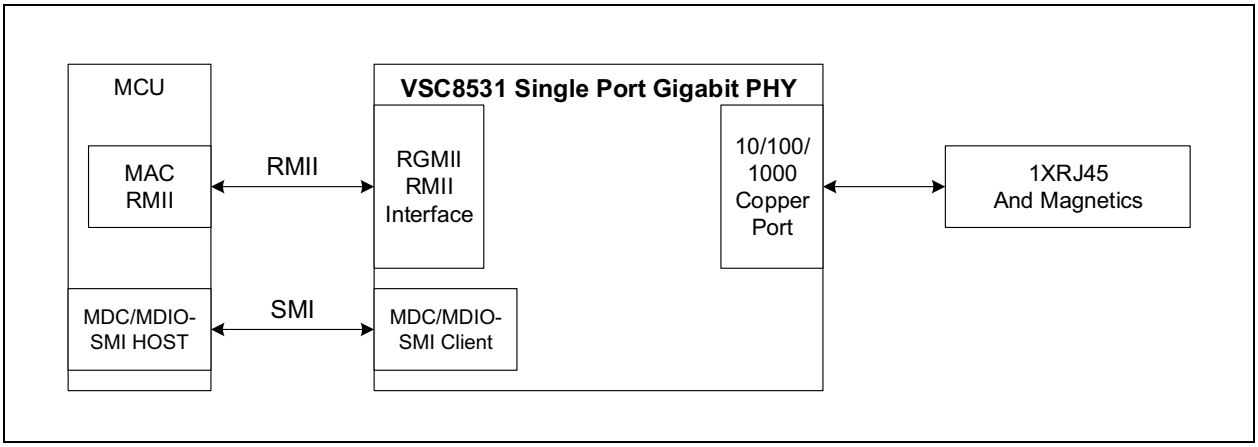
6.2 Design for Using RMII™ Interface

- Set signal E pin 21 **RX_CTL** = 1 by using an external pull-up resistor to configure the RGMII/RMII interface to RMII mode.

  Note: RMII only supports 100 Mbps and 10 Mbps, and not 1000 Mbps. When RMII mode is selected, the link advertisement selection must also be changed to either 01, 10, or 11 settings (see Table 10-4 for details). For consistency, it is also suggested not to connect copper port pairs C and D to the RJ45 and magnetics.

- Use an MDC/MDIO-SMI interface that can access all MIIM registers for this GPHY. See Figure 6-2.

FIGURE 6-2: DIAGRAM EXAMPLE FOR USING RMII™ INTERFACE TO MAC RMII



7.0 DIGITAL INTERFACE

7.1 Strap Pins for RGMII and RMII™ Configuration

- The VSC8531 provides one digital interface. The interface can be configured to RGMII or RMII with different modes through the strap pins 21, 40, and 41. For detailed configurations, refer to Table 7-1.

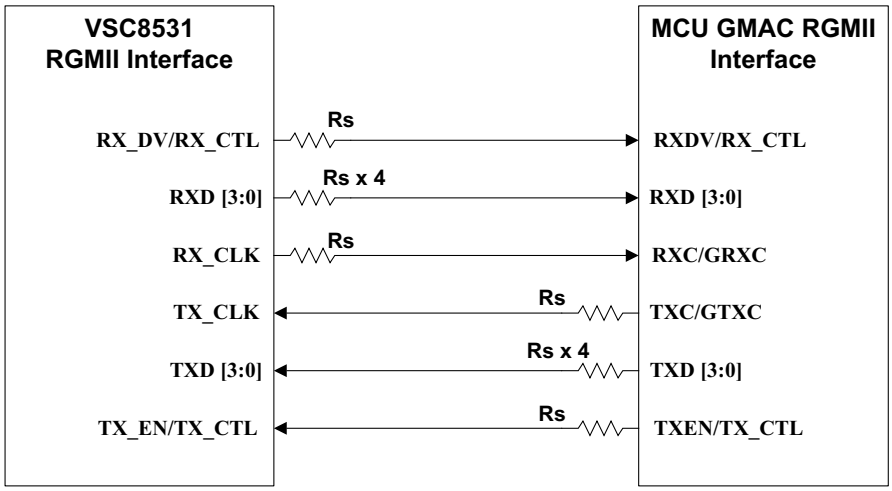
TABLE 7-1: INTERFACE CONFIGURATIONS

Interface Modes	Strap Pin 21 RX_CTL Pull-down = 0, Pull-up = 1 (Default = 0)	REFCLK_SEL [1,0], Pins [40,41] Pull-down = 0, Pull-up = 1 (Default =11)
RGMII		
25 MHz Crystal	0	00
25 MHz Oscillator	0	01
50 MHz Oscillator	0	10
125 MHz Oscillator	0	11
RMII Mode 1 - Normal Mode		
50 MHz mode	1	10
RMII Mode 2 - Clock Mode		
25 MHz Crystal	1	00
25 MHz Oscillator	1	01
125 MHz Oscillator	1	11

7.2 RGMII Interface

- The VSC8531 provides RGMII. The RGMII interface contains two distinct groups of signals: one for transmission and one for receiving. See Table 7-1 for detailed configuration of the RGMII.
- The VSC8531 devices support RGMII versions 1.3 and 2.0. The RGMII interface supports all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps) and is used as an interface to an RGMII-compatible MAC. The devices are compliant with the RGMII interface specification when VDDMAC is operating at 2.5V. While the RGMII specification only specifies operation at 2.5V, the devices can also support the RGMII interface at 1.5V, 1.8V, and 3.3V.
- MCU GMAC RGMII should have the same speed and duplex as the VSC8531 RGMII interface. The VSC8531 RGMII connections with MCU RGMII are shown in Figure 7-1.

FIGURE 7-1: CONNECTIONS BETWEEN VSC8531 RGMII AND MCU RGMII INTERFACE



7.2.1 SYSTEM CONSIDERATION FOR DESIGN WITH RGMII INTERFACE

- The VSC8531 supports RGMII V2.0 specifications. The RMII interface needs to meet Ingress Internal Delay (RGMII-IID) and Egress Internal Delay (RGMII-EID) specifications. In most cases, setting the VSC8531 RGMII ID is required based on other end RMII-ID to meet the RGMII V2.0 specifications. Take note to use either strap pins or the register 20E2 to set the VSC8531 RGMII-ID. The VSC8531 RGMII-ID setting principles are detailed in Table 7-2.
- The VSC8531 RGMII register setting is based on the other end RGMII clock input/output clock delay and RGMII traces routing with equal length for two distinct groups of signals in the PCB layout.

TABLE 7-2: REFERENCE FOR RGMII STRAP PINS OR REGISTER CONFIGURATION

VSC8531 Strapping Pins RXD0, RXD1 (Signal A, B) Pins [20, 18] Default = 00	VSC8531 RGMII RX_CLK and TX_CLK Input and Output Delay	VSC8531 Register (20E2)	VSC8531 RGMII Clock Delay/ Slew Configuration	Other End RGMII Default RGMII-ID or Configuration
1,0 = 2.0 ns 1,1 = 2.6 ns For both TX_CLK and RX_CLK	Ingress Clock Input (TX_CLK)	Bits [2:0]	Delay	No Delay or A Little Delay
	Egress Clock Output (RX_CLK)	Bits [6:4]	Delay	No Delay or A Little Delay
If strapping is not sufficient, the registers must be set for RX_CLK and TX_CLK delays to meet RGMII specification	Ingress Clock Input (TX_CLK)	Bits [2:0]	Delay	No Delay or A Little Delay
	Egress Clock Output (RX_CLK)	Bits [6:4]	No Delay or A Little Delay	Delay
If strapping is not sufficient, the registers must be set for RX_CLK and TX_CLK delays to meet RGMII specification	Ingress Clock Input (TX_CLK)	Bits [2:0]	No Delay or A Little Delay	Delay
	Egress Clock Output (RX_CLK)	Bits [6:4]	Delay	No Delay or A Little Delay
0, 0 = 0.2 ns (Default) 0, 1 = 1.1 ns For both TX_CLK and RX_CLK	Ingress Clock Input (TX_CLK)	Bits [2:0]	No Delay or A Little Delay	Delay
	Egress Clock Output (RX_CLK)	Bits [6:4]	No Delay or A Little Delay	Delay

Note 1: Based on this table, the strap pin method can be used when the other end transmitting/receiving RGMII-ID has the same no delay (a little delay) or delay for both cases.

7.3 RMII™ Interface

- Table 7-1 shows the detailed configuration of the RMII mode 1, 50 MHz RMII Normal mode and RMII mode 2, 25 MHz/125 MHz RMII Clock mode of the VSC8531 interface. The RMII Clock mode provides a 50 MHz RMII reference clock, and the RMII Normal mode receives a 50 MHz RMII reference clock.
- The RMII interface supports 10 Mbps and 100 Mbps speeds and is used as an interface to an RMII-compatible MAC. The devices are compliant with the RMII interface specification when VDDMAC is operating at 3.3V. While the RMII specification only specifies operation at 3.3V, the devices can also support the RMII interface at 1.5V, 1.8V, and 2.5V.
- The VSC8531 interface RMII mode 1, 50 MHz RMII Normal mode (input 50 MHz reference clock) and RMII mode 2, 25 MHz/125 MHz RMII Clock mode (output 50 MHz reference clock) are shown in Figure 7-2 and Figure 7-3, respectively.

7.3.1 RMII™ MODE 1, 50 MHZ RMII NORMAL MODE

- The VSC8531 Interface can be set to RMII mode 1. See Table 7-1.
- In this mode of operation, an external source is used to provide a 50 MHz clock through **RMII_CLKIN** and the **XTAL1** pin. This 50 MHz clock is used as the main clock for the RMII interface and must be used as the reference clock for the PHY connected to the **XTAL1** pin. In this mode, the **RMII_CLKOUT** signal from the PHY is not used. The **RMII_CLKOUT** is enabled by default, and that clock output should be disabled through register 27E2.4.

- The other side can be a MAC RMII Clock mode or a MAC RMII Normal mode. The connections are illustrated in Figure 7-2 and Figure 7-3.

FIGURE 7-2: CONNECTIONS BETWEEN VSC8531 RMII™ MODE 1 (50 MHZ RMII NORMAL MODE) AND MAC RMII NORMAL MODE (INPUT 50 MHZ REFCLK CLOCK)

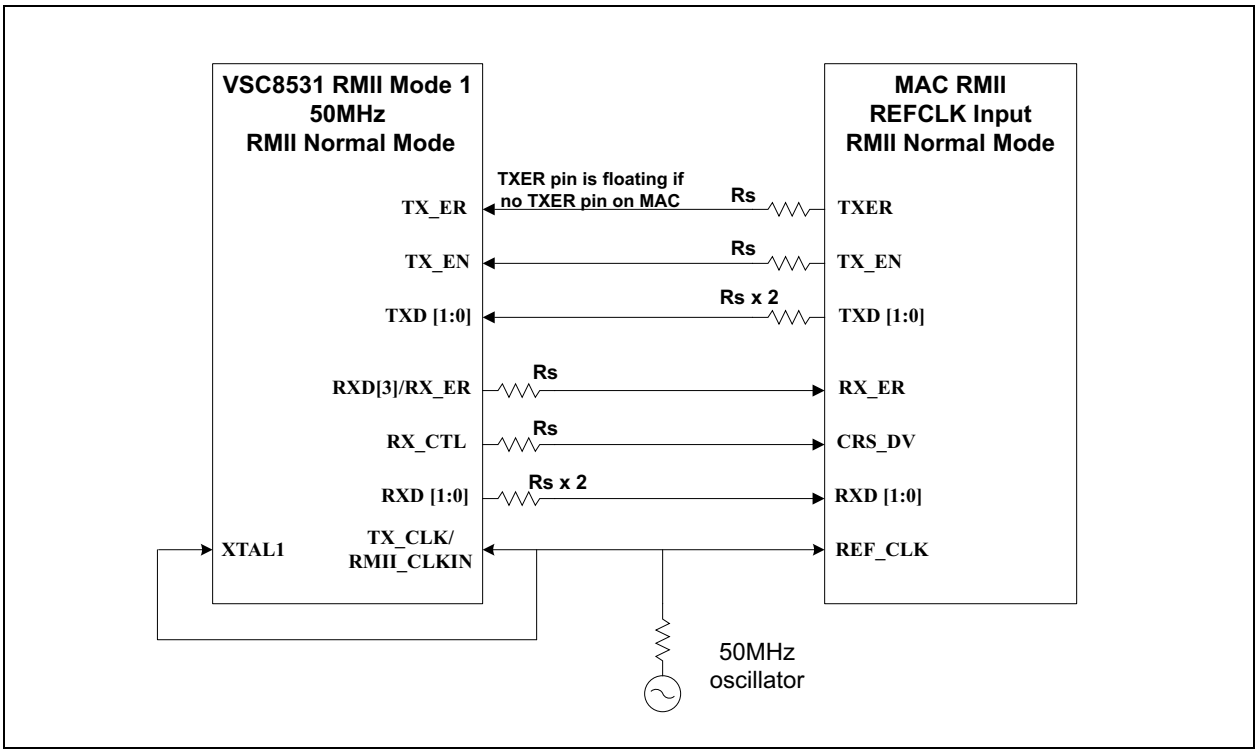
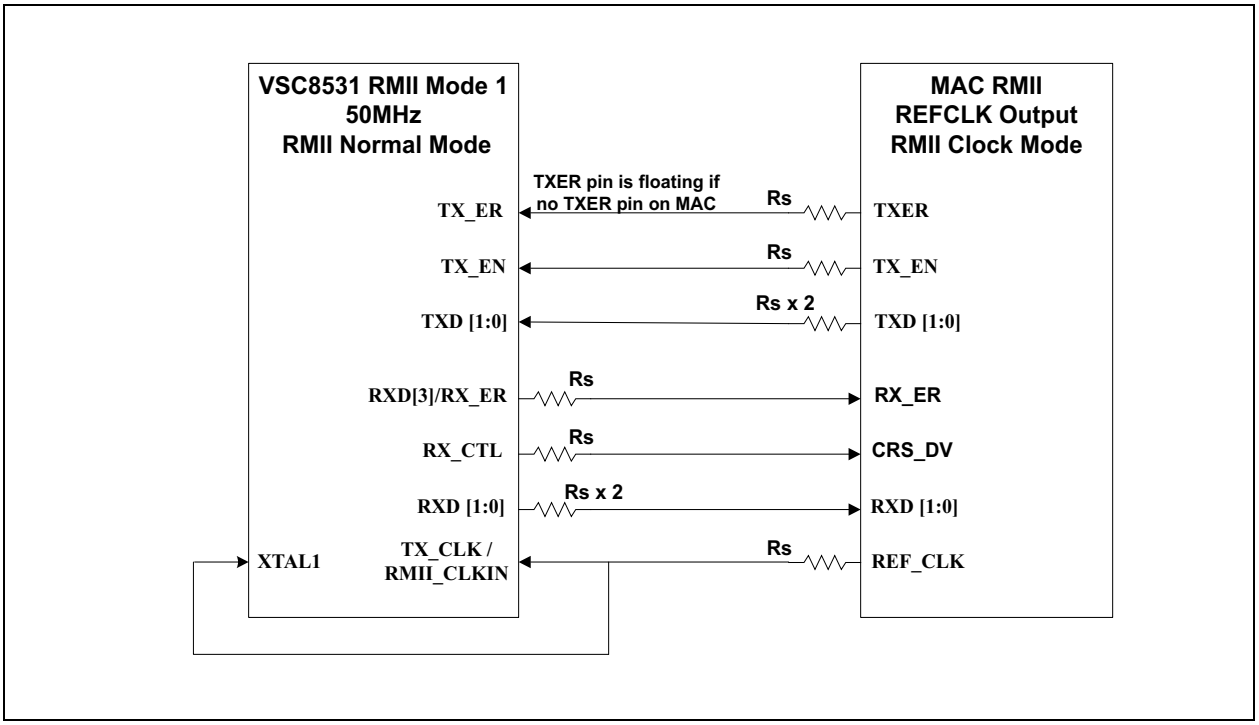


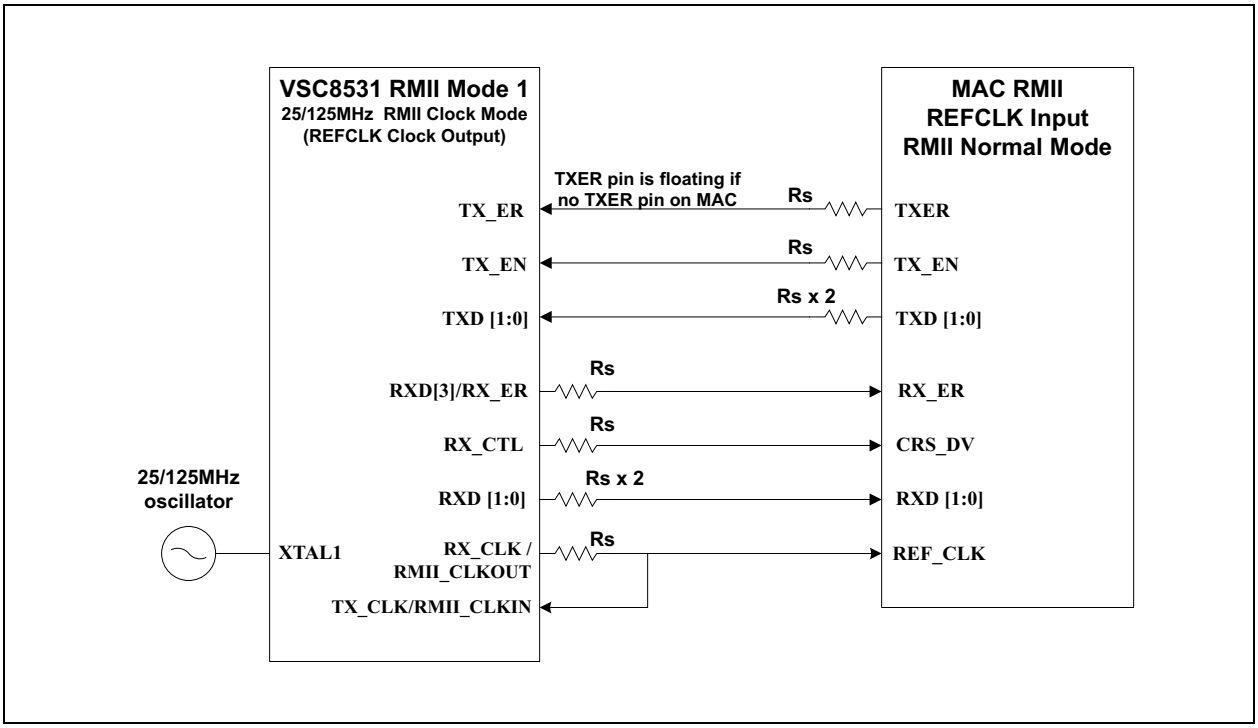
FIGURE 7-3: CONNECTIONS BETWEEN VSC8531 RMII™ MODE 1 (50 MHZ RMII NORMAL MODE) AND MAC RMII CLOCK MODE (OUTPUT 50 MHZ REFCLK CLOCK)



7.3.2 RMII™ MODE 2, 25 MHZ/125 MHZ RMII CLOCK MODE

- The VSC8531 interface can be set to RMII mode 2. See Table 7-1.
- In this mode of operation, the PHY operates from a 25 MHz crystal (**XTAL1** and **XTAL2**) or 25 MHz/125 MHz single-ended external clock (**XTAL1**) and sources the 50 MHz clock required for the RMII interface. This 50 MHz clock is outputted from the PHY on the **RMII_CLKOUT** pin and then connected to the MAC **REF_CLK** and PHY **RMII_CLKIN** signals. In this mode, the PHY generates a 50 MHz clock for the system, and that clock output is enabled.
- The other side can be a MAC RMII Normal mode to receive 50 MHz RMII REFCLK clock. The connections are illustrated in Figure 7-4.

FIGURE 7-4: CONNECTIONS BETWEEN VSC8531 RMII™ MODE 2 (25 MHZ/125 MHZ RMII CLOCK MODE) AND MAC RMII NORMAL MODE (INPUT 50 MHZ REFCLK CLOCK)



7.4 RGMII and RMII™ Interface Series Terminations

- Provisions should be made for series resistors for all outputs on the RGMII and RMII interfaces. Series resistors will enable the designer to closely match the output driver impedance of the VSC8531 and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system. The recommended values of these series resistors (Rs) and PCB Rs placement are in Table 7-3 and Table 7-4.

TABLE 7-3: RECOMMENDED SERIES TERMINATION RESISTOR VALUES

VDDMAC Value	Series Termination Resistor Rs Value
1.5V	27Ω
1.8V	33Ω
2.5V	39Ω
3.3V	39Ω

TABLE 7-4: SERIES TERMINATIONS FOR RGMII AND RMII™ INTERFACE

Signals for RGMII and RMII Interfaces	Series Resistors at VSC8531 RGMII and RMII Drive Pins	Series Resistors at the other end RGMII and RMII Drive Pins
RXD [3:0]/RXD [1:0]	Rs	—
RX_CTL/CRS_DV	Rs	—
RX_CLK/RMII_CLKOUT	Rs	—
TX_CLK/RMII_CLKIN	—	Rs
TX_CTL/TX_EN	—	Rs
TXD [3:0]/TXD [1:0]	—	Rs

Note 1: The series resistors should be placed as close as possible to both VSC8531 drive pins and the other end drive pins in the PCB layout.

2: The unused pins of the interfaces should be unconnected except the unused I/O pin without internal pull-up or pull-down.

8.0 MANAGEMENT INTERFACE

8.1 Serial Management Interface (SMI)

- The VSC8531 family of devices includes an IEEE 802.3-compliant Serial Management Interface (SMI) that is affected by using the devices' **MDC** and **MDIO** pins. The SMI provides access to device control and status registers stated in the *VSC8531 Data Sheet*. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Additional pages of registers are accessible using device register 31.
- Energy-efficient Ethernet (EEE) control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 to 14.
- The SMI is a synchronous serial interface with input data to the VSC8531 family of devices on the **MDIO** pin that is clocked on the rising edge of the **MDC** pin. The output data is sent to the **MDIO** pin on the rising edge of the MDC signal. The interface can be clocked at a rate ranging from 0 MHz to 12.5 MHz, depending on the total load on **MDIO**. An external 2 kΩ pull-up resistor is required on the **MDIO** pin.

8.2 SMI Pins

- **MDC** (pin 31): This pin is a management data clock. A maximum of 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
- **MDIO** (pin 33): This pin is a management data input/output pin. From this pin, serial data is bidirectionally and synchronously written or read between the PHY and station manager on the positive edge of MDC. One 2 kΩ external pull-up resistor is required, and the pull-up resistor should be tied to the VDDMDIO power.
- **MDINT** (pin 34): This pin is a management interrupt signal. This output is open-drain and requires an external pull-up resistor. It may be wired with other open-drain interrupt signals. If **MDINT** is unused, it may be left unconnected, without a resistor.

9.0 STARTUP

9.1 Reset

- The VSC8531 must be reset at power-up. One option is to hold **NRESET** low for a minimum of 1 ms after all power rails are up, control pins are stable, and clocks are active. Another option is to pulse **NRESET** low for a minimum 1 ms after power-up. **NRESET** is typically driven by a voltage monitor device or by the management processor or FPGA. It is acceptable to use a simple R/C reset circuit with 10 kΩ pull-up and 0.1 µF capacitor pull-down to meet 1 ms reset time for a power-up reset.
- The **NRESET** (pin 35) is an active-low Reset input. This signal resets all logic and all register bits to their default values within the VSC8531.

10.0 CONFIGURATION PINS (STRAPPING OPTIONS)

- The VSC8531 family of devices provides hardware-configured modes of operation that are achieved by sampling output pins on the rising edge of Reset and externally pulling the pin to a logic high or low (based on the desired configuration). These pins become inputs while **NRESET** is asserted, and the logic states of the pins are latched in the device upon deassertion of **NRESET**. To ensure correct operation of the hardware strapping function, any other device connected to these pins must not actively drive a signal onto them.

10.1 Hardware Mode Strapping and PHY Addressing

Table 10-1 lists the pins used for Hardware mode strapping and PHY addressing as well as their respective modes.

TABLE 10-1: HARDWARE MODE STRAPPING AND PHY ADDRESSING

Pins and Default PU = 1, PD = 0	Operation Mode	Description
CLKOUT (pin 36 PD)	Enable/Disable CLKOUT signal and clock output	Clock output 0 = Disabled (Default) 1 = Enabled The frequency of CLKOUT can be programmed to the following values through register 13G.14:13: • 25 MHz • 50 MHz • 125 MHz
RX_CLK (pin 22 PD)	Managed or Unmanaged mode	Mode Select 0 = Managed mode (Default) 1 = Unmanaged mode
RXD0 (pin 20 PD)	Signal A	Managed mode: See Table 10-2 for PHY Addressing Unmanaged mode: See Table 10-3, Table 10-4, and Table 10-5.
RXD1 (pin 18 PD)	Signal B	
RXD2 (pin 17 PD)	Signal C	
RXD3 (pin 16 PD)	Signal D	
RX_DV/RX_CTL (pin 21 PD)	Signal E	

Note 1: If CLKOUT is enabled, the clock output is from pin 36 **CLKOUT**.

10.2 Managed Mode

- When the **RX_CLK** pin is pulled low and the state of that signal is latched to logic 0 on the rising edge of Reset, the devices operate in the Managed mode. In Managed mode, the remaining five signals (A to E) are used to set the PHY address, allowing up to 32 devices to reside on the shared MDIO bus. In this mode, the devices can be configured using register access and no additional hardware configuration is provided. Table 10-2 lists the assigned PHY address values in the Managed mode.

TABLE 10-2: PHY ADDRESS IN MANAGED MODE

Signal	PHY Address Values
Signal A	PHY address bit 0
Signal B	PHY address bit 1
Signal C	PHY address bit 2
Signal D	PHY address bit 3
Signal E	PHY address bit 4

10.3 Unmanaged Mode

- When **RX_CLK** is pulled high externally and the state of that signal is latched to logic 1 on the rising edge of Reset, the devices operate in the Unmanaged mode. Signals A to E are used to set default chip configurations as described in the following:
  - Signals A and B are used to set the RGMII **RX_CLK** and **TX_CLK** (**GTX_CLK**) delay settings (as defined in register 20E2). Table 10-3 shows the details for the strap pins in Table 10-1.
  - Signals C and D are used to select the link advertisement setting. Table 10-4 shows the details for strap pins.
  - Signal E is used to select between RMII and RGMII interface modes. Table 10-5 lists the details for strap pins.

TABLE 10-3: SIGNAL A AND B STRAP FUNCTION IN UNMANAGED MODE

Signal A, B	RX_CLK and TX_CLK Delay
0, 0	000 – 0.2 ns
0, 1	010 – 1.1 ns
1, 0	100 – 2.0 ns
1, 1	110 – 2.6 ns

TABLE 10-4: SIGNAL C AND D STRAP FUNCTION IN UNMANAGED MODE

Signal C, D	Link Advertisement
0, 0	Default mode of operation, 10/100/1000 FDX/HDX, Auto-negotiation ON
0, 1	10/100 FDX/HDX, Auto-negotiation ON (disable 1000BT advertisements)
1, 0	100BTX, HDX Forced mode, Auto-negotiation OFF
1, 1	10BT, HDX Forced mode, Auto-negotiation OFF

Note 1: RMII only supports 10/100 Mbps speeds. When RMII mode is selected, the link advertisement selection must be changed to any of the following settings: 01, 10, or 11.

TABLE 10-5: SIGNAL E STRAP FUNCTION IN UNMANAGED MODE

Signal E	Interface Mode
0	RGMII mode
1	RMII mode

10.4 General External Pull-Up and Pull-Down Resistors

- If there is no specified pull-up resistor value, using a 4.7 kΩ resistor is recommended.
- If there is no specified pull-down resistor value, using a 1 kΩ or 4.7 kΩ resistor is recommended.

11.0 MISCELLANEOUS

11.1 Miscellaneous Pins

- **REF_REXT** (pin 48) on the VSC8531 should connect to the system ground through a 2 kΩ resistor with a tolerance of 1.0%. This pin is used to set up critical bias currents for the Ethernet physical devices.
- **REF_FILT** (pin 46) on the VSC8531 should connect to the system ground through a 0.01 µF with a tolerance of 20%.

11.2 Unused Pins

- **RESERVED_0** (pin 45): This pin should be left unconnected.
- **RESERVED_1** (pin 44): This pin should be left unconnected.

12.0 HARDWARE CHECKLIST SUMMARY

TABLE 12-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.1, "Current Requirements"	Refer to Table 3-1 and Table 3-2 to ensure that the power pins are correct. Select the correct power components with at least 25% margin for the system power consumption.		
	Section 3.2, "Power Supply Planes"	When creating a PCB layout, refer to this section for power supply planes design.		
	Section 3.3, "Power Circuit Connection and Analog Power Plane Filtering"	Refer to Figure 3-1 to check the power circuit connection and filtering.		
	Section 3.4, "Decoupling Capacitors"	Refer to this section for the required decoupling capacitors when creating a PCB layout.		
Section 4.0, "Ethernet Signals"	Section 4.1, "10/100/1000 Mbps Interface Connection"	Verify all analog I/O pin connections and circuit design based on Figure 4-1.		
	Section 4.2, "10/100/1000 Mbps Magnetics Connection"	Verify the magnetics and the Common-mode capacitor connections based on Figure 4-1.		
	Section 4.3, "10/100 Mbps Interface Connection"	Verify the 10/100 analog I/O pin connections and circuit design based on Figure 4-2.		
	Section 4.4, "10/100 Mbps Magnetics Connection"	Verify the 10/100 analog I/O pin connections and circuit design based on Figure 4-2.		
	Section 4.5, "10/100 Mbps RJ45 Connection"	Verify the RJ45 connector spare pin pair and termination resistor connections based on Figure 4-2.		
	Section 4.6, "Other Considerations"	If the design has RJ45, verify the use of chassis ground and one ferrite bead. Use the resistor and capacitor to connect to the system ground.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections"	Verify the **REFCLK_SEL** strap pin settings for the input clock used. Check the crystal circuit design or oscillator circuit design based on Figure 5-1 for the correct schematic design		
Section 6.0, "Configuration for System Application"	Section 6.1, "Design for Using RGMII Interface"	If the digital I/O interface uses the RGMII mode, make sure that the configuration strap pins are set correctly.		
	Section 6.2, "Design for Using RMII™ Interface"	If the digital I/O interface uses RMII mode, make sure that the configuration strap pins are set correctly.		

TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Digital Interface"	Section 7.1, "Strap Pins for RGMII and RMII™ Configuration"	Ensure that the strapping for the digital I/O interface is correct based on Table 7-1.		
	Section 7.2, "RGMII Interface"	For VSC8531 RGMII with other end RGMII connections, make sure that the pin-to-pin and the input and output connections are correct based on Figure 7-1.		
	Section 7.2.1, "System Consideration for Design with RGMII Interface"	If using strap pins for ingress and egress internal delay, refer to Table 7-2 based on other end RGMII ingress and egress internal delay.		
	Section 7.3, "RMII™ Interface"	For VSC8531 RMII with other end RMII connections, make sure that the input and output connections are correct.		
		If other end RMII requires to receive 50 MHz RMII reference clock, check the design connections based on Figure 7-2.		
		If other end RMII can output 50 MHz RMII reference clock, check the design connections based on Figure 7-3.		
		If VSC8531 RMII is using 25 MHz/125 MHz mode (RMII Clock mode) to output 50 MHz RMII clock, check the design connection based on Figure 7-4.		
	Section 7.4, "RGMII and RMII™ Interface Series Terminations"	Check if all drive pins have the series termination resistors and correct resistor value for the digital I/O interface based on Table 7-3 and Table 7-4. All series termination resistors should be placed as close as possible to their drive pins in the PCB layout.		
Section 8.0, "Management Interface"	Section 8.1, "Serial Management Interface (SMI)"	When using an MDC/MDIO interface, the MDC clock frequency should be less than 12.5 MHz, and the MDIO should have a 2 kΩ pull-up resistor.		
	Section 8.2, "SMI Pins"	Ensure that the correct SMI pin numbers and VDDMDIO power are used.		
Section 9.0, "Startup"	Section 9.1, "Reset"	Ensure that the designed Reset circuit meets the reset time requirement.		
Section 10.0, "Configuration Pins (Strapping Options)"	Section 10.1, "Hardware Mode Strapping and PHY Addressing"	To comply with the design required and system application, make sure that the strapping is correct based on Table 10-1.		
	Section 10.2, "Managed Mode"	If using Managed mode, use the correct strap pins based on Table 10-2 for PHY Addressing.		
	Section 10.3, "Unmanaged Mode"	If using Unmanaged mode, use the correct strap pins based on Table 10-3,Table 10-4, and Table 10-5 for correct strapping options.		
	Section 10.4, "General External Pull-Up and Pull-Down Resistors"	Remember that it is recommended to use a 4.7 kΩ pull-up resistor and a 1 kΩ pull-down resistor.		

TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 11.0, "Miscellaneous"	Section 11.1, "Miscellaneous Pins"	Check if the resistor and capacitor values for the two miscellaneous pins are correct.		
	Section 11.2, "Unused Pins"	Refer to this section for unused pins.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004035A (06-16-21)	Initial release	

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