USB3346

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB3346. These checklist items should be followed when utilizing the USB3346 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 9. Detailed information on these subjects can be found in the corresponding sections:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB"
- Section 5.0, "Clock Circuit"
- Section 7.0, "Startup"
- Section 8.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required References

The USB3346 implementor should have the following documents on hand:

- *USB3346 Data Sheet*
- *AN19.17 ULPI Design Guide*
- *AN18.15 PCB Design Guidelines for QFN and DQFN Packages*
- *AN26.21 USB Device Design Checklist*
- USB 2.0 Specification
- ULPI Specification

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

- The ground flag, **GND**, must be connected to the solid ground plane on the board.
- The ground flag is the only circuit ground for power. Other signals that are connected to ground should not be relied upon to provide ground.
- **GND** is also the main path for removing heat from the USB3346. It is therefore important that there are enough vias under the USB3346 connecting it to the ground and that those vias are evenly distributed.
- It is also important that the vias be plugged or vented in such a way as to prevent voids from forming in the solder connection. For details on this topic, see the *AN18.15* and *AN26.21* application notes.

3.0 POWER

- USB3346 requires power at:
  - 3.3V for USB analog circuits on **VDD33** pins
  - 1.8V for internal digital circuits on **VDD18** pins

- USB3346 contains internal voltage regulators at 3.3V and 1.8V. The 3.3V regulator is enabled automatically when **VBAT** is supplied. Otherwise, 3.3V must be supplied externally, and the 3.3V regulator is automatically disabled.
  - **VDD18** (pin 22 /B3) must have a 1.0 µF filter capacitor attached and connected to ground. One capacitor for both pins is sufficient.
  - **VDD33** (pin15) must have a 1.0 µF filter capacitor attached if the 3.3V regulator is enabled, having less than 1Ω ESR, connected to ground. If the 3.3V regulator is disabled, it should have a 1.0 µF decoupling capacitor attached and connected to ground.
  - **VDD18** and **VDA33** may not be used to supply power to other devices.
- **VBAT** (pin 16) may be supplied from **VBUS**. In this case, an overvoltage protection should be added to the **VBAT** input for protection from surges on **VBUS**. In addition, R_{VBUS} must be added to the **VBUS** input.

The power and ground connections are shown in Figure 3-1, Figure 3-2, and Figure 3-3.

FIGURE 3-1: POWER AND GROUND CONNECTIONS, INTERNAL REGULATION

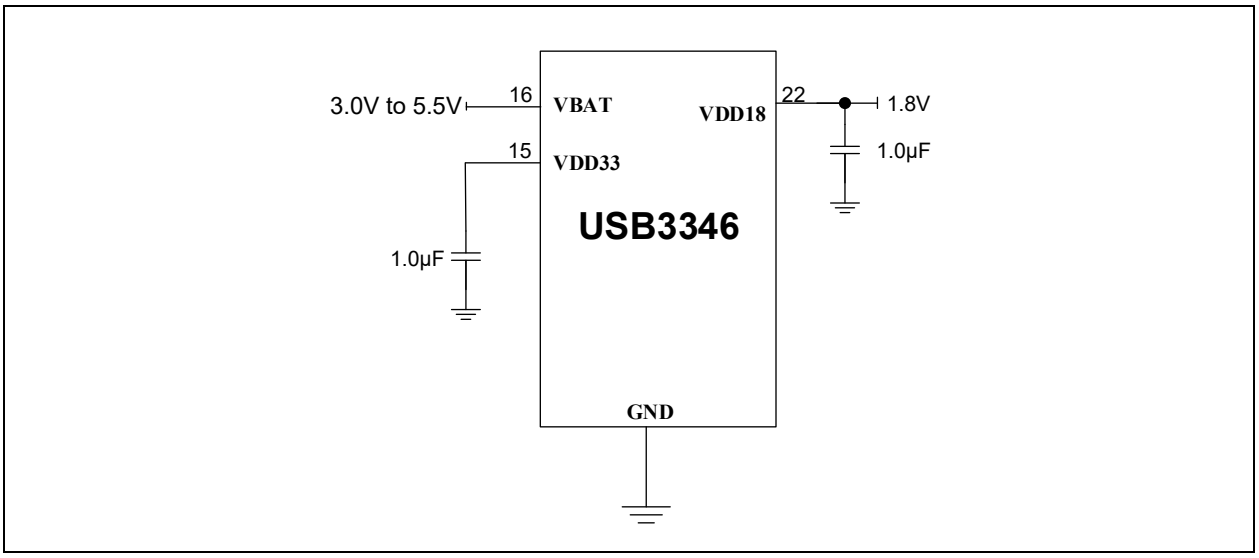


FIGURE 3-2: POWER AND GROUND CONNECTIONS, EXTERNAL REGULATION

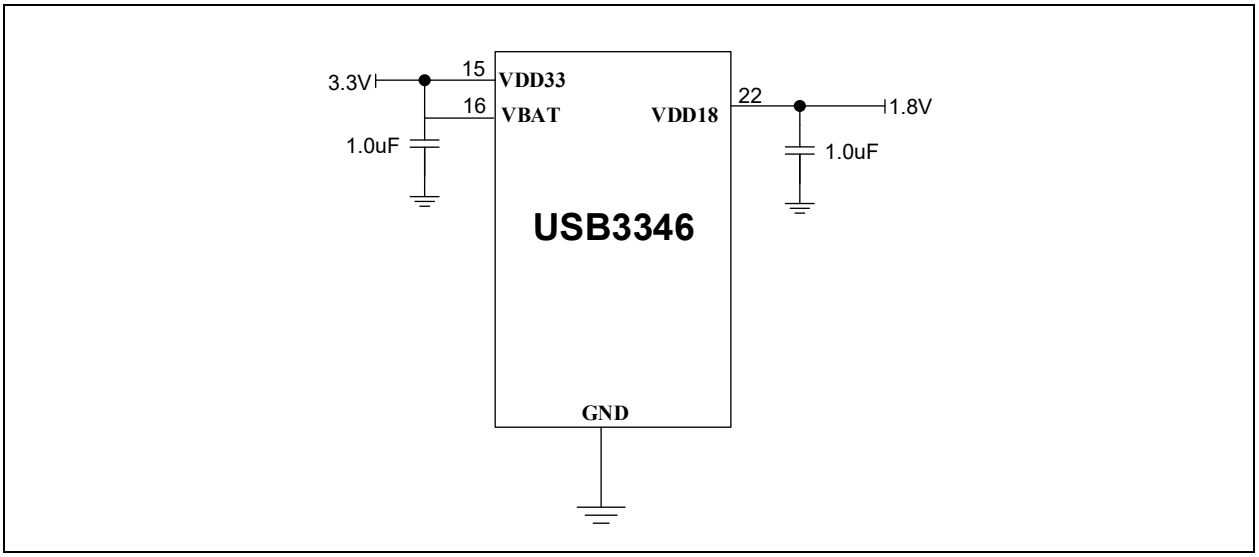
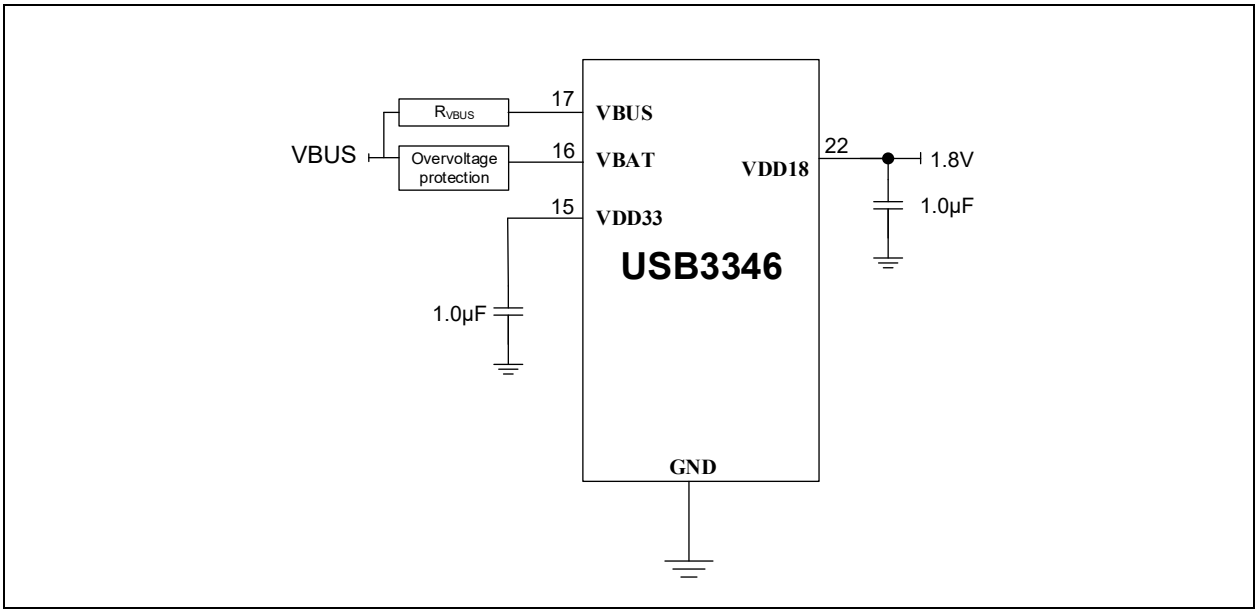


FIGURE 3-3: POWER AND GROUND CONNECTIONS, VBUS-SUPPLIED



4.0 USB

USB operation is defined by the USB 2.0 Specification. This specification may be obtained from USB Implementers Forum (USB-IF) at www.usb.org. USB3346 implementors should have a copy of the USB 2.0 Specification and should be familiar with its contents.

The USB3346 can be used for the PHY level of a USB peripheral (device) or a USB host, or a USB On-The-Go (OTG) device (capable as either host or peripheral). (See Figure 4-1 and Figure 4-2.) The required behaviors of each are defined in the USB 2.0 Specification.

4.1 USB Signals

- **DP** (pin 13): This is the positive signal of the USB signal pair.
- **DM** (pin 14): This is the negative signal of the USB signal pair.
  - **DP** and **DM** signals should have controlled impedance. Control the single-ended characteristic impedance (Z0) of USB signals to between 40Ω and 55Ω. Control the differential impedance (Zdiff) of the DP/DM signals to 90Ω, +5/–10Ω.
- **VBUS** (pin 17): This is the VBUS signal. The USB3346 uses this pin for the VBUS comparator inputs and for VBUS pulsing during session request protocol.
  - R_{VBUS} may be installed in this configuration to assist in protecting the **VBUS** pin. An R_{VBUS} of 820Ω will protect against VBUS transients up to 8.5V. An R_{VBUS} of 10 kΩ will protect against transients up to 10V.
  - C_{VBUS} is a transient-suppressing capacitor that is required for USB 2.0 compliance. For a USB 2.0 host, the recommended value for C_{VBUS} is 120 µF. For a USB 2.0 device, the recommended value for C_{VBUS} is 1 µF. C_{VBUS} should be located near the USB receptacle and nearer to the receptacle than R_{VBUS}.
- **ID** (pin 18): This is the ID input used for USB On-The-Go (OTG) applications. In OTG applications, the ID pin is connected to the ID pin of the OTG-compatible USB Connector and is used to determine the type of USB cable that is connected.
  - When connected to a non-OTG device or an OTG B-Device, this pin floats and is pulled up by an internal resistor.
  - When connected to an OTG A-Device, the ID pin is pulled to the ground by the device.

FIGURE 4-1: USB CONNECTIONS IN A PERIPHERAL APPLICATION

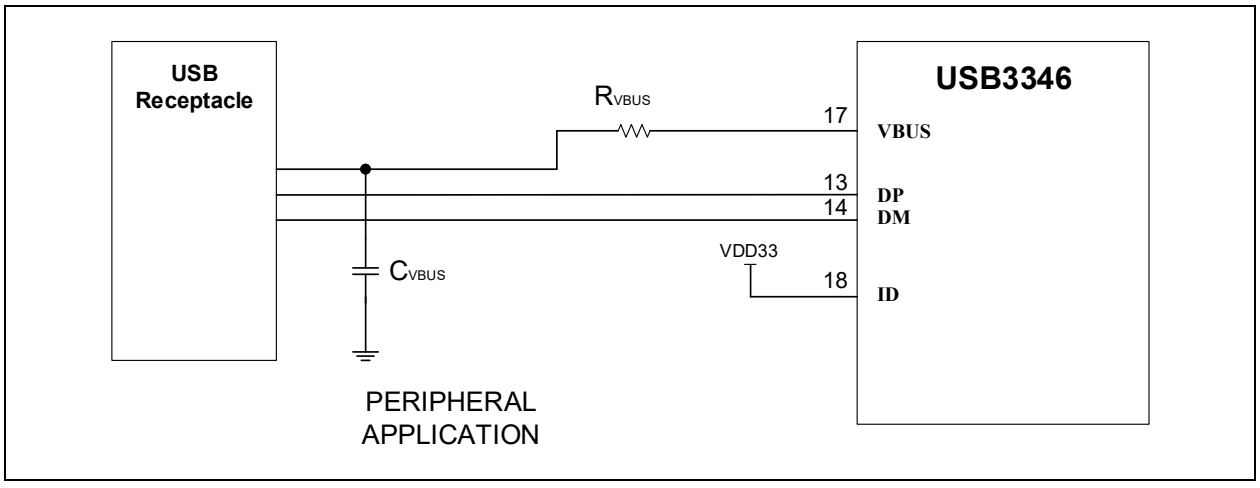
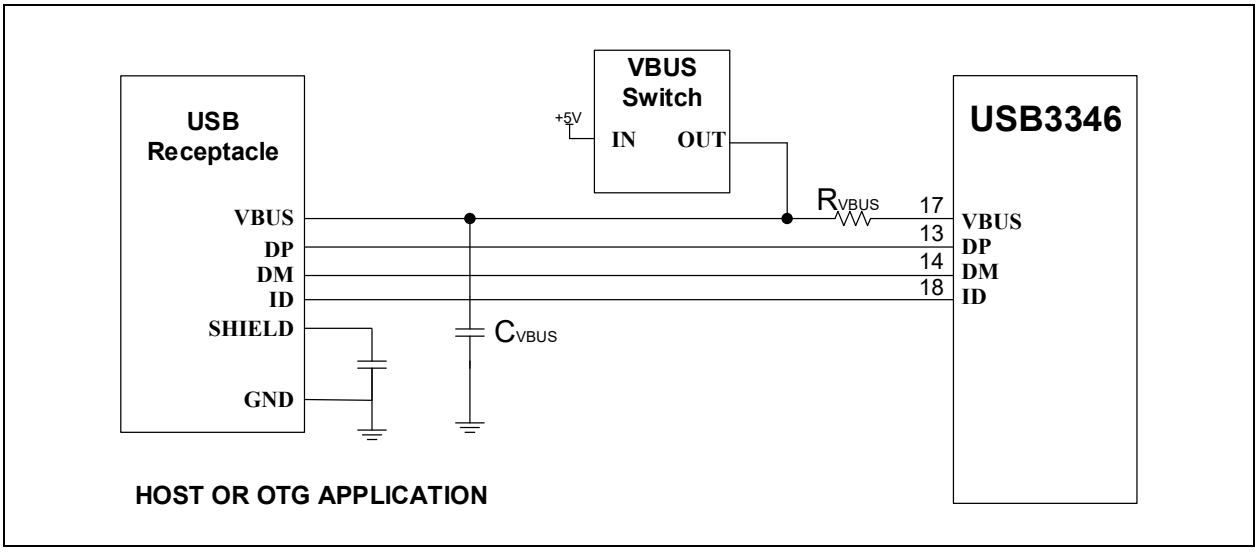


FIGURE 4-2: USB CONNECTIONS IN A HOST OR OTG APPLICATION



4.2 VBUS Switch

The USB 2.0 host or OTG applications must be able to provide 5V on **VBUS** to supply power to USB devices that are attached. The current requirement varies considerably. The USB 2.0 Specification should be consulted for a complete explanation of the VBUS power requirements:

- 100 mA is required for all devices at connection and for low-power, bus-powered devices.
- 500 mA is required for high-power, bus-powered devices.
- As much as 5A total may be required for battery charging and other device circuits.

USB3346 supports these requirements by means of an external 5V switch. The VBUS switch connects a 5V supply to **VBUS** under ULPI register instruction and can detect the current that is supplied through **VBUS**.

The VBUS switch should feature current detection. To be compliant with the USB 2.0 Specification, the current limit must be no more than 5A.

Factors to consider in selecting a VBUS switch include:

- The current rating of the switch, the current at which the switch asserts the FAULT signal, and the amount of current the system is required to provide
- The capability of the switch to provide protection from reverse currents in the On and Off states

The *USB3346 Data Sheet* contains additional detail regarding the operation of an external VBUS switch by the USB3346.

4.3 ESD and EMI

The use of external components (diodes, capacitors, and inductors) applied to USB signals is not generally recommended unless there is a specific need for such protection. Such components tend to make USB-IF compliance tests more difficult to pass, which can add time and cost to a project. At the same time, USB3346 is tolerant of protection devices that have been designed specifically for USB 2.0 signal application, and which are guaranteed compliant by their manufacturers.

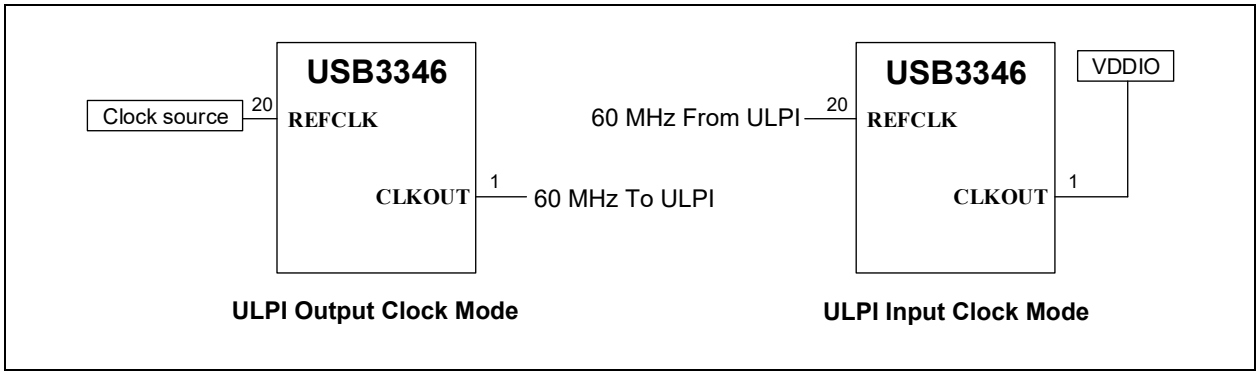
5.0 CLOCK CIRCUIT

5.1 ULPI Clock Modes

The USB3346 is designed to operate in one of two available modes: ULPI Input Clock and ULPI Output Clock.

In the ULPI Input Clock mode, a 60 MHz ULPI clock is driven to the **REFCLK** pin 20. In the ULPI Output Clock mode, the USB3346 generates the ULPI clock to the **CLKOUT** pin 1. The frequency of the ULPI clock is always 60 MHz. See Figure 5-1.

FIGURE 5-1: ULPI CLOCK MODES

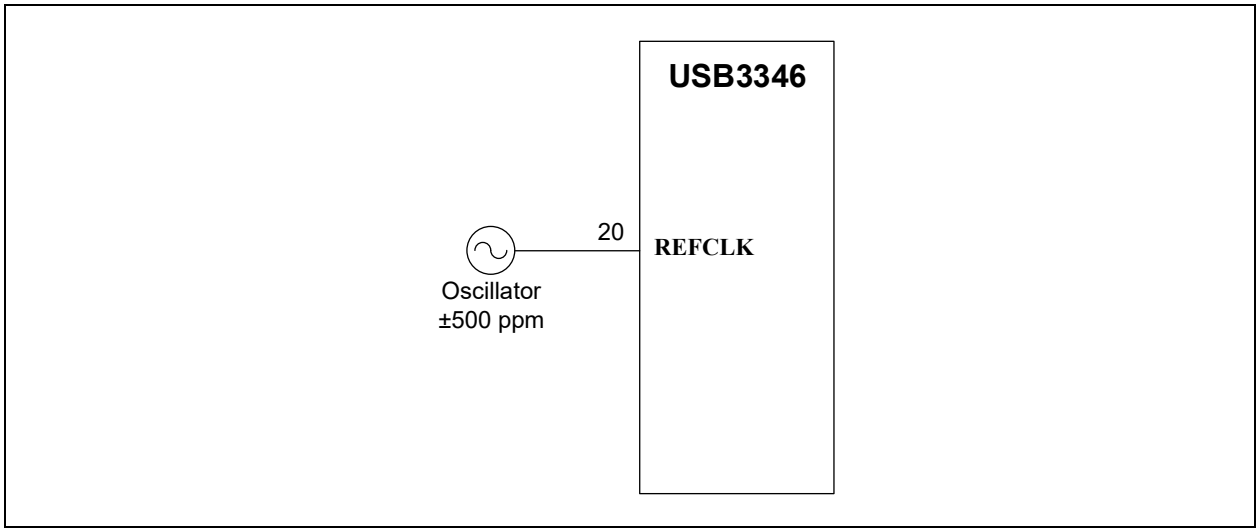


5.2 Reference Frequency

The USB3346 can receive an external reference frequency. In addition, the USB3346 has the ability to either receive or provide the ULPI clock. When the USB3346 is in the ULPI Input Clock mode, the ULPI clock is applied to **REFCLK** and the frequency is always 60 MHz.

See Figure 5-2.

FIGURE 5-2: OSCILLATOR AND CLOCK CONNECTIONS



6.0 ULPI INTERFACE

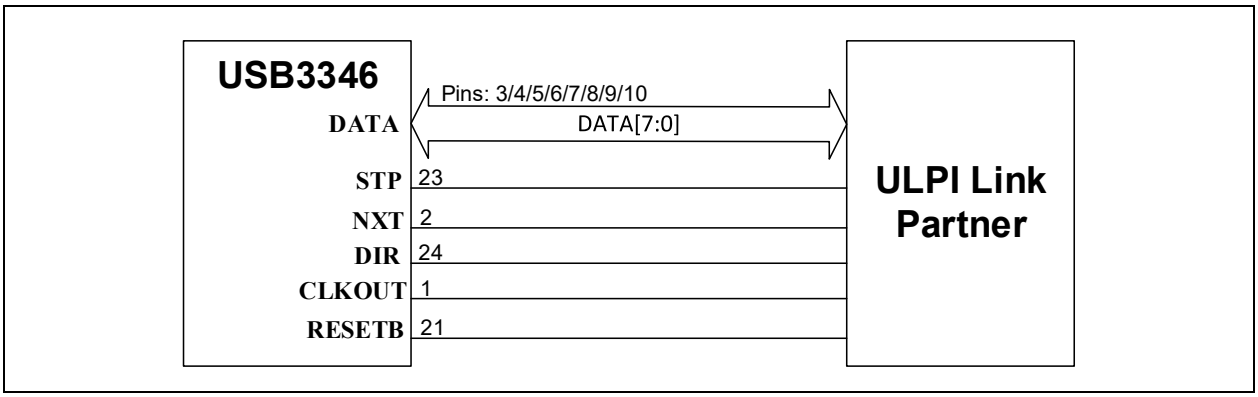
- The ULPI interface connects the PHY layer (USB3346) to the LINK layer. The LINK layer consists of an ASIC, FPGA, or other SOC combined with the LINK layer firmware. The ULPI interface is a single-ended, bidirectional bus that operates at 60 MHz. Refer to Table 6-1 and Figure 6-1.

TABLE 6-1: ULPI SIGNALS

ULPI Signal	Description
DATA[7:0]	Bidirectional data signals
STP	Input from the link layer
DIR	Output to the link layer
NXT	Output to the link layer

- The ULPI interface is intended to cover short distances between integrated circuits on the same PCB. It is not expected to operate through connectors or a cable.
- ULPI DATA traces should be of similar length although precisely equal lengths are not required.
- ULPI traces should not have stubs or components to V_{CC} or ground (such as capacitors).
- ULPI operation is covered in the *USB3346 Data Sheet* and in the *AN19.17 Application Note*.

FIGURE 6-1: ULPI CONNECTIONS



7.0 STARTUP

7.1 Reset Circuit

The **RESETB** (pin 22) is an active-low transceiver Reset. The use of the **RESETB** pin is optional. The state of this pin may be changed asynchronously to the clock signals. When asserted for a minimum of 1 ms and then deasserted, the ULPI registers are reset to their default state and all internal state machines are reset.

The LINK must drive the **RESETB** pin to the desired state at all times (including system start-up), or connect the **RESETB** pin to **VDDIO**.

8.0 MISCELLANEOUS

8.1 RBIAS Resistor

The **RBIAS** (pin 19) on the USB3346 must connect to the ground through a 6.06 kΩ resistor with a tolerance of +/–1.0%. This is essential to the correct setup of critical bias currents.

8.2 Connector Selection

The normal connector type selection is based on the role of the USB3346.

- For a host, a Type-A receptacle is used.
- For a device, a Type-B, Mini-B, or Micro-B receptacle is used.
- For a system that implements a Type-C port, either Host or Device mode may be implemented. The system integrator must ensure that the Type-C port role and the mode of operation of the PHY are also in alignment.

For USB 2.0 Specification compliance, the designer should select a USB receptacle to which the USB Integrators Forum has assigned a Test Certification ID (TID). TID numbers that exist for connectors are listed at https://usb.org/products.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required References"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
Section 3.0, "Power"		Each **VDD33** pin is supplied between 3.0V and 3.6V.		
		For internal VDD33 regulation, 1.0 µF is present on **VDD33**.		
		For external VDD33 regulation, 1.0 µF is present on **VDD33**.		
		A capacitor of 1.0 µF is present on the **VDD18.**		
		VDD18 is not connected to other devices.		
Section 4.0, "USB"	Section 4.0, "USB"	A copy of the USB 2.0 Specification has been downloaded from www.usb.org.		
	Section 4.1, "USB Signals"	**DP** and **DM** are routed with differential impedance of 90Ω.		
		DP and **DM** are routed with single-ended impedance of 40Ω to 55Ω.		
		VBUS is connected to **CVBUS** of 120 µF if host, otherwise 1 µF. **CVBUS** is located near the USB receptacle.		
		VBUS is connected with optional **RVBUS** no greater than 10 kΩ.		
		For host, **ID** pin is connected to the receptacle.		
	Section 4.2, "VBUS Switch"	A **VBUS** switch has been selected according to system requirements.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 5.0, "Clock Circuit"	Section 5.1, "ULPI Clock Modes" and Section 5.2, "Reference Frequency"	For the internal oscillator, the crystal is rated 500 µW or greater.		
		For internal oscillator, the loading capacitors match the crystal manufacturer's specification.		
		For the internal oscillator, the crystal or capacitor traces are short.		
		If crystal is used, it should be rated for a drive level of at least 500 µW at +/– 500 ppm.		
		For the external oscillator, the signal amplitude is 0V to 3.3V (nominal).		
Section 6.0, "ULPI Interface"		ULPI DATA signals are of similar length to the extent practical.		
		ULPI DATA signals have no stubbing (parallel) components connected.		
		No ULPI signal is connected to a header or external connection.		
		ULPI DATA signals do not traverse stubbing vias.		
Section 7.0, "Startup"	Section 7.1, "Reset Circuit"	If **RESET** is to be driven, the signal complies with the data sheet (Section 6.1.11).		
		If **RESET** is not to be driven, the pin is connected to **VDD33**.		
Section 8.0, "Miscellaneous"		**RBIAS** resistor is 8.06 kΩ ±1.0%.		
		In layout, the ground flag is connected with at least nine vias in a square pattern.		
		In layout, gas blocking or venting techniques have been implemented in the ground flag vias.		
		In layout, the guidance of *AN26.21* and *AN18.15* has been followed.		
		The USB receptacle has a TID assigned by USB-IF.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004418A (02-24-22)	Initial release	

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