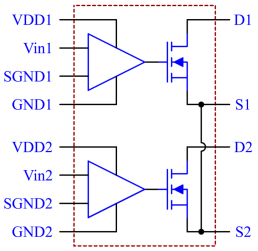
1000 V, 30 MHz, 2000 W RF Power MOSFET-Driver Hybrid

DRF1301

Product Overview

1000 V RF Power MOSFET-Driver Push-Pull Hybrid: 2000 W at 13.56 MHz



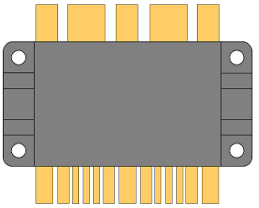


Table 1. Ordering Information

Catalog Part Number (CPN)	Package	Packing Media	Qualification
DRF1301	T4	Box	Industrial

Features

- Switching frequency: DC to 30 MHz
- Low pulse width distortion
- 1 V CMOS Schmitt trigger input with 1 V hysteresis
- Isolated backside to 1000 V
- RoHS compliant

Benefits

- High efficiency
- Lower cost, more compact system than non-integrated driver and MOSFET
- Excellent thermal performance for high power density

Applications

- Class-D, Class-E RF generators
- Switch-mode power amplifiers
- Plasma
- Pulse generators
- CO_2 lasers
- Semiconductor capital equipment
- Flat-panel displays, industrial glass, photovoltaic
- Induction heating, defrosting, drying
- Hazardous or toxic gas, waste treatment
- Lighting
- Ignition
- Ultrasonic cavitation

1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device. T_C = 25 °C unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_{DD}	Maximum driver supply current	15	A
V_{DD}	Driver power supply voltage	15	V
V_{in}	Input voltage	–5.0 to V_{DD} + 0.3	
V_{DSS}	Drain-source voltage	1000	
I_D	Continuous drain current	18	A
I_{D_PK}	Peak drain current[1]	20	A
f	Maximum operating frequency	30	MHz

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

1.2 Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance (per MOSFET)		0.15	0.16	°C/W
Q	Heat dissipation (per MOSFET)			938	W
T_J	Operating junction temperature	–55		175	°C
T_A	Operating ambient temperature			125	
T_{STG}	Storage temperature	–40		125	
Wt	Package weight		9.8		g

ESD practices should comply with JESD-625.

1.3 Electrical Performance (per Driver-MOSFET Section)

The following table shows the static characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{DD} = 12 V, V_{in} = 0 V, I_{DS} = 250 µA	1000			V
$R_{DS(on)}$	Drain-source on-resistance	V_{DD} = 12 V, I_{DS} = 9 A			1000	mΩ
V_{DD}	Driver power supply voltage		8		15	V
V_{in}	Input voltage		–5.0		V_{DD} + 0.3	
I_{DSS}	Zero-gate voltage drain current	V_{DS} = 1000 V, V_{in} = 0 V			25	µA

.....continued						
Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
I_O	Output current	HV_{DC} = 500 V, P_{out} = 2000 W, Frequency = 13.56 MHz, Duty cycle = 50%			4.5	A

The following table shows the dynamic characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
C_{in}	Input capacitance	V_{DD} = 12 V, V_{DS} = 0 V, V_{in} = 0 V, ƒ = 1 MHz		3.0		pF
C_{oss}	Output capacitance	V_{DS} = 150 V, V_{in} = 0 V, ƒ = 1 MHz		335		
$t_{d(on)}$	Turn-on delay time (50% to 50%)	V_{DD} = 12 V, V_{in} = 0 V to 5 V, R_L = 16.6 Ω, C_L = 0.4 nF		26.9		ns
t_r	Voltage rise time (10% to 90%)			13.4		
$t_{d(off)}$	Turn-off delay time (50% to 50%)			35.3		
t_f	Voltage fall time (90% to 10%)			2.0		
$V_{T(on)}$	Turn-on threshold voltage	V_{DD} = 12 V, V_{in} = 0 V to 5 V ramp	1.75		2.65	V
$V_{T(off)}$	Turn-off threshold voltage	V_{DD} = 12 V, V_{in} = 5 V to 0 V ramp	0.75		1.25	
R_{in}	Input parallel resistance			1.0		MΩ

2. Test Circuits

The following figure shows the test circuits for each driver-MOSFET section of this device.

Figure 2-1. Simplified Circuit Diagram

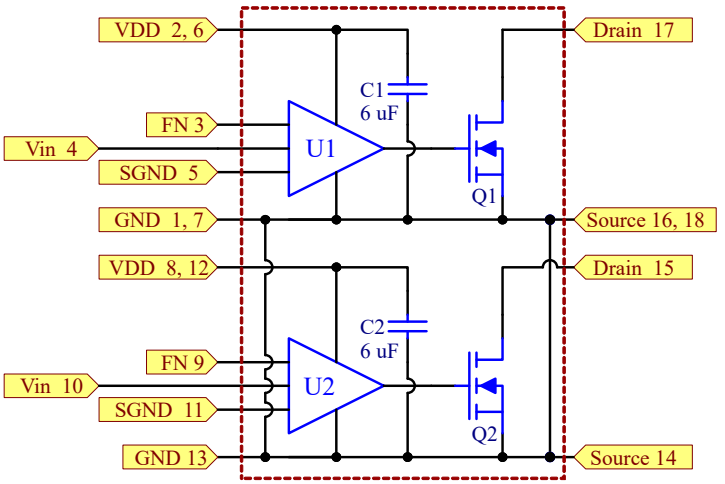
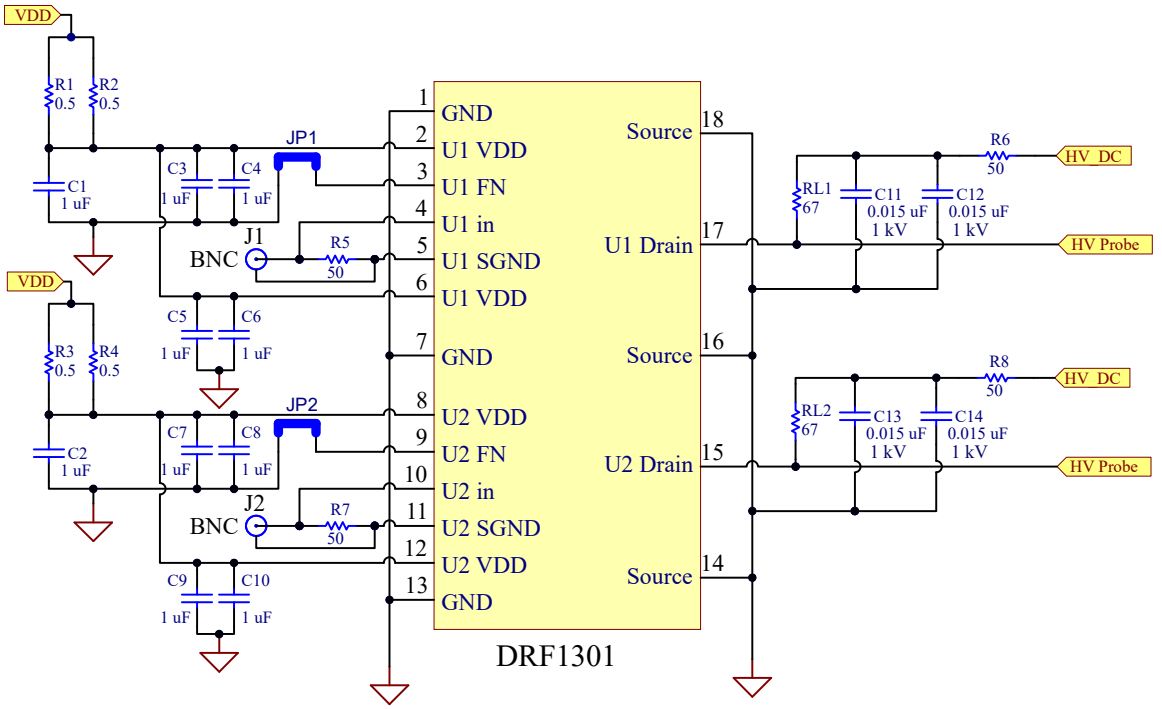


Figure 2-2. Test Configuration



Note:
The test circuit illustrated in Figure 2-2 was used to evaluate the DRF1301 (available as an evaluation board DRF13XX/EVALSW.) The input control signal is applied via VIN and SGND pins using RG188. This provides excellent noise immunity and control of the signal ground currents. The +VDD inputs (pins 2, 6, 8, and 12) should be heavily bypassed by 1 µF capacitors as close to the pins as possible. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load. RL values are set for IDM at VDS max for the load used to evaluate output performance.

The function pin (FN, pin 3 or pin 9) is the invert or non-invert select pin; it is internally held high. See the following table for more information.

Table 2-1. Truth Table (Referenced to SGND)

FN (Pin 3)	V_{IN} (Pin 4)	MOSFET U1	FN (Pin 9)	V_{IN} (Pin 10)	MOSFET U2
HIGH	HIGH	ON	HIGH	HIGH	ON
HIGH	LOW	OFF	HIGH	LOW	OFF
LOW	HIGH	OFF	LOW	HIGH	OFF
LOW	LOW	ON	LOW	LOW	ON

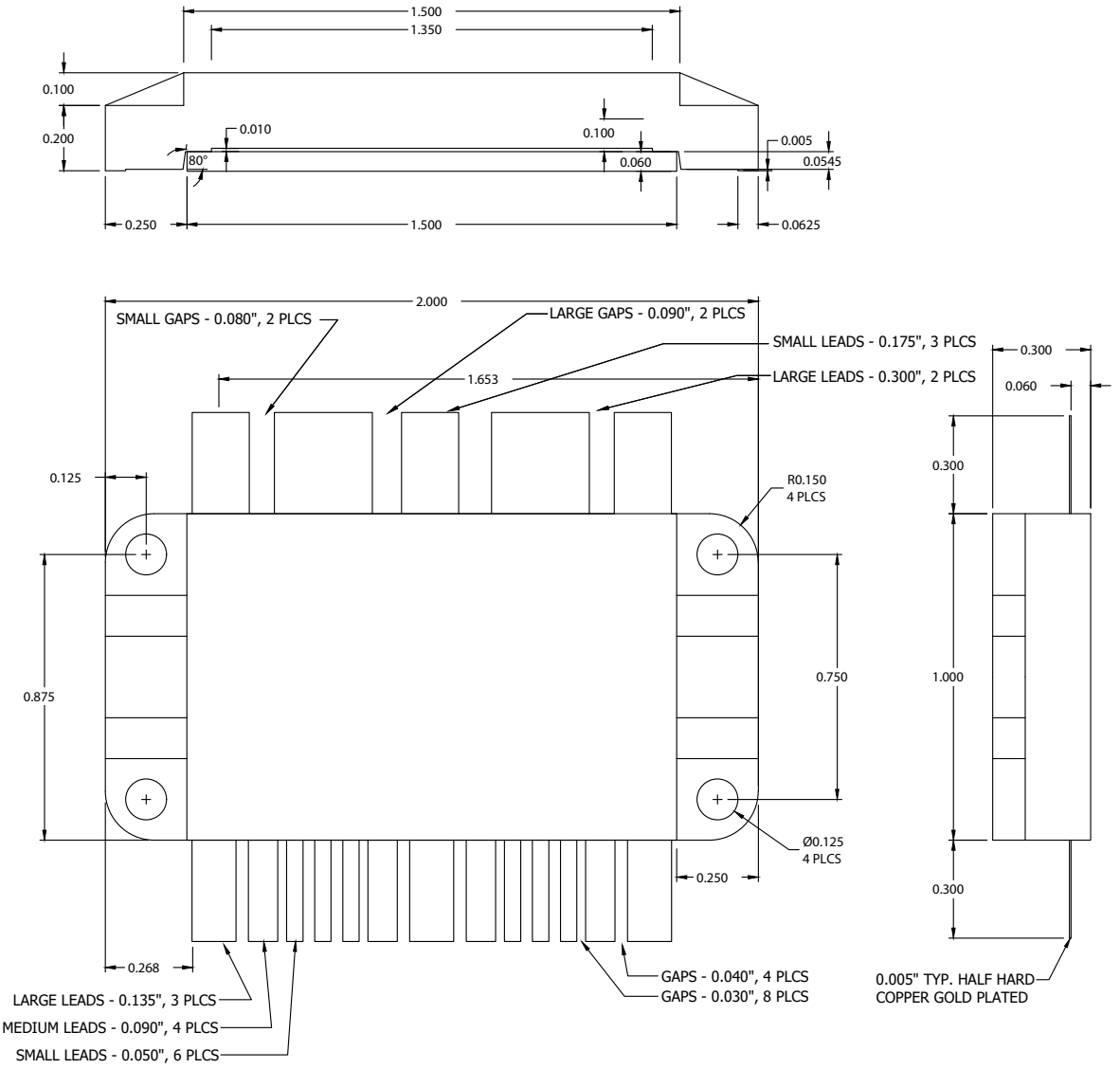
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the package outline of this device. The dimensions in the figure below are in inches.

Figure 3-1. Package Outline Drawing



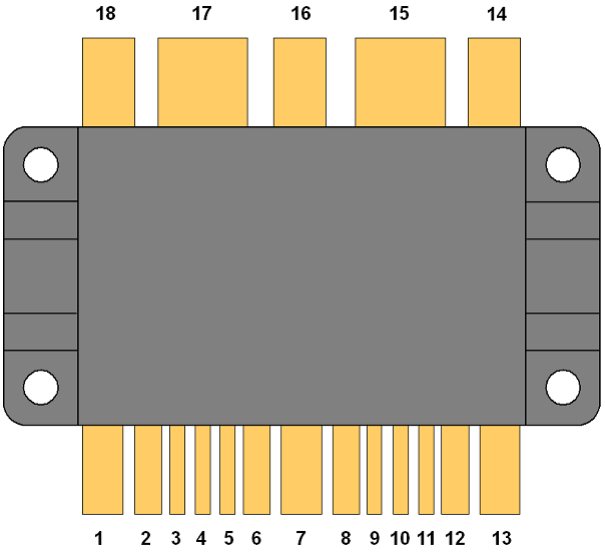
CAUTION

Hazardous Material Warning!

The white ceramic portion of the device between leads and mounting flange is beryllium oxide, BeO. Beryllium oxide dust is highly toxic when inhaled. Care must be take during handling and mounting to avoid damage to this area. These devices must never be thrown away with general industrial or domestic waste.

The following figure ilustrates the pin assignments of this device.

Figure 3-2. Pin Assignments



The following table shows the terminal pinout of this device.

Table 3-1. Terminal Pinout

Pin Assignments	
Pin 1	Ground
Pin 2	U1 $+V_{DD}$
Pin 3	U1 FN
Pin 4	U1 in
Pin 5	U1 SGND
Pin 6	U1 $+V_{DD}$
Pin 7	Ground
Pin 8	U2 $+V_{DD}$
Pin 9	U2 FN
Pin 10	U2 in
Pin 11	U2 SGND
Pin 12	U2 $+V_{DD}$
Pin 13	Ground
Pin 14	Source
Pin 15	U2 Drain
Pin 16	Source
Pin 17	U1 Drain
Pin 18	Source

Note:

- SGND: Signal ground

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
B	02/2025	• Updated Package Outline Drawing. • Added Truth Table to Section 2. • Updated table values in Sections 1.1, 1.3, and 3.1. • Added Pin Assignments image in Section 3.1. • Corrected content in Revision History and added references to Microsemi versions of this datasheet.
A	01/2025	Document migrated from Microsemi template to Microchip template; assigned Microchip literature number DS-00005743A,which replaces the previous Microsemi literature number 050-4975.
Initial Microsemi releases (A–C)	04/2008 – 06/2011	Initial releases.

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