ST M41T11 → MCP7940N Migration

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INTRODUCTION

This migration document describes how to replace the ST M41T11 RTCC with the MCP7940N RTCC.

Note: The MCP7940N has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in manufacturing this device, this device may have different performance characteristics than its earlier version. These differences may cause the device to perform differently in your application than the earlier version.

Note: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

The MCP7940N is an I²C™ RTCC device similar to M41T11. The MCP7940N and M41T11 are available in the standard 8-lead SOIC package.

Table 1 shows considerations that must be taken into account when migrating from M41T11 to the MCP7940N.

TABLE 1: M41T11 – MCP7940N MIGRATION REQUIRED MODIFICATIONS

No.	Required changes	HW	SW	Section Reference
1	External load capacitors required	✓	—	**Crystal Circuit**
2	MCP7940N recommends additional components for the battery backup circuit	✓	—	**Battery Backup**
3	The MCP7940N battery backup function is enabled by setting the VBATEN bit	—	✓	**Battery Backup**
4	MCP7940N can work on 100 kHz and 400 kHz I²C™ frequency versus 100 kHz for M41T11	✓	✓	**Configuring The I²C Bus**
5	MCP7940N and M41T11 have different I²C control bytes	—	✓	**Device Addressing**
6	The MCP7940N MFP pin (FT/OUT on M41T11) has more functions: square-wave, alarms and firmware-controlled output	—	✓	**FT/OUT vs. MFP Functionality**
7	MCP7940N has a dedicated register for the clock calibration. The calibration range and resolution is different for these two devices	—	✓	**Clock Calibration**
8	The MCP7940N oscillator is enabled by a control bit with inverse polarity	—	✓	**Starting the Oscillator**
9	MCP7940N has an automatic leap year indicator. M41T11 does not have leap year indicator, but it has a century bit	—	✓	**Accessing the RTCC and SRAM Registers**
10	Additional control and status bits in the Date and Time registers. SRAM address range changes	—	✓	**Accessing the RTCC and SRAM Registers**

TABLE 2: MCP7940N ADDITIONAL FEATURES

No.	Feature
1	64 bytes of battery-backed SRAM; M41T11 has only 56 bytes of battery-backed SRAM.
2	Two programmable alarms.
3	More package options: 8-lead SOIC, TSSOP, MSOP and 2x3 TDFN.
4	100 kHz and 400 kHz I^2C™ compatible.
5	Power-Up/Down Time-Stamp registers.
6	MCP7940N is available in Extended Temperature Range (-40°C to +125°C)
7	Leap year indication bit.

M41T11 and MCP7940N are electrically compatible. Although there are some differences between the two devices (shown in Table 3), these do not influence the migration process.

TABLE 3: ELECTRICAL DIFFERENCES BETWEEN MCP7940 AND M41T11

No.	Description	Symbol	Differences	
			MCP7940N	M41T11
1	Supply Voltage	V_{CC}	Industrial (I): 1.8V-5.5V	SO8: 2V-5.5V
				SOH28: 3.3V-5.5V
2	Active supply current	I_{CC}	Read: Max. 300 µA (400 kHz) Write: Max. 400 uA (400 kHz)	Max. 300 uA (100 kHz)
3	V_{BAT} Battery Voltage	V_{BAT}	1.3-5.5V (Typ. 3V)	2.5-3.5V (Typ. 3V)
4	V_{BAT} Change Over	V_{TRIP} (V_{SO} on M41T11)	Typ. 1.5V	V_{BAT}-0.5V
5	V_{BAT} Current (V_{BAT} = 3.0V)	I_{BAT}	Typ. 700 nA	Typ. 800 nA
6	Crystal Selection	—	6-9pF (external capacitors required)	12.5pF (includes internal capacitors)

SCHEMATIC RECOMMENDATIONS

The differences between the schematics of MCP7940N and M41T11 are the load capacitors (CX1 and CX2), the battery backup circuit and the pull-up resistors for the I^2C bus.

The recommended connections for the MCP7940N and M41T11 devices are shown in Figure 1 and Figure 2.

FIGURE 1: RECOMMENDED CONNECTIONS FOR M41T11 DEVICES

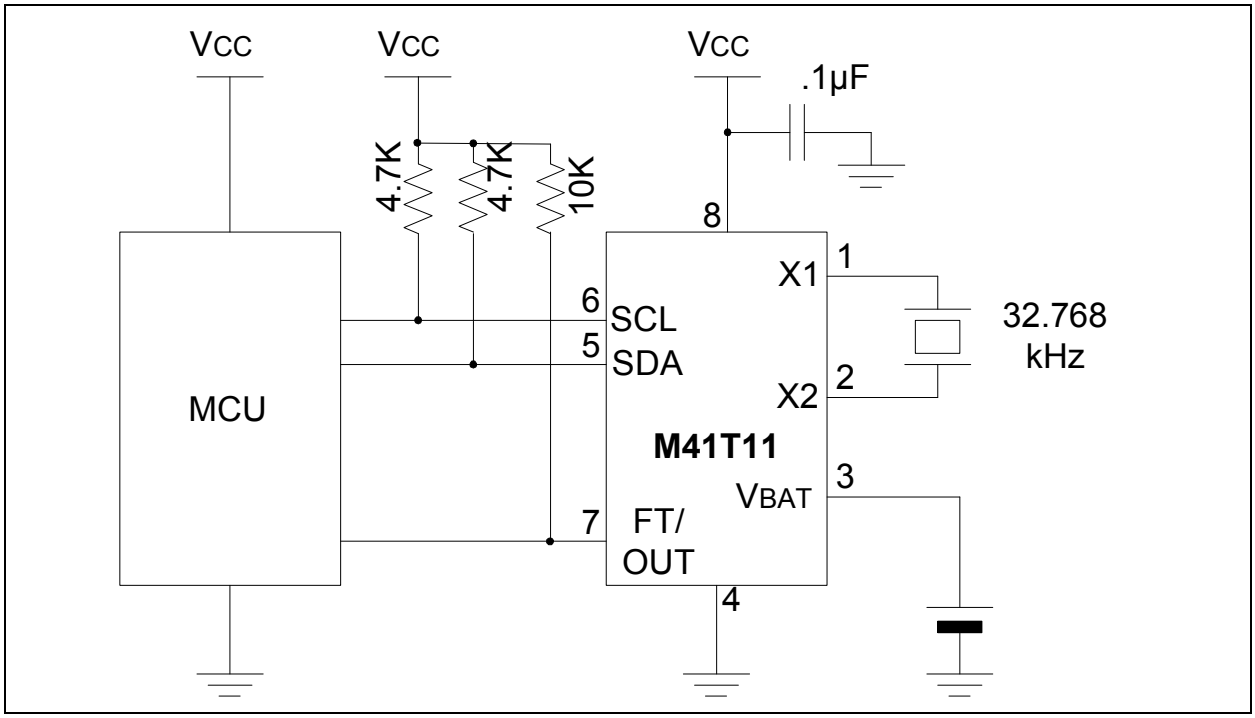
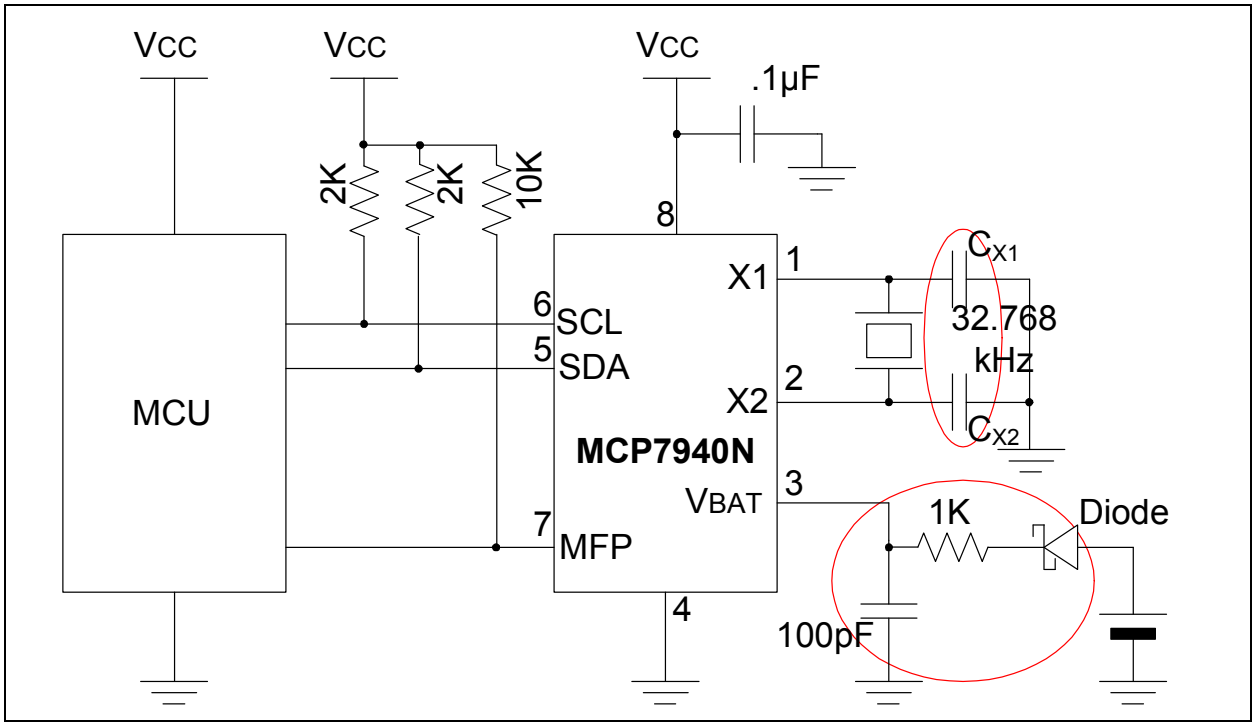


FIGURE 2: RECOMMENDED CONNECTIONS FOR MCP7940N DEVICES



CRYSTAL CIRCUIT

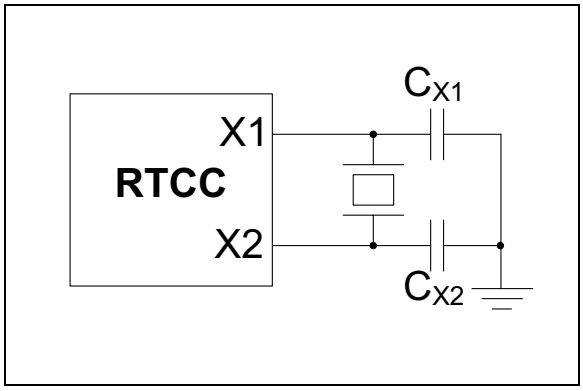
M41T11 is designed to use 32.768 kHz crystals with 12.5pF load capacitance. The CX1 and CX2 capacitors are internal.

Figure 3 shows the MCP7940N schematic for the oscillator circuit (this device does not have internal load capacitors, which must be included on the PCB). It has been designed to operate with a standard 32.768 kHz tuning fork crystal with a load capacitance of between 6-9pF.

Microchip recommends several crystals for which MCP7940N works reliably. For more information, please consult the following documents:

- AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"* (DS01365)
- MCP7940N Data Sheet (DS25010)

FIGURE 3: OSCILLATOR DIAGRAM



BATTERY BACKUP

MCP7940N and M41T11 devices both have an automatic switchover from VCC to VBAT, backup supply, to maintain the RTCC and SRAM during a VCC power fail.

The M41T11 battery backup feature is always enabled in hardware. On the MCP7940N, the battery backup feature is controlled by the VBATEN bit (bit 3) in the Day register (0x03). The VBATEN bit should be set to '1' to match the functionality of the M41T11. This bit is cleared by default on the MCP7940N.

Note: If the battery backup function is not enabled, the SRAM content will be lost and RTCC will be reset when VCC drops to VTRIP. If the device is operating in Battery Backup mode and the VBAT drops to the minimum voltage (see Table 3, VBAT parameter), the entire SRAM and RTCC data will no longer be preserved during power loss.

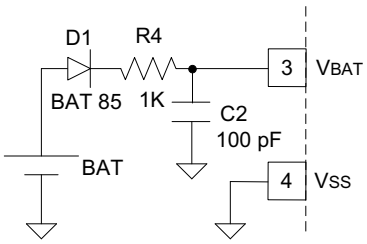
The MCP7940N and M41T11 are fully accessible through the serial interface while VCC is higher than VTRIP/VSO. After VCC drops to VTRIP/VSO, the devices will be powered by VBAT, only to maintain the RTCC and SRAM data contents (Table 4).

TABLE 4: VBAT vs. VCC

Device	Supply Condition	Serial Access	Powered By
M41T11	VCC > VSO	Yes	VCC
	VCC < VSO	No	VBAT
MCP7940N	VCC > VTRIP	Yes	VCC
	VCC < VTRIP	No	VBAT

Note: The VTRIP parameter on MCP7940N is typically 1.5V. On M41T11, the VTRIP parameter is named VSO and is typically VBAT - 0.5V (VBAT = 3V typically).

FIGURE 4: BATTERY BACKUP



When using any supply, it is recommended to include a 1K series resistor, R4 and a 100pF capacitor, C2, between the supply and the VBAT pin (as seen in Figure 4). This is required to remove the spikes that can occur when switching from VCC to VBAT.

Additionally, a series diode, D1, is recommended when using a battery to eliminate any current flowing into the cell during a catastrophic failure. For more information, see AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"* (DS01365).

CONFIGURING THE I²C BUS

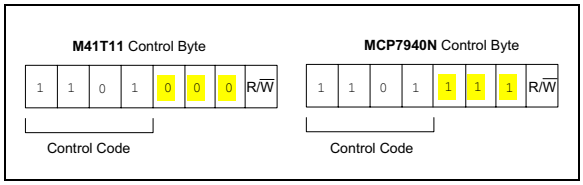
The MCP7940N is I²C 100 kHz and 400 kHz compatible (the M41T11 operates in the Standard mode – 100 kHz only). The SDA and SCL pins are open-drain terminals, therefore, they require pull-up resistors to VCC (typically 10 kΩ for 100 kHz and 2 kΩ for 400 kHz).

If the 400 kHz frequency is used, the master device must be configured to communicate at this increased speed.

DEVICE ADDRESSING

M41T11 and MCP7940N devices are I²C standard compatible, only the control bytes are different (as shown in Figure 5).

FIGURE 5: ADDRESS SEQUENCE BIT ASSIGNMENTS



The MCP740N control byte for accessing the SRAM and RTCC registers is set to '1101111x' (0xDF for a read, 0xDE for a write). The RTCC registers and the SRAM share the same address space.

The control byte for M41T11 is different, '1101000x' (0xD0 for a write, 0xD1 for a read operation).

FT/OUT vs. MFP FUNCTIONALITY

The FT/OUT pin from the M41T11 is called MFP on the MCP7940N. FT/OUT and MFP pins can be used to output a square-wave signal with a programmable frequency or toggled via the control bit, OUT. Alternatively, MFP can be asserted when the alarm is triggered.

On power-up, the FT/OUT and MFP pins have the same default state polarity.

TABLE 5: FT/OUT AND MFP DEFAULT STATE POLARITY

Device	Pin No.	Pin Name	Power-Up State
M41T11	7	FT/OUT	High
MCP7940N	7	MFP	High

The MFP pin functionality is controlled by the Control register, similar to FT/OUT on the M41T11.

TABLE 6: M41T11 AND MCP7940N CONTROL REGISTER

Device	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
M41T11	07h	OUT	**FT**	**S**	**Calibration**				
MCP7940N	07h	OUT	**SQWE**	**ALM1**	**ALM0**	**EXTOSC**	**RS2**	**RS1**	**RS0**

Note 1: Set the ALM1, ALM0, RS2, RS1, RS0, and EXTOSC to '0' to match with the M41T11 functionality.

2: SQWE and FT bits have the same function, to generate a square-wave signal. By default, on power-up, the FT and SQWE bits are set to '0'.

3: EXTOSC allows an external 32.768 kHz signal to drive the RTCC.

4: ALM1:ALM0 determines which alarms are active.

5: S is the Calibration sign bit (see **Section "Clock Calibration"**).

When FT/OUT and MFP are not used to generate a square-wave signal, the default state is controlled by the OUT bit (see Table 6). If OUT = 1, then FT/OUT = 1 and MFP = 1; if OUT =0 then, FT/OUT = 0 and MFP = 0.

The SQWE and RS2:RS0 bits control the MFP when it is used to generate a square-wave signal (see Table 7); FT/OUT is controlled by the FT bit.

TABLE 7: CONFIGURE FT/OUT AND MFP TO GENERATE A SQUARE-WAVE SIGNAL

Device	Pin	Control Bits			Square-Wave Frequency
M41T11	FT/OUT	FT = 1			512 Hz
		FT = 0			Disabled
MCP7940N	MFP	SQWE = 1	RS2	RS1:RS0	1 Hz
			0	01	4 kHz
				10	8 kHz
				11	32 kHz
			1	X	64 Hz
		SQWE = 0			Disabled

Note: Calibration Mode — See device data sheet.

CLOCK CALIBRATION

M41T11 and MCP7940N allow calibration of the crystal by adding to or subtracting from the oscillator divider circuit.

On M41T11, the last five bits from the Control register represent the calibration value byte. The sign bit (bit 5 in the Control register) indicates a positive (add cycles, S = 1) or a negative (subtract cycles, S = 0) calibration.

MCP7940N has a dedicated Calibration register (address 08h). The first bit is the sign bit, and the last seven bits represent the calibration byte (each bit gives the ability to add or subtract two clock cycles). If sign bit = 1, cycles are added to the oscillator divider circuit and if sign bit = 0 the cycles are subtracted.

The calibration effect can be seen by generating a square-wave signal on MFP pin.

TABLE 8: CALIBRATION PROCESS ON M41T11 AND MCP7940N

Device	Register Address	Sign Bit	Calibration Value	Calibration Effect	Clock/Bit	Calibration Range	PPM Resolution
M41T11	Control Register (07h)	Bit 5 (S)	Bit4:Bit0	One second of each minute from 2 minutes*Calibration Byte in the 64 minutes cycle	S = 0, -256 clocks S = 1, +512 clocks	- 64 ppm to +128 ppm	+4 ppm, -2 ppm
MCP7940N	Calibration (08h)	Bit 7	Bit6:Bit0	RS2 = 0 Every minute (only one cycle in sixty will be affected) RS2 = 1 Every cycle of the 64 Hz square-wave signal	±2 clocks	-127 ppm to +127 ppm	±1 ppm

Note: For more information, please refer to the MCP7940N and M41T11 data sheets.

When migrating from M41T11 to MCP7940N, the following equation can be used to write initialize the Calibration register:

EQUATION 1:

```
MCP7940N_Calib_Reg = (M41T11_Calib_Value) * 2 * (2 * M41T11_Calib_Sign) + (M41T11_Calib_Sign<< 2);
```

Note:
```
M41T11_Calib_Value = (M41T11_Ctrl_Reg & 0x1F);
M41T11_Calib_Sign = (M41T11_Ctrl_Reg & 0x20);
```

STARTING THE OSCILLATOR

The oscillator in the both RTCC's is enabled by a control bit but the polarity varies between the devices. The enable is bit 7 in the Seconds register (0x00). On power-up, the MCP7940N oscillator is stopped.

Device	Bit Name	State	Reset State
M41T11	ST (Stop Oscillator)	1=disable oscillator 0=enable oscillator	0
MCP7940N	ST (Start Oscillator)	1=enable oscillator 0=disable oscillator	0

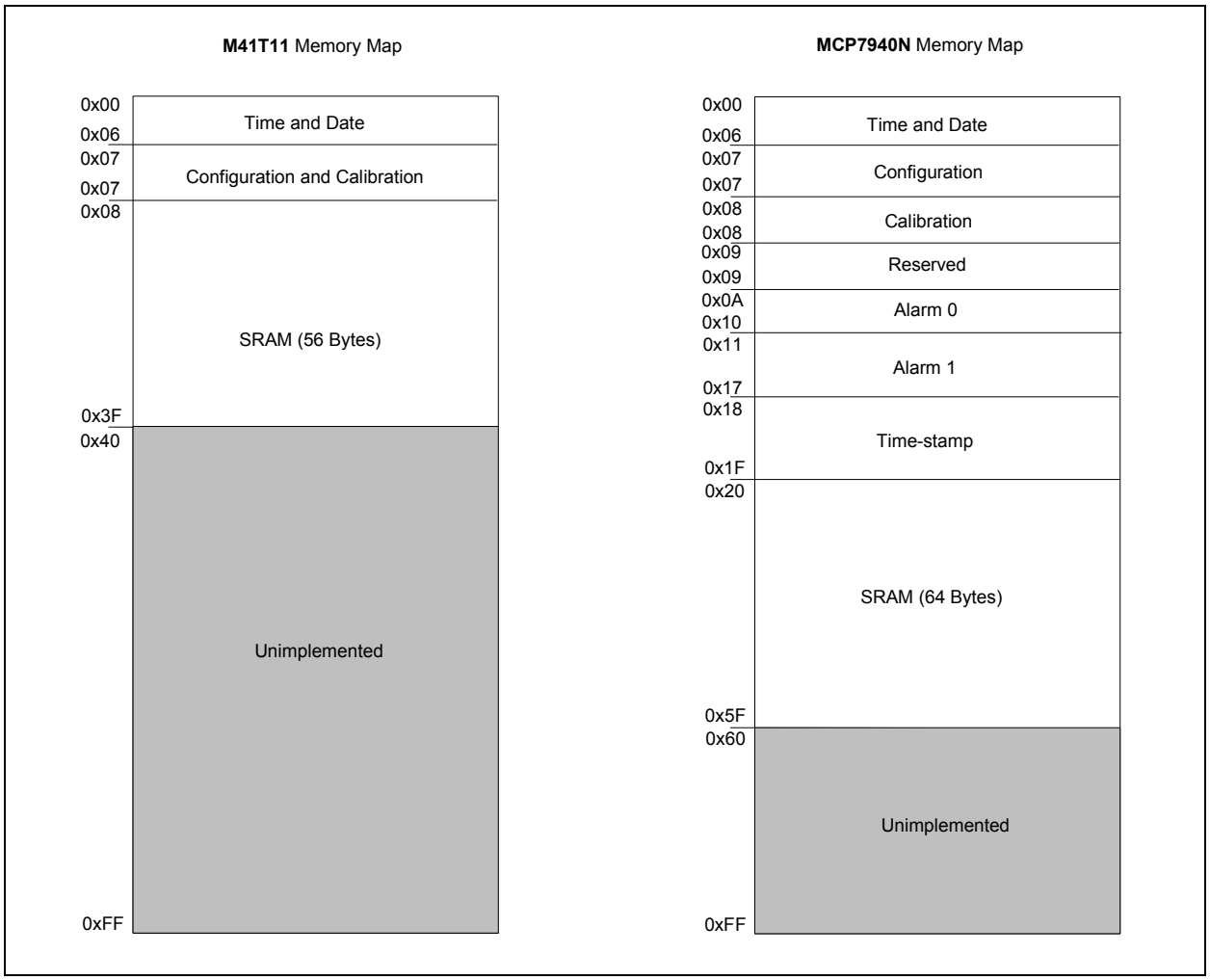
ACCESSING THE RTCC AND SRAM REGISTERS

On M41T11, the 56 bytes of RAM are located in address locations from 08h to 3Fh. These memory locations are used on MCP7940N by the calibration alarms and time-stamp registers.

On MCP7940N, the 64 bytes of RAM are located in address locations 20h to 5Fh.

Differences between the M41T11 and MCP7940N memory maps are shown in Figure 6.

FIGURE 6: M41T11 AND MCP7940N MEMORY MAP



The Date and Time registers are mapped on MCP7940N the same as M41T11 (from 00h to 06h address) with several differences that will be described below. The MINUTES, DATE and YEAR registers are mapped the same as the M41T11.

The DAY register on MCP7940N contains the BCD day and additional bits for configuration and status. The VBATEN bit (bit 3) is used to enable/disable the battery backup. The VBAT bit (bit 4) is set by hardware when the VCC falls and cleared by firmware. The OSCON bit (bit 5) is set and cleared by hardware, indicating if the oscillator is running or not. This is a read-only bit.

The MONTH register has an additional bit, LP (bit 5), which indicates if the current year is a leap one. This is a read-only bit. M41T11 has a Century bit, but does not have a leap year indicator. MCP7940N and M41T11 have automatic leap year correction.

Care should be taken when the Date and Time registers are read or written. A number of the unimplemented “don’t care” bits on DS1307, which read as ‘0’, are used on MCP7940N as control and status bits (they are highlighted in Table 9).

TABLE 9: DATE AND TIME REGISTER MAP FOR MCP7940N

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range	Reset State
Time Registers											
00h	ST	10 Seconds			Seconds				Seconds	00-59	00h
01h		10 Minutes			Minutes				Minutes	00-59	00h
02h	X(2)	12/24(1)	10 Hour AM/PM	10 Hour	Hour				Hours	1-12 + AM/PM 00 - 23	00h
03h	X	X	**OSCON(3, 7)**	**VBAT(4, 7)**	**VBATEN(5,7)**	Day			Day	1-7	01h
04h	X	X	10 Date		Date				Date	01-31	01h
05h	X	X	**LP(6,7)**	10 Month	Month				Month	01-12	01h
06h	10 Year				Year				Year	00-99	01h

Note 1: 12/24 bit determines hour format (set to ‘0’ enables 24-hour format, set to ‘1’ enables 12-hour format). This bit is the CB (century bit) on M41T11.

2: This bit is the CEB (century enable bit) on M41T11.

3: OSCON bit indicates if the oscillator is running or not.

4: VBAT bit is set by hardware when VCC falls.

5: VBATEN bit is used to enable/disable the battery backup.

6: LP bit indicates if the current year is a leap one.

7: The OSCON, VBAT, VBATEN and LP bits are “don’t care” bits on M41T11. The OSCON, VBAT and LP bits are read-only on the MCP7940N.

8: X = Don’t Care.

Note: Shaded areas are not implemented on M41T11.

EXAMPLE 1: READ DATE AND TIME FROM MCP7940N

```
Seconds = (((Seconds_Register & 0x70) >> 4) * 10) + (Seconds_register & 0x0F);
Minutes = (((Minutes_Register & 0x70) >> 4) * 10) + (Minutes_Register & 0x0F);
Hours = (((Hours_Register & 0x30) >> 4) * 10) + (Hours_Register & 0x0F);
Date = (((Date_Register & 0x30) >> 4) * 10) + (Date_Register & 0x0F);
Day = Day_Register & 0x07;
Month = (((Month_Register & 0x10) >> 4) * 10) + (Month_Register & 0x0F);
Year = (((Year_Register & 0xF0) >> 4) * 10) + (Year_Register & 0x0F);
```

EXAMPLE 2: WRITE DATE AND TIME TO MCP7940N

```
Seconds_Register |= ((Seconds / 10) << 4) | (Seconds % 10);
Minutes_Register = ((Minutes / 10) << 4) | (Minutes % 10);
Hours_Register = ((Hours / 10) << 4) | (Hours % 10);
Date_Register = ((Date / 10) << 4) | (Date % 10);
Day_Register |= Day;
Month_Register = ((Month/10) << 4) | (Month % 10);
Year_Register = ((Year /10) << 4) | (Year%10);
```

MCP7940N does not have a Century bit indicator, but a software routine can be used to assert a flag when the century was changed. Therefore, a flag can be toggled when the time is 00:00:00, 01/01/2x01.

NOTES:

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