ZL30292

PCIe Gen 1/2/3/4/5/6 Clock and Platform Timing Generator

Features

- Fully Compliant with PCIe Gen 1/2/3/4/5/6
- 19 Low-Power Push-Pull HCSL PCIe Outputs
  - Seven Dedicated 100 MHz Outputs
  - Three Dedicated 25 MHz Outputs
  - Nine Selectable Outputs: 25 MHz or 100 MHz
  - All Outputs have Embedded 100Ω Differential Series Termination
  - Embedded Source Terminations
- Platform Time Input and Output Clocks
- Ultra-Low Jitter: 80 fs Maximum
- Programmable SSC on 100 MHz Outputs
- Embedded Low Dropout (LDO) Voltage Regulator Provides Superior Power Supply Noise Rejection
- Maximum Output-to-Output Skew of 50 ps
- SMBus and Side-Band Interface
- 3.3V ±10% Power Supply Tolerance Meets PCIe Electromechanical Specification (3.3V ±9%)

Applications

- PCIe Gen1/2/3/4/5/6 Clock Generation
- Platform Tuning
- Intel QPI/UPI
- Servers
- Storage and Data Centers
- Switches and Routers

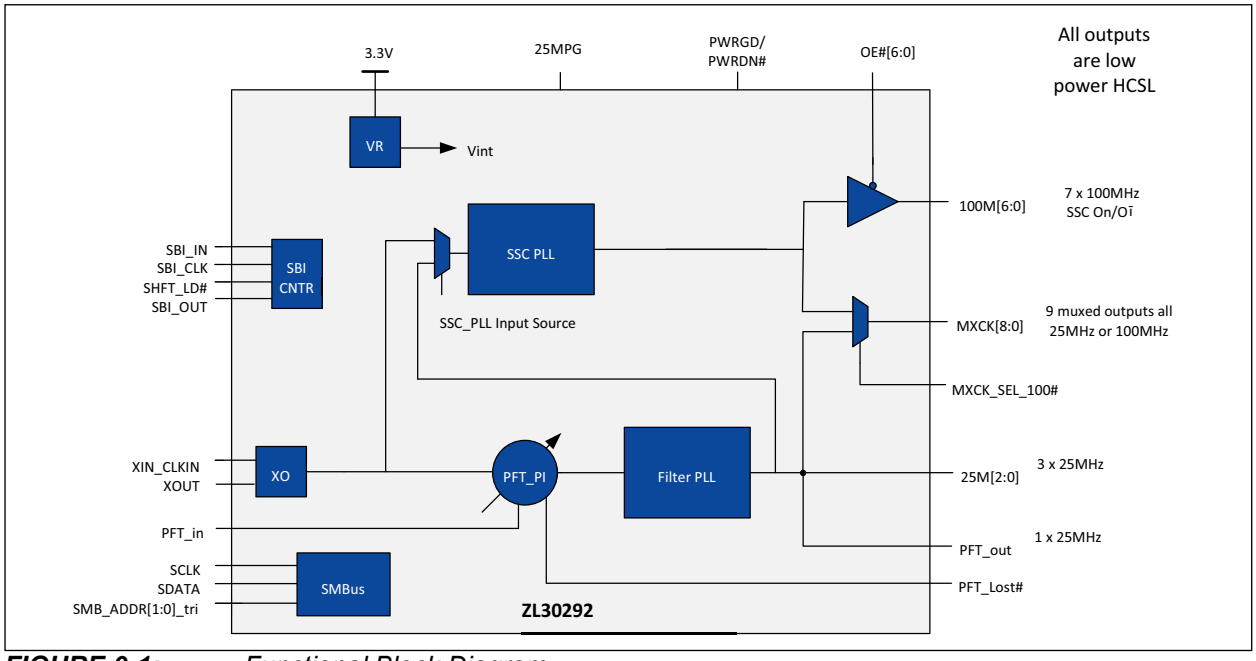

FIGURE 0-1: *Functional Block Diagram.*

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1.0 PIN DESCRIPTION AND CONFIGURATION

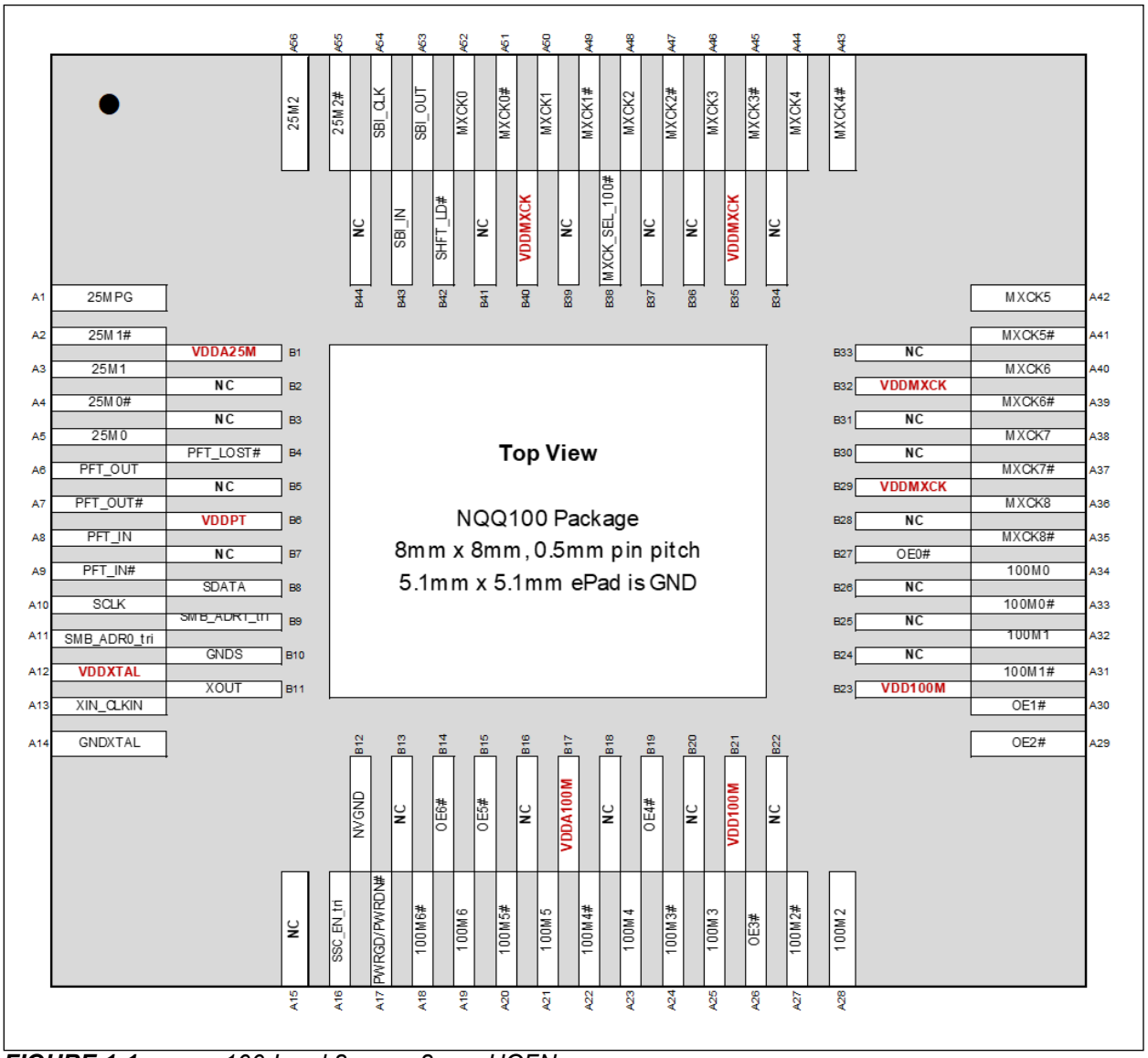


FIGURE 1-1: *100-Lead 8 mm x 8 mm UQFN.*

The I/O column uses the following symbols: I – input, IPDT – Input power down tolerant (must tolerate being driven by external signal while the device is powered down) O – output, OD – open-drain output with internal 120 kΩ pull-up resistor, I/OD – Input/Output Open-Drain pin, NC – No connect pin, P – power supply pin, ITRI – Tri-level input pin.

TABLE 1-1: PIN DESCRIPTIONS

Pin Number	Pin Name	I/O	Description
Crystal Oscillator, Input XO Clock			
A13	XIN_CLKIN	IPDT	**Passive crystal in/out or active CMOS single-ended input for XO** Input frequency 25 MHz. Leave XOUT unconnected when XIN_CLKIN is connected to a crystal oscillator. Please refer to ZLAN-825 for recommendations on Crystal Oscillator Circuit.
B11	XOUT	O	
100 MHz Output Clocks			
A34	100M0	O	**100 MHz Differential Outputs 0 to 6**
A33	100M0#		
A32	100M1		
A31	100M1#		
A28	100M2		
A27	100M2#		
A25	100M3		
A24	100M3#		
A23	100M4		
A22	100M4#		
A21	100M5		
A20	100M5#		
A19	100M6		
A18	100M6#		
25 MHz Output Clock			
A5	25M0	O	**25 MHz Differential Outputs 0 to 2**
A4	25M0#		
A3	25M1		
A2	25M1#		
A56	25M2		
A55	25M2#		

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	I/O	Description	
100 MHz or 25 MHz (Selectable)				
A52	MXCK0	O	**100 MHz or 25 MHz (Selectable) Differential Outputs 0 to 8**	
A51	MXCK0#			
A50	MXCK1			
A49	MXCK1#			
A48	MXCK2			
A47	MXCK2#			
A46	MXCK3			
A45	MXCK3#			
A44	MXCK4			
A43	MXCK4#			
A42	MXCK5			
A41	MXCK5#			
A40	MXCK6			
A39	MXCK6#			
A38	MXCK7			
A37	MXCK7#			
A36	MXCK8			
A35	MXCK8#			
Platform Timing				
A8	PFT_IN	IPDT	**25 MHz Differential Platform Timing Input** Pull down with 10 kΩ resistor or connect to ground, if not used.	
A9	PFT_IN#			
A6	PFT_OUT	O	**25 MHz Differential Platform Timing Output**	
A7	PFT_OUT#			
B4	PFT_LOST#	OD	**This output is asserted when PFT_IN is lost.** If used, pull up with 10 kΩ resistor.	
Hardware Control				
B27	OE0#	I	**Output Enable for 100M Outputs.** Logic level on these pins enables/disables the corresponding output.	
A30	OE1#			
A29	OE2#			
A26	OE3#			
B19	OE4#		OE_n#	100Mn/n#
B15	OE5#		0	Active
B14	OE6#		1	Low/Low both pulled low by 50Ω resistor
B38	MXCK_SEL_100#	I	**MXCK Clock Output Selection** 0: 100 MHz 1: 25 MHz	
A1	25MPG	I	**25M2/25M2# Enable for Platform Boot.** When this pin is pulled high 25M2/25M2# will stay active while PWRDN# is pulled low.	

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	I/O	Description	
A17	PWRGD/PWRDN#	I	**Power up/Power down.** Refer to section PWRGD/PWRDN# for details.	
A16	SSC_En_tri	ITRI	**Tri-level Spread Spectrum Control**	
			SSC_ENABLE Pin	SSC Modulation
			0	Off
			MID	–0.3%
			HIGH	–0.5%
SMBus Control				
A10	SCLK	I	**SMBus Client Clock Input.** Pull down with 10 kΩ resistor or connect to ground, if not used.	
B8	SDATA	I/OD	**Input/Open-Drain SMBus Data.** Pull up as per SMBUS specification.	
A11	SMB_ADDR0_tri	ITRI	**Tri-level Address Selection Inputs** (Please refer to addresses in Table 2-4 and tri-level thresholds in Table 4-2) Pull down with 10 kΩ resistor or connect to ground, if not used.	
B9	SMB_ADDR1_tri			
Side Band Interface				
B43	SBI_IN	IPDT	**Side Band Interface Data.** Pull down with 10 kΩ resistor or connect to ground, if not used.	
A54	SBI_CLK	IPDT	**Side Band Interface Clock.** Pull down with 10 kΩ resistor or connect to ground, if not used.	
B42	SHIFT_LD#	IPDT	**Side Band Shift Register Load** When this pin gets pulled low, the values stored in shift register get loaded to 20-bit SBI Output Enable Control Register. Pull down with 10 kΩ resistor or connect to ground, if not used.	
A53	SBI_OUT	O	**Side Band Interface Output.** Leave unconnected if not used.	
Power and Ground				
B29	VDDMXCK	P	**Positive Supply Voltage for MXCK Outputs.** Connect to 3.3V supply.	
B32				
B35				
B40				
B21	VDD100M	P	**Positive Supply Voltage for 100M Outputs.** Connect to 3.3V supply.	
B23				
B17	VDDA100M	P	**Positive Analog Supply Voltage.** Connect to 3.3V supply	
B6	VDDPT	P	**Positive Supply Voltage for Platform Timing** Connect 3.3V power supply	
B1	VDDA25	P	**Positive Analog Supply Voltage** Connect 3.3V power supply	
A12	VDDXTAL	P	**Positive Supply Voltage for Crystal Oscillator Circuit** Connect 3.3V power supply	
A14	GNDXTAL	P	**Ground for XTAL oscillator** Connect to ground	
B10	GNDS	P	**Ground** Connect to ground	
B12	NVGND	P	**Ground** Connect to ground	
ePad	GND	P	**Ground.** Connect to ground	

TABLE 1-1: PIN DESCRIPTIONS (CONTINUED)

Pin Number	Pin Name	I/O	Description
No Connect Pins			
A15 B2 B3 B5 B7 B13 B16 B18 B20 B22 B24 B25 B26 B28 B30 B31 B33 B34 B36 B37 B39 B41 B44	NC	NC	**No Connect.** These pins are not connected to the die. Leave them open.

2.0 FUNCTIONAL DESCRIPTION

2.1 Applications

ZL30292 is a variant of the ZL30292 CK440Q compliant device. The only difference between ZL30292 and ZL30292 is that the ZL30292 device outputs are conditioned for transmission lines with 85Ω differential characteristic impedance and ZL30292 outputs are conditioned for transmission lines with 100Ω differential characteristic impedance.

ZL30292 is a clock generator/synchronizer that is fully compliant with PCIe Gen 1/2/3/4/5/6 specifications. ZL30292 provides a complete clock solution for PCIe and the platform timing. The following figures show typical applications. For larger servers (typically more than two CPUs) ZL30292 will be used in conjunction with ZL40293/295 (20 ouptput PCIe clock buffers conditioned for transmission lines with 100Ω differential characteristic impedance).

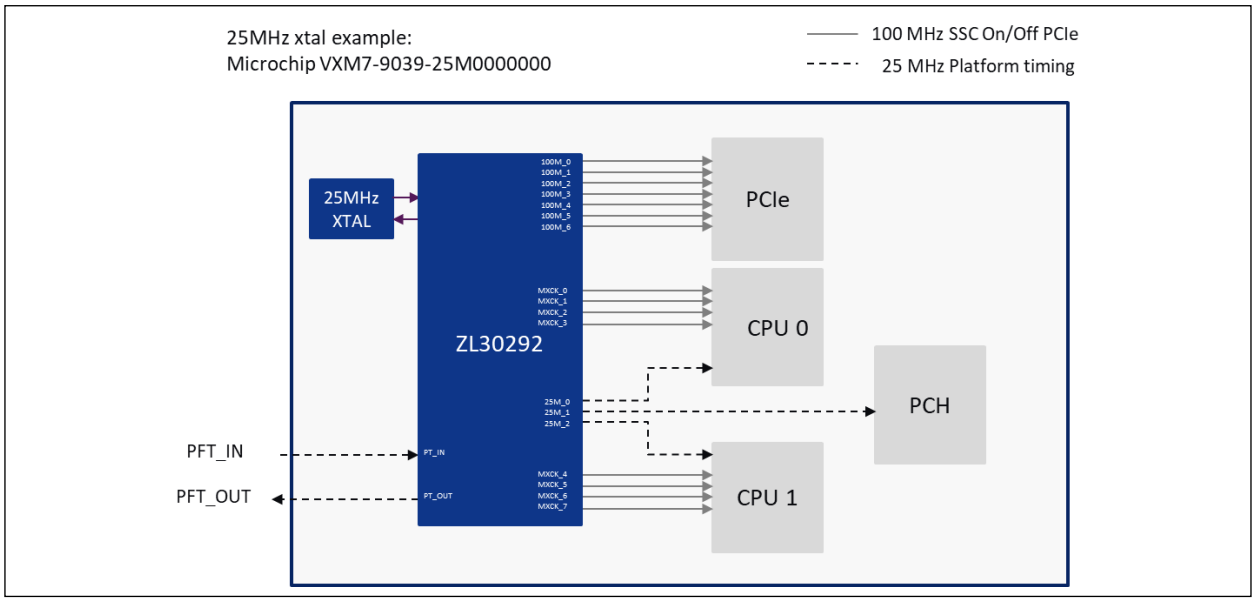


FIGURE 2-1: *Server with Two CPUs.*

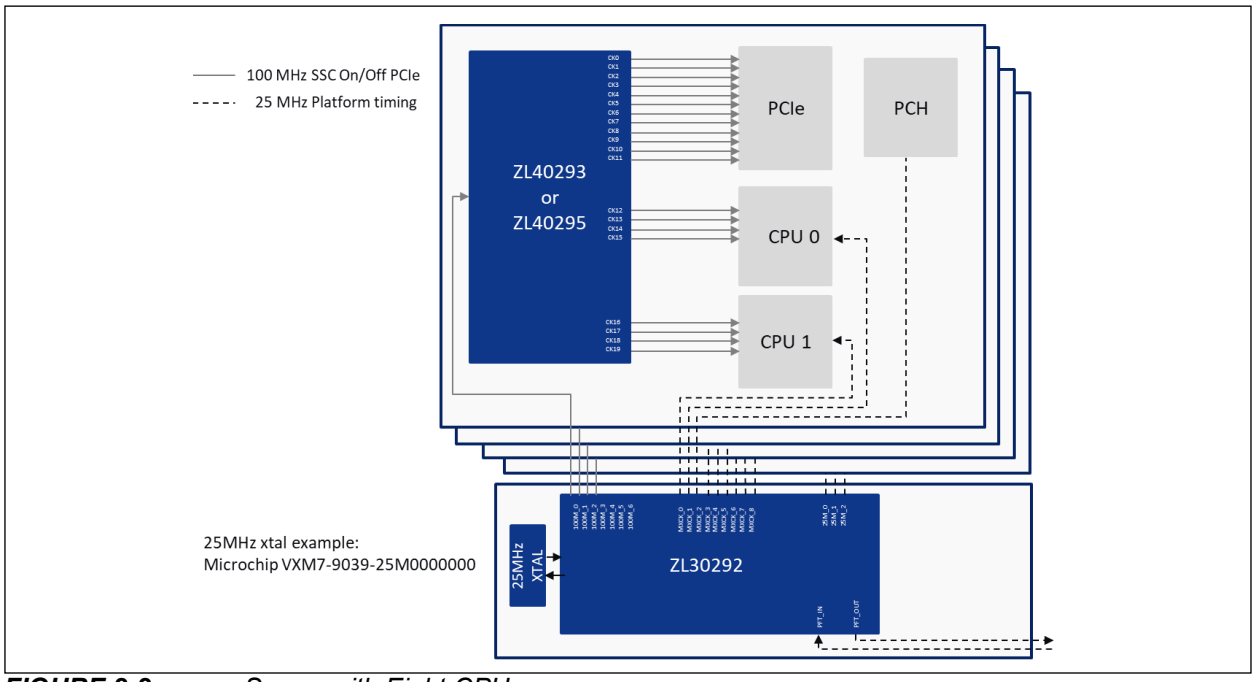


FIGURE 2-2: *Server with Eight CPUs.*

2.2 Functional Description

The ZL30292 is an ultra-low jitter, low power clock generator that is fully compliant with PCIe Gen 1/2/3/4/5/6 specifications.

The device can operate from 3.3V±10% supply to meet PCIe Electromechanical Specification that requires 3.3V supply tolerance of ±9%. Its operation is guaranteed over the industrial temperature range of –40°C to +85°C.

2.3 Platform Timing Clock Input

The following block diagrams show how to terminate different signals fed to the ZL30292 inputs.

The platform timing input (PFT_IN) can be fed with transmission lines of any impedance. The examples below show only 50Ω single-ended, 85Ω differential, and 100Ω differential, which are the most common ones in practice. Figure 2-3 and Figure 2-4 show how to terminate the input when driven from a push-pull and traditional HCSL drivers respectively.

Figure 2-5 shows how to terminate a single-ended output, such as LVCMOS. This example assumes 50Ω transmission line, which is the most common for single-ended LVCMOS signaling. Resistors R1 and R2 are chosen to provide 50Ω termination and proper biasing and $R_O + R_S$ ideally should be 50Ω so that the transmission line is terminated at both ends with its characteristic impedance. If the driving strength of the output driver is not sufficient to drive low impedance, the value of series resistor R_S should be increased. This will reduce the voltage swing at the input but this should be fine as long as the input voltage swing requirement is not violated (Figure 2-5). The source resistors of R_S = 270Ω could be used for a standard LVCMOS driver. This will provide 516 mV of voltage swing for 3.3V LVCMOS driver with load current of (3.3V/2) *(1/(270Ω + 50Ω)) = 5.16 mA. If the strength of output driver is sufficient to support voltage swing above 750 mV, then the biasing voltage determined with R1, R2, R3, and R4 resistors needs to be increased to avoid signal going below 0 volts.

For optimum performance both differential input pins (_p and _n) need to be DC biased to the same voltage. Hence, the ratio R1/R2 should be equal to the ratio R3/R4.

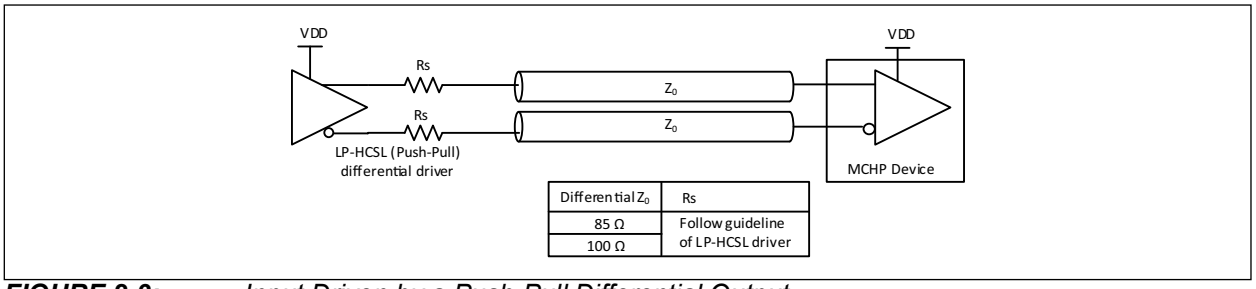


FIGURE 2-3: *Input Driven by a Push-Pull Differential Output.*

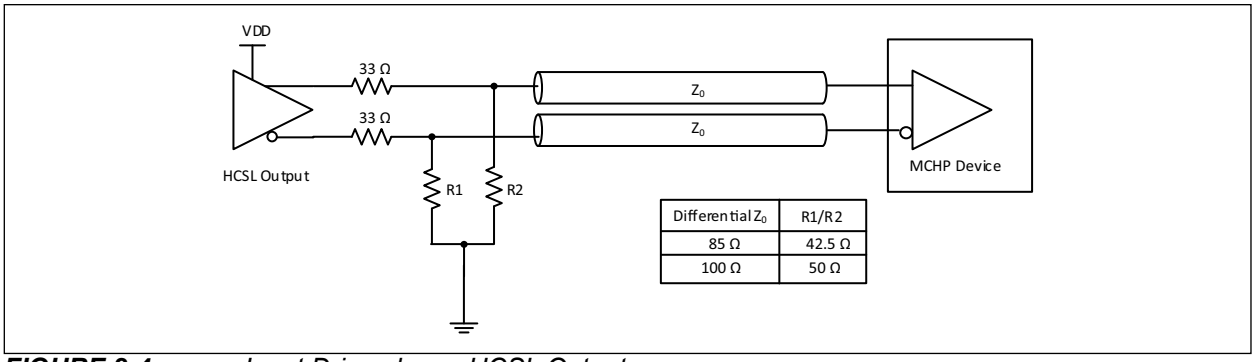


FIGURE 2-4: *Input Driven by an HCSL Output.*

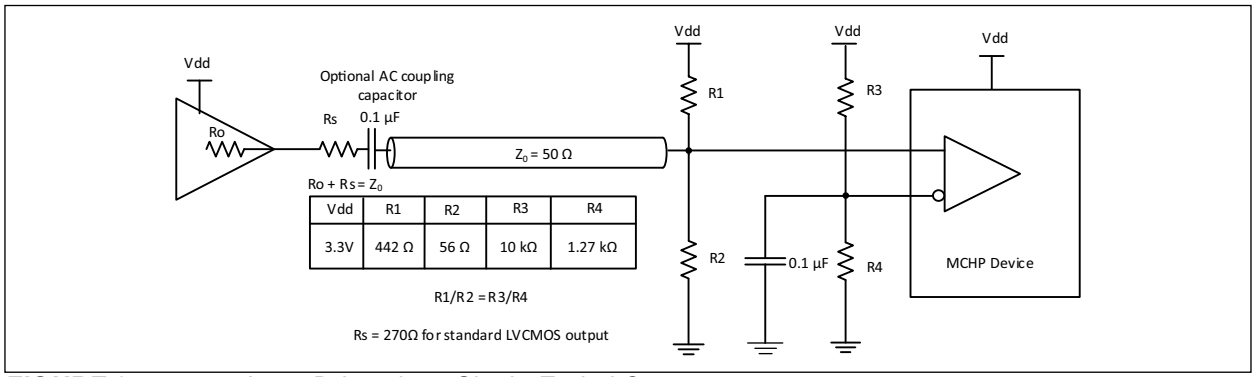


FIGURE 2-5: *Input Driven by a Single-Ended Output.*

2.4 Clock Outputs

Differential outputs have embedded termination resistors as shown in Figure 2-6. This provides significant saving relative to traditional current based HCSL outputs which require four resistors per differential pair.

Embedded series termination resistors are matched for 100Ω differential transmission line.

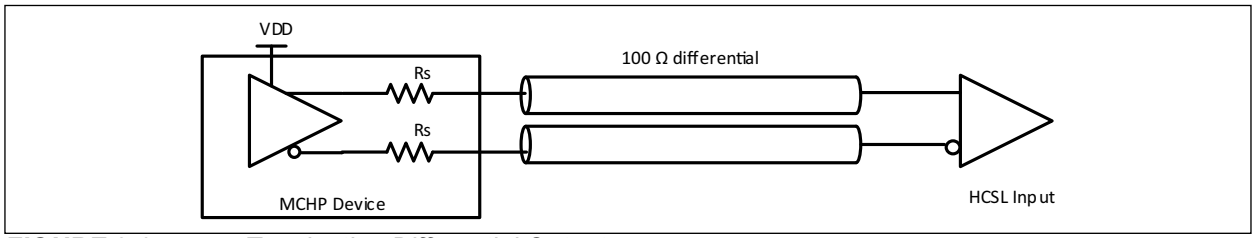


FIGURE 2-6: *Terminating Differential Outputs.*

2.5 Termination of Unused Outputs

Unused outputs should be left unconnected.

2.6 OE# and Output Enables (Control Register)

The ZL30292 has three methods for enabling and disabling outputs. In order for an output to be enabled, all three methods must enable the output. If any method disables the output, the output will be disabled.

The first is the traditional method of OE# pins that are used for PCI Express clock enabling at the PCIe connector. Each of the 7 dedicated 100 MHz clock outputs can be enabled or disabled with the OE[6:0]# pins individually. The OE# pin must be pulled low to enable the output.

The second method is by using the SMBus output enable bits. Any of the 19 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set that can enable or disable the clock outputs. The Output Enable bits in the SMBus registers are active high and are set to enable by default.

The third is using the Side Band Interface (SBI). This is a DB2000QL compatible method of enabling outputs using a hardware shift/load method.

Refer to Table 2-1 for the truth table for enabling and disabling 100M outputs via hardware and software. In addition to the PWRGD/PWRDN# pin, all three output enabling methods must be set to “enable” for the clock to be active on that pin.

Refer to Table 2-2 for the truth table for enabling and disabling MXCK or 25M or PFT_OUT outputs via software. In addition to the PWRGD/PWRDN# pin, both the SMBus method and SBI method must be set to “enable” for the clock to be active on that pin.

Clocks always start and stop in a glitch free manner, meaning duty cycle requirements are still met.

TABLE 2-1: OE FUNCTIONALITY FOR 100M[6:0] OUTPUTS

Inputs	OE# Hardware Pins, Control Register Bits, and SBI			
PWRGD/ PWRDN#	OE# Pin	SBI	SMBus	100M[6:0] 100M[6:0]#
0	X	X	X	Disabled
1	0	1	1	Running
	1	X	X	Disabled
	X	0	X	Disabled
	X	X	0	Disabled

TABLE 2-2: OE FUNCTIONALITY FOR 25M[2:0] AND MXCK[8:0] OUTPUTS

Inputs	PFT_OUT, OE Control Register Bits, and SBI		
PWRGD/ PWRDN#	SBI	SMBus	PFT_OUT/PFT_OUT# 25M[2:0]/25M[2:0]# MXCK[8:0]/MXCK[8:0]#
0	X	X	Disabled
1	1	1	Running
	0	X	Disabled
	X	0	Disabled

2.7 OE[6:0]# Assertion (Transition from '1' to '0')

All differential outputs that were disabled are to resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 0 to 10 CK (differential output) clock periods.

2.8 OE[6:0]# De-Assertion (Transition from '0' to '1')

The impact of de-asserting OE# is each corresponding output will transition from normal operation to disabled in a glitch free manner. A minimum of four valid clocks will be provided after the de-assertion of OE#. The maximum latency from the de-assertion to disabled outputs is 10 CK clock periods.

2.9 25MPG

The 25MPG pin enables output 25M[2]/25M[2]# while the rest of the chip is still in reset. The pin shall not be asserted before V_{DD} reaches $V_{DD(MIN)}$. Prior to the power supply reaching $V_{DD(MIN)}$, 25MPG must be held low (less than 0.5V)

De-assertion of 25MPG does not gate 25M[2]/25M[2]# outputs if PWRGD is asserted. Essentially PWRGD/PWRDN# and 25MPG are OR-ed and this signal is used as a glitchless Output Enable of 25M[2]/25M[2]# output.

TABLE 2-3: 25MPG PWRGD/PWRDN# FUNCTIONALITY

PWRGD/PWRDN#	25MPG	25M2 OE bit in Byte 2	25M[2]/25M[2]#
0	0	1	Disabled
X	1	1	Running
1	0	1	Running, Note 1
X	X	0	Disabled

Note 1: Refer to next section for details on PWRGD/PWRDN# operation.

2.10 PWRGD/PWRDN#

PWRGD is asserted high and deasserted low. Deassertion of PWRGD (pulling the signal low) is equivalent to indicating a power-down condition. PWRGD (assertion) is used by the ZL30292 to sample initial configurations such as SMB_ADR0_tri, SMB_ADR1_tri, SSC_EN_tri, and MXCK_SEL_100# selections.

After PWRGD has been asserted high for the first time, the pin becomes a PWRDN# (Power Down) pin, which is used to disable (drive low/low) all clocks cleanly and instruct the device to invoke power savings mode. PWRDN# is a completely asynchronous active-low input. When entering power savings mode, PWRDN# should be asserted low prior to shutting off the input clock or power to ensure all clocks shut down in a glitch free manner. When PWRDN# is de-asserted high, all clocks will start and stop without any abnormal behavior and will meet all AC and DC parameters.

The assertion and de-assertion of PWRDN# is asynchronous. Refer to Table 2-1, Table 2-2, and Table 2-3 for details on PWRGD/PWRDN# functionality.

2.11 PWRDN# Assertion

When PWRDN# is sampled low by two consecutive rising edges of CK#, all differential outputs will be disabled on the next CK# high to low transition. It is possible that PWRDN# transition occurs right after the rising edge of 100M clock because PWRDN# transition is asynchronous with 100M clock. In this case it will take up to three clock cycles to disable the outputs.

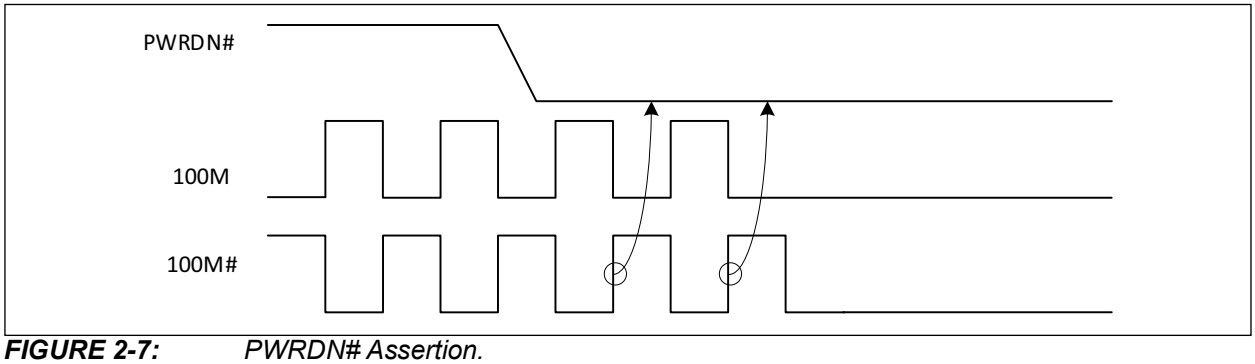


FIGURE 2-7: *PWRDN# Assertion.*

2.12 PWRGD Assertion

PWRGD to the clock buffer should not be asserted before V_{DD} reaches $V_{DD(MIN)}$ = 3.3V – 9%. Prior to $V_{DD(MIN)}$, it is recommended to hold PWRGD low (less than 0.5V).

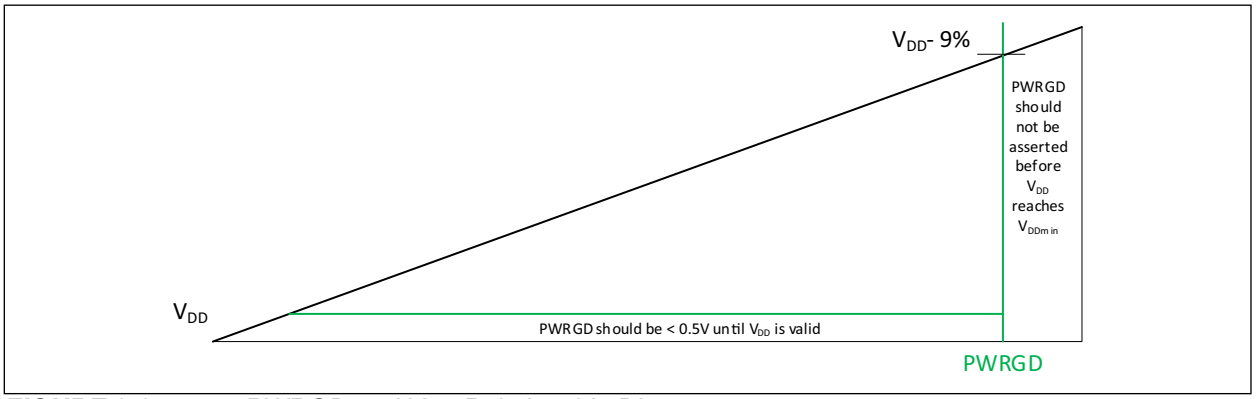


FIGURE 2-8: *PWRGD and V_{DD} Relationship Diagram.*

The power-up latency t_{STABLE} is to be less than 5 ms. This is the time from the assertion of the PWRGD signal to the time that stable clocks are output from the buffer chip. All differential outputs that are stopped in a Low/Low condition resulting from power down must be driven to high/low differential output in less than 300 µs of PWRGD assertion to a voltage greater than 200 mV.

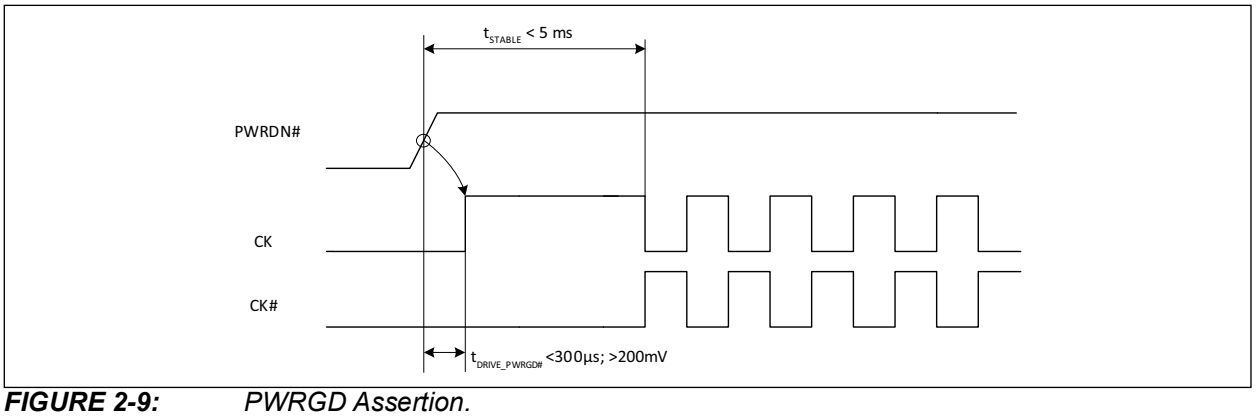


FIGURE 2-9: *PWRGD Assertion.*

2.13 SMB_ADR0_tri, SMB_ADR1_tri – Address Selection

SMB_ADR0_tri and SMB_ADR1_tri are tri-level hardware pins, which program the appropriate address for the ZL30292. The two tri-level input pins can configure the ZL30292 to nine different addresses as indicated in Table 2-4 (refer to Table 3-16 for VIL_tri, VIM_tri, VIH_tri signal level).

TABLE 2-4: SMBUS ADDRESS TABLE

SMBUS_ADR1_tri	SMBUS_ADR0_tri	SMBus Address
L	L	D2
L	M	D4
L	H	D6
M	L	B2
M	M	B4
M	H	B6
H	L	BA
H	M	BC
H	H	BE

2.14 SMBus Byte Read/Write

Reading or writing a register in a SMBus client device in byte mode always involves specifying the register number.

Read. The standard byte read is as shown in Figure 2-10. It is an extension of the byte write. The write start condition is repeated then the client device starts sending data and the server acknowledges it until the last byte is sent. The server terminates the transfer with a NAK then a stop condition. For byte operation, the 2^7th bit of the command byte must be set. For block operations, the 2^7th bit must be reset. If the bit is not set, the next byte must be the byte transfer count.

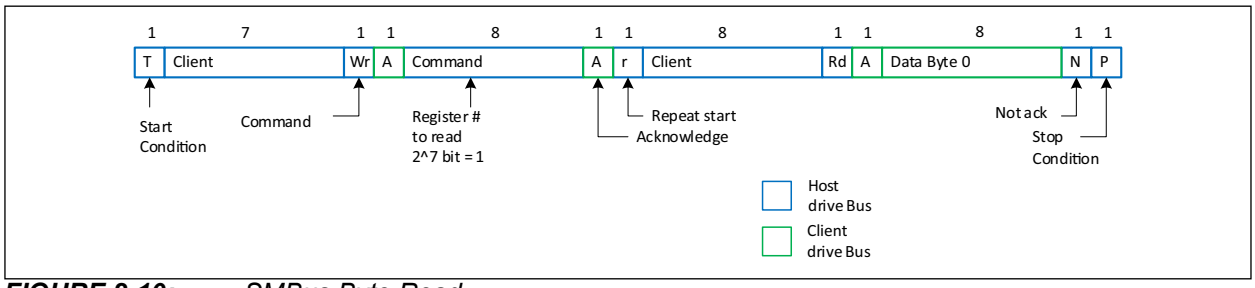


FIGURE 2-10: *SMBus Byte Read.*

Write. Figure 2-11 illustrates a simple typical byte write. For byte operation the 2^7th bit of the command byte must be set.

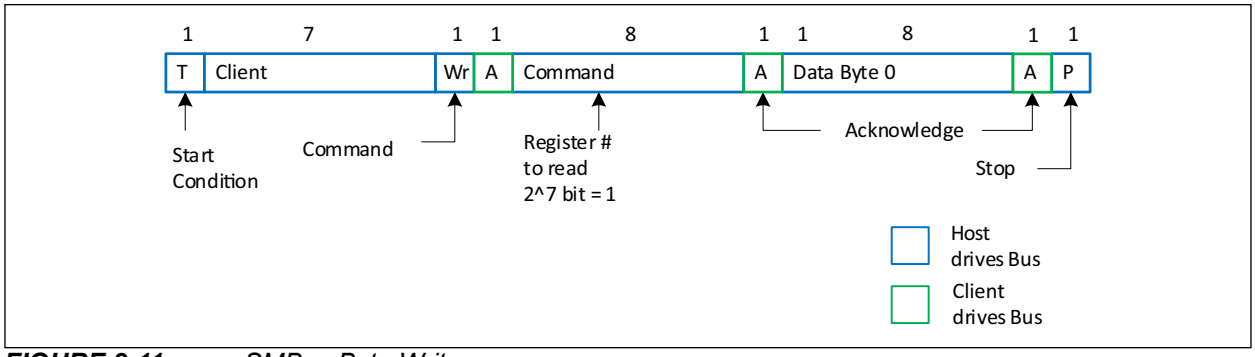


FIGURE 2-11: *SMBus Byte Write.*

2.15 SMBus Block Read/Write

For block operations, the 2^7th bit must be reset. If the bit is not set the next byte must be the byte transfer count. The count can be between 1 and 32. It cannot be zero or exceed 32.

Read. After the client address is sent with the R/W condition bit set, the command byte is sent with the MSB = 0. The client Ack's the register index in the command byte. The server sends a repeat start function. After the client Ack's this the client sends the number of bytes. The server Ack's each byte except the last and sends a stop function.

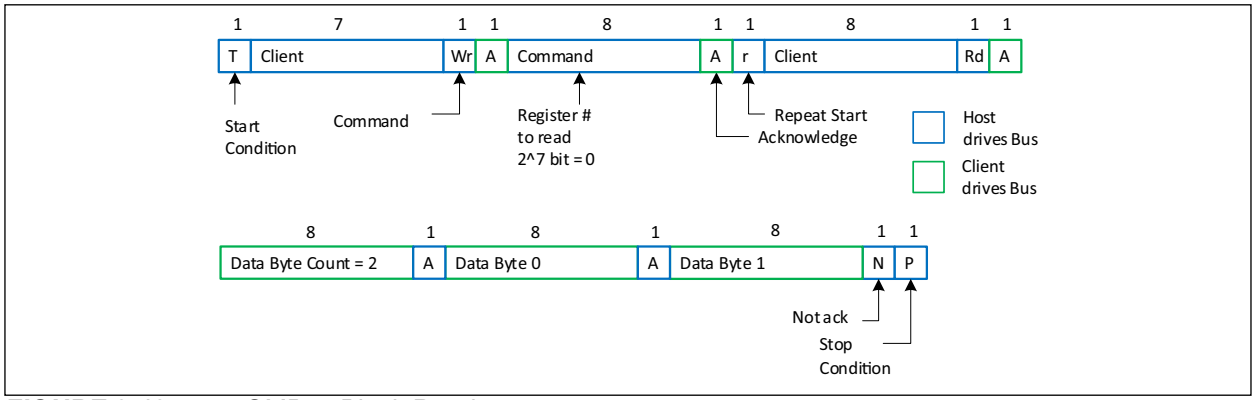


FIGURE 2-12: *SMBus Block Read.*

Write. After the client address is sent with the R/W condition bit not set, the command byte is sent with the MSB = 0. The lower seven bits indicate what register to start the transfer at. If the command byte is 00h, the client device will be compatible with existing block mode client devices. The next byte of a write must be the count of bytes that the server will transfer to the client device. The byte count must be greater than zero and less than 33. Following this byte are the data bytes to be transferred to the client device. The client device always acknowledges each byte received. The transfer is terminated after the client sends the Ack and the server sends a stop function.

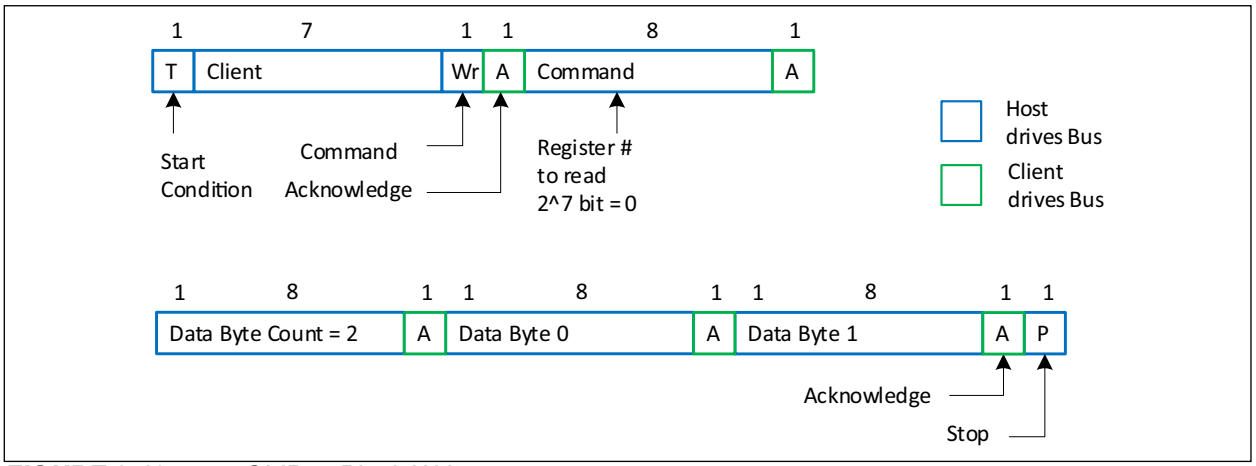


FIGURE 2-13: *SMBus Block Write.*

2.16 Programming via Side-Band Interface

The third output enable/disable method is a simple serial interface referred to as the Side-Band Interface (SBI). In the DB2000QL, this is a 3-wire interface consisting of SBI_DATA (input), SBI_CLK, and SHFT_LD# pins. The device adds an additional pin: SBI_OUT. This output is the last stage of the internal 20-bit shift register. The SBI_DATA pin is renamed to SBI_IN. When the SHFT_LD# pin is high, the rising edge of SBI_CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# loads the shift register contents to the output control register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable of outputs, regardless of the method used.

Because the CK440Q has dedicated pins for the SBI, both SBI and the traditional SMBus methods are active at the same time. There are SMBus registers for masking off the disable function of the SBI interface. When set to a one, the mask register forces the SBI for its respective output to indicate ‘enabled’. This prevents accidentally disabling critical outputs when using the SBI. Remember that the traditional SMBus enable bits and the OE# pins may still disable an output.

If the application does not use the SBI, the SBI input pins may be tied ‘Low’. Figure 2-14 provides a high level functional description of the SBI.

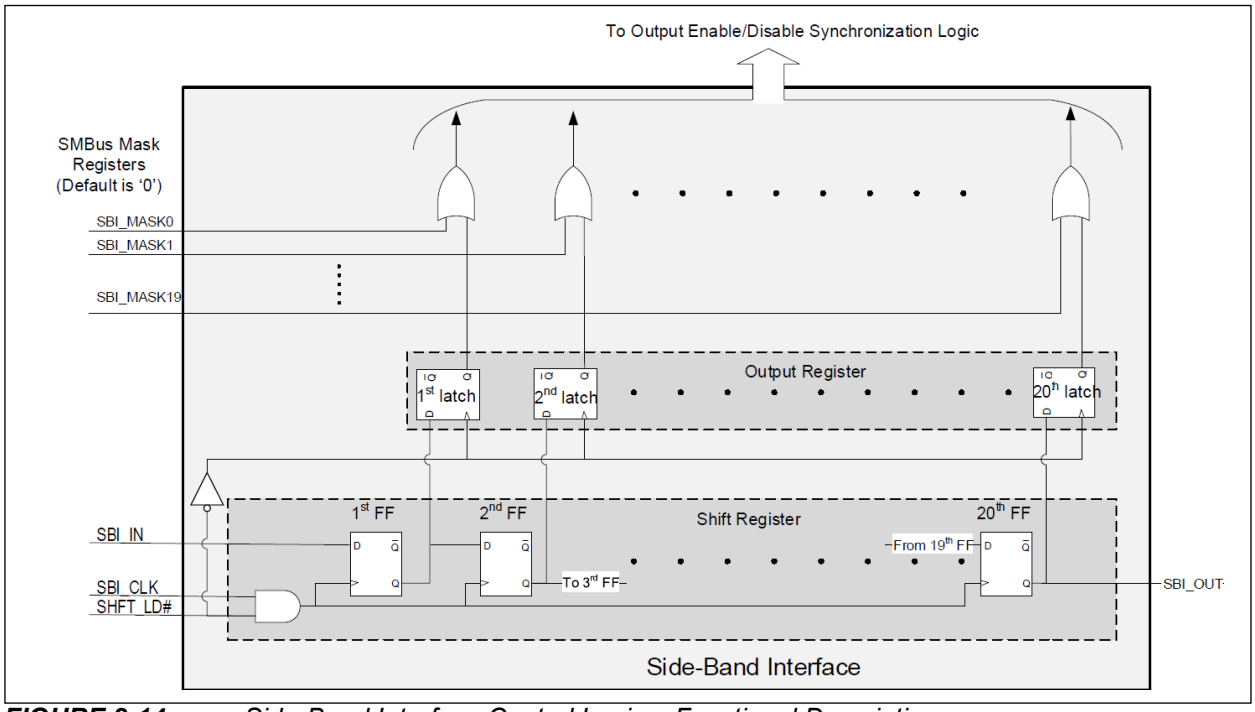


FIGURE 2-14: *Side-Band Interface Control Logic – Functional Description.*

2.17 Output Enable/Disable Priority

The outputs are enabled by an 'AND' function of all methods of enabling the output. Figure 2-15 illustrates this. There are three enable/disable paths: OE# pin (if present), a SMBus OE bit, and the Side-Band Interface. All three must indicate 'enable' for the output to be enabled. Conversely, any single enable/disable path can disable an output if it indicates 'disable'.

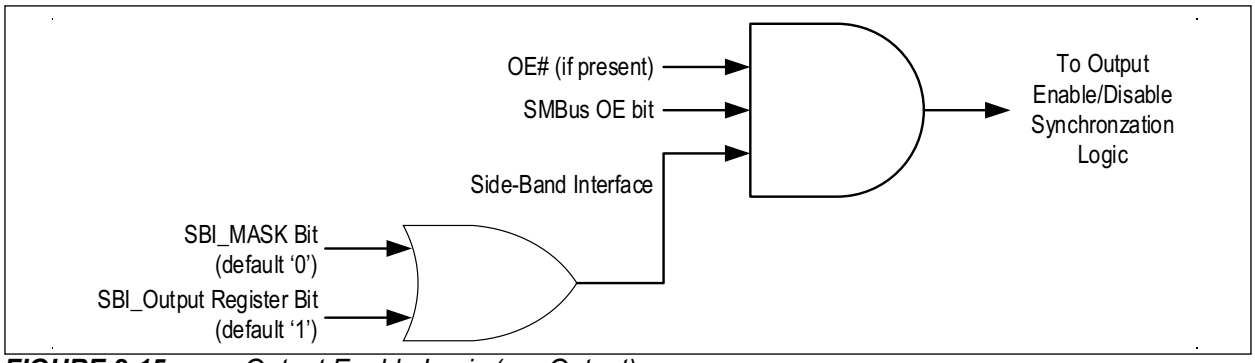


FIGURE 2-15: *Output Enable Logic (per Output).*

A closer study of Figure 2-15 shows the following must be true to enable an output:

- OE# pin (if present) must be 'low'
- SMBus OE bit must be 'high'
- Side-Band Interface must be 'high'

Additionally, one can see that the Side-Band Interface indicates a 'high' if the SBI_Mask_Bit OR the SBI_Output Register Bit are 'high'. This means that the SBI_MASK_Bit can prevent the SBI interface from disabling an output. Note that the SBI_MASK_Bits are SMBus registers.

The shift order follows the order of the SMBus enable bits in Byte[2:0] as shown in Figure 2-16. The first bit shifted in would be the output enable for the PFT_OUT, which is in Byte 2 bit 3. The last bit shifted in would be the output enable for 100M0, which is in Byte 0, bit 0.

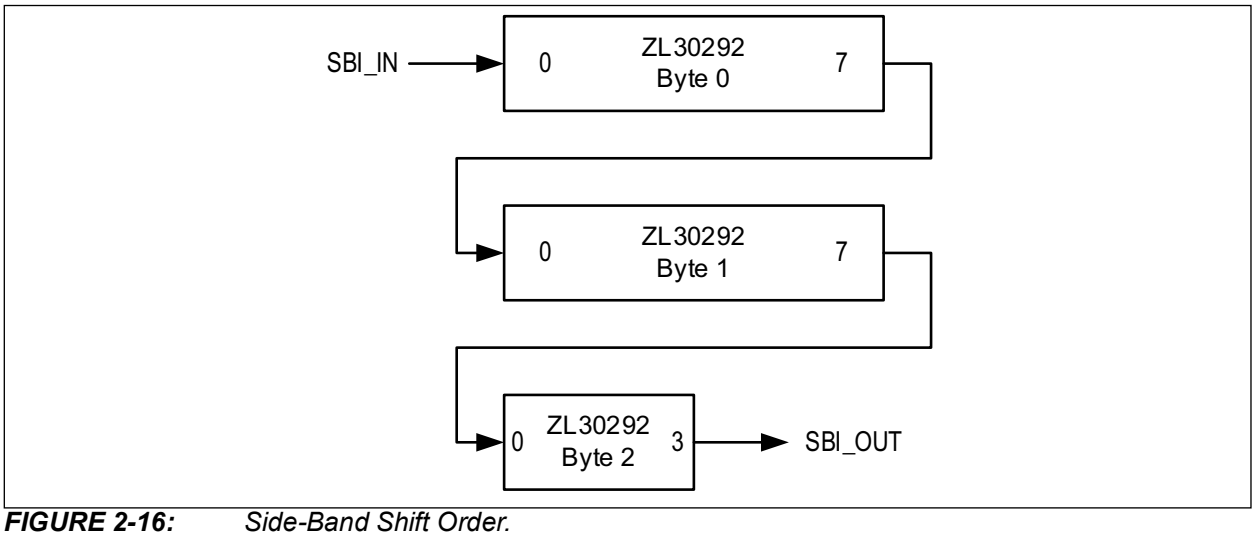


FIGURE 2-16: *Side-Band Shift Order.*

The SMBus registers for the SBI Output and SBI_Mask follow the same bit order. Note that the SBI Output register contains the value latched from the shift register. Software must apply the SBI Mask bits to this value to get the output of the Side-Band Interface OR gate in Figure 2-15.

Figure 2-17 illustrates a star topology connection for the ZL30292 SBI interface. The star topology allows independent configuration of each device. For ZL30292, this means shifting 20 bits at a time. A disadvantage is that a separate SHFT_LD# pin is required for each device.

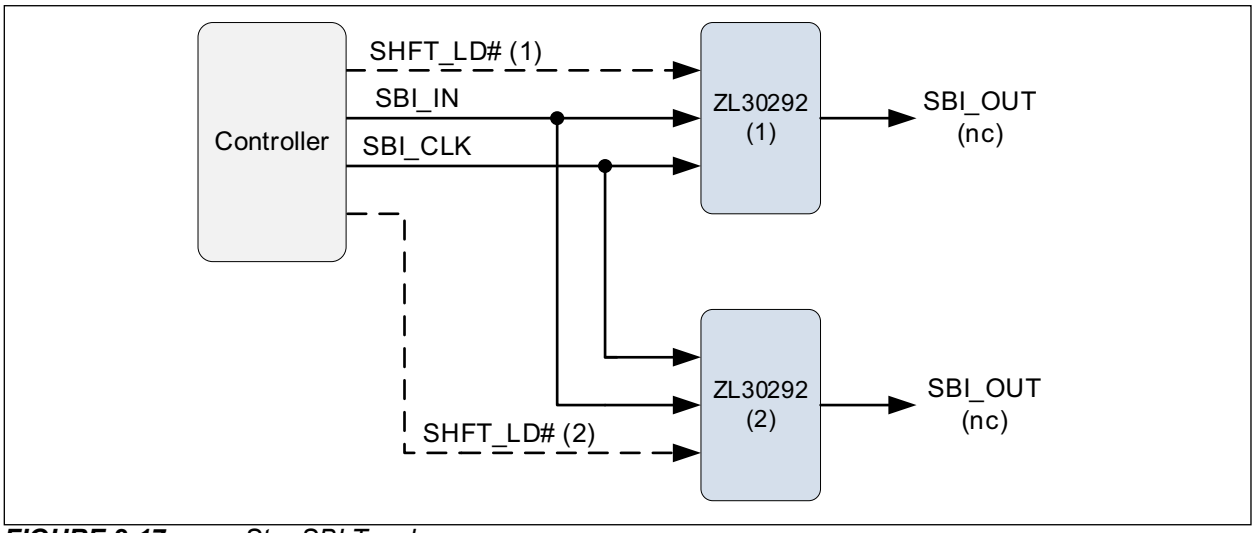


FIGURE 2-17: *Star SBI Topology.*

The daisy chain topology allows configuration of any number of devices with only three signals from the SBI controller. It utilizes the SBI_OUT pin of one device to drive the SBI_IN pin of the next device in the daisy chain. Users must take care to shift the proper number of bits in this configuration. For the example shown in Figure 2-18, the SBI bit stream consists of 40 bits.

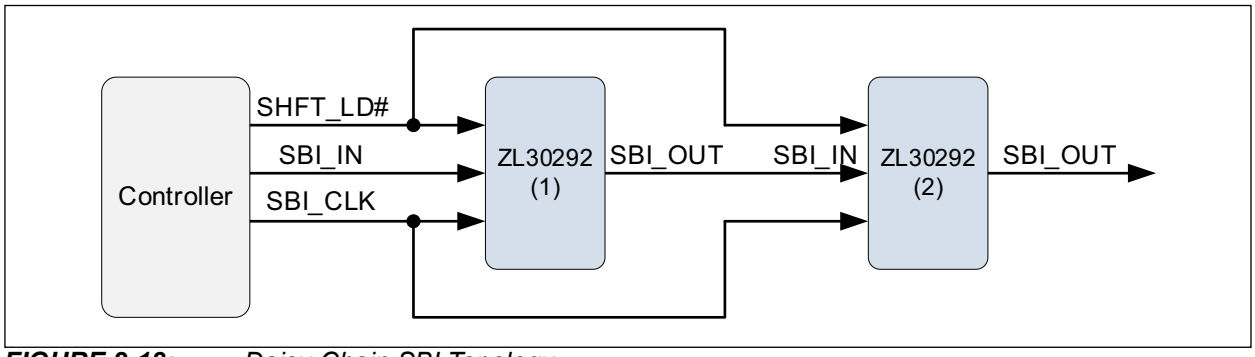


FIGURE 2-18: *Daisy-Chain SBI Topology.*

2.18 Side-Band Interface Functionality and Detailed Timing

Figure 2-19 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the SBI_CLK input. Next, the rising edge of SBI_CLK clocks SBI_IN data into the shift register. After the 20th clock, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# latches the shift register contents to the output control register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

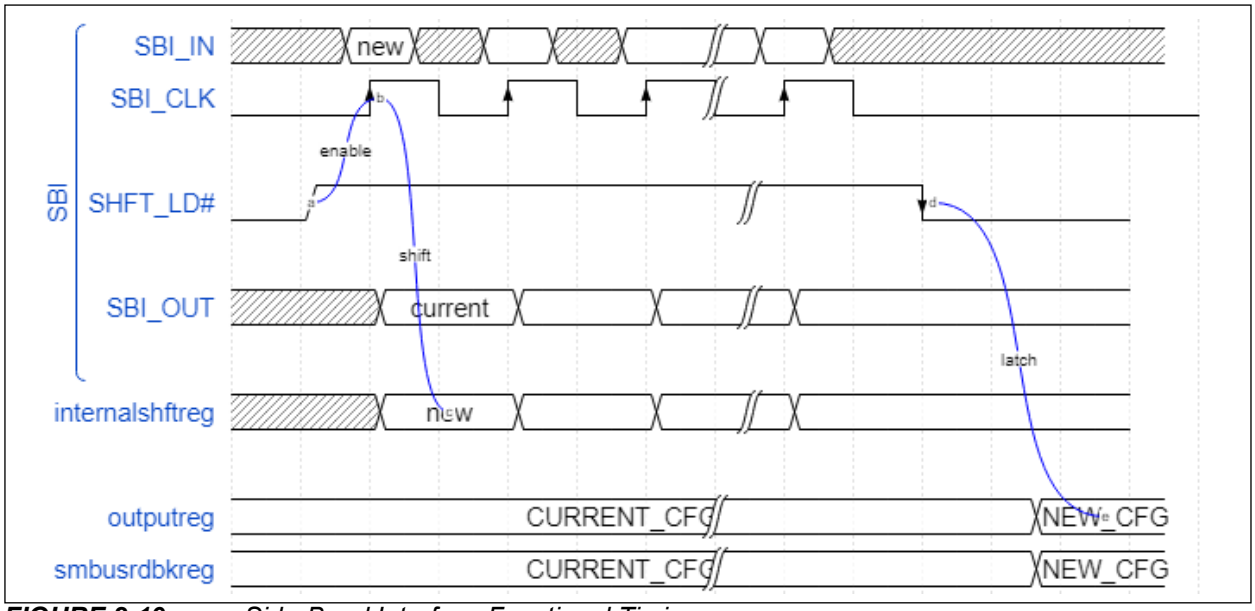


FIGURE 2-19: *Side-Band Interface Functional Timing.*

The SBI interface supports clock rates up to 25 MHz. The device allows two SBI connection topologies: star and daisy chain. In a star topology, multiple devices may share SBI_CLK and SBI_IN pins. In this topology, each device has a dedicated SHFT_LD# pin. In a daisy-chain topology, the SBI_OUT of one device connects to the SBI_IN device of a downstream device. When using the daisy chain topology, the user must shift a complete set of bits for the combined devices. Two daisy-chained devices require shifting of 40 bits. When the SHFT_LD# pin is low, the SBI interface ignores any activity on the SBI_CLK and SBI_IN pins.

2.19 Platform Time (PFT) Phase/Frequency Tracking

PFT_IN/OUT allows different devices to frequency lock the 25 MHz clocks to a single time base. The system implementation is shown in Figure 2-20.

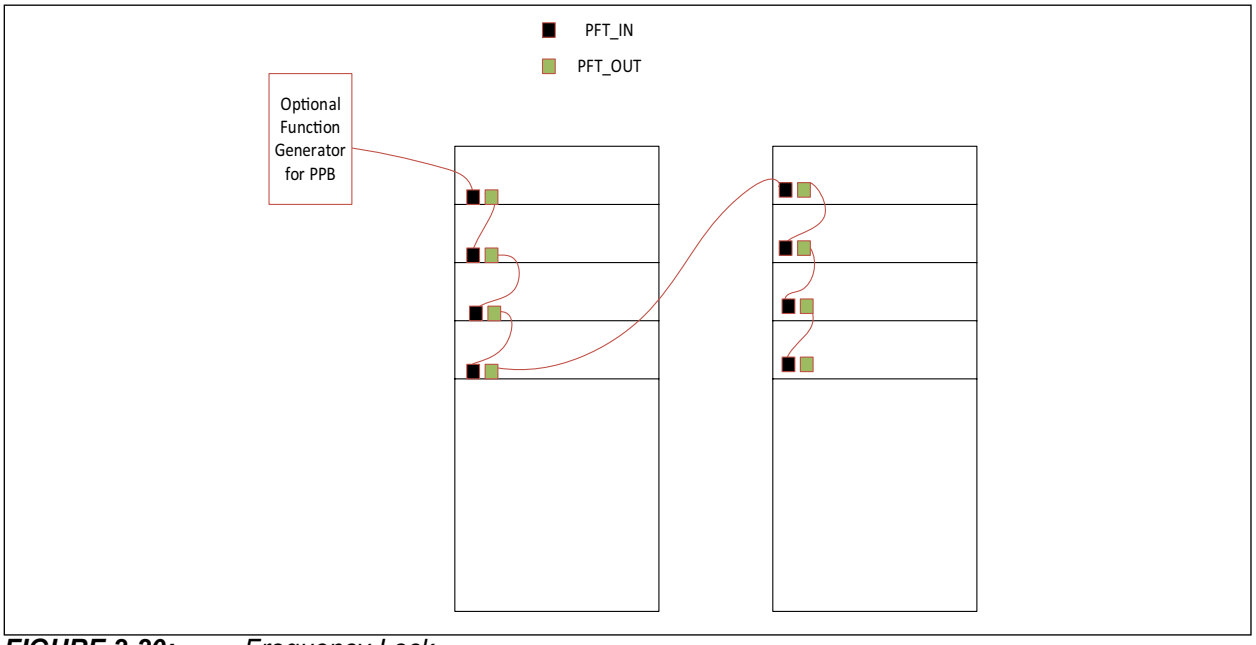


FIGURE 2-20: *Frequency Lock.*

The local 25 MHz frequency locks to the PFT_IN clock if it is present. If PFT_IN is not present, the local 25 MHz frequency is sourced from the local crystal.

The output signal PFT_LOST# asserts if the PFT_IN clock is not present. If the PFT_IN clock is lost during operation, PFT_OUT and all other clocks are continued without timing glitches. If the PFT_IN clock is applied during operation, the frequency lock occurs according to the PFT filter to ensure a glitchless output of PFT_OUT.

PFT_IN does not replace the need for the local crystal oscillator and may not be used as the oscillator source.

The signed PPM difference between the supplied PFT_IN clock and the local crystal oscillator can be read in the SMBUS registers. The PPM difference is defined as the number of 1 ns steps that were required in the last 215 clocks, signed for direction.

The platform time tracking must be able to track ±125 ppm difference between the local clock and the PFT_IN clock. The phase relationship between input PFT_IN and PFT_OUT is within (±4 ns). The PTO timing parameters are given in Table 2-5.

TABLE 2-5: PLATFORM TIME TIMING PARAMETERS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
PTO_OUT Period	t_{PERIOD}	38	40	42	ns	Clock period
PPM Tracking	PFT_PPM	±125	—	—	ppm	—

3.0 REGISTER MAP

Note: When differential outputs are disabled they drive low/low. For example, if 100M0 output is disabled, it will drive low on both 100M0 and 100M0# pins.

TABLE 3-1: BYTE 0: OUTPUT ENABLE CONTROL REGISTER 0

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable 100M0	Disabled	Enabled	RW	1	100M0
1	Output Enable 100M1	Disabled	Enabled	RW	1	100M1
2	Output Enable 100M2	Disabled	Enabled	RW	1	100M2
3	Output Enable 100M3	Disabled	Enabled	RW	1	100M3
4	Output Enable 100M4	Disabled	Enabled	RW	1	100M4
5	Output Enable 100M5	Disabled	Enabled	RW	1	100M5
6	Output Enable 100M6	Disabled	Enabled	RW	1	100M6
7	Output Enable MXCK8	Disabled	Enabled	RW	1	MXCK8

TABLE 3-2: BYTE 1: OUTPUT ENABLE CONTROL REGISTER 1

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable MXCK0	Disabled	Enabled	RW	1	MXCK0
1	Output Enable MXCK1	Disabled	Enabled	RW	1	MXCK1
2	Output Enable MXCK2	Disabled	Enabled	RW	1	MXCK2
3	Output Enable MXCK3	Disabled	Enabled	RW	1	MXCK3
4	Output Enable MXCK4	Disabled	Enabled	RW	1	MXCK4
5	Output Enable MXCK5	Disabled	Enabled	RW	1	MXCK5
6	Output Enable MXCK6	Disabled	Enabled	RW	1	MXCK6
7	Output Enable MXCK7	Disabled	Enabled	RW	1	MXCK7

TABLE 3-3: BYTE 2: OUTPUT ENABLE CONTROL REGISTER 2

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable 25M0	Disabled	Enabled	RW	1	25M0
1	Output Enable 25M1	Disabled	Enabled	RW	1	25M1
2	Output Enable 25M2	Disabled	Enabled	RW	1	25M2
3	Output Enable PFT_OUT	Disabled	Enabled	RW	1	PFT_OUT
4	Reserved	—	—	—	0	Reserved
5	Realtime Readback of MXCK_SEL pin	100 MHz Selected	25 MHz Selected	R	0	MXCK[8:0]
6	MXCK_SEL Control (Note 1)	Pin Control	Register Control	RW	0	MXCK[8:0]
7	MXCK_SEL	100 MHz	25 MHz	RW	0	MXCK[8:0]

Note 1: If MXCK_SEL Control (bit 6) is set to ‘0’ (default), MXCK[8:0] outputs are controlled with MXCK_SEL_100 pin. If MXCK_SEL Control (bit 6) is set to ‘1’ then MXCK[8:0] outputs are controlled with MXCK_SEL bit (bit 7). MXCK_SEL switchover is asynchronous. If the user needs glitch free transition, the outputs shall be disabled first and enabled only after the MXCK_SEL is changed.

TABLE 3-4: BYTE 3: PFT CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Defualt	Output(s) Affected
0	Reserved	—	—	—	0	Reserved
1	Reserved	—	—	—	0	Reserved
2	Reserved	—	—	—	0	Reserved
3	Reserved	—	—	—	0	Reserved
4	Reserved	—	—	—	0	Reserved
5	Clear Delta Frequency Registers (Byte 4 and 5)	—	All bits reset to 0	RW	0	Reserved
6	Stop Delta Frequency Update (Byte 4 and 5)	Disabled	Enabled	RW	0	Reserved
7	Realtime Readback of PFT_LOST#	PFT_LOST# low	PFT_LOST# high	R	Realtime	PFT_OUT

Note 1: Prior to reading the delta frequency between PFT_IN and the local 25 MHz XO (Bytes 4 and 5), the user should set bit 6 to prevent the case where one of the PFT Frequency Delta Registers is read before and the other after the internal update. This bit should be cleared after the read has been completed.

TABLE 3-5: BYTE 4: PFT FREQUENCY DELTA REGISTER 0 (LEAST SIGNIFICANT BYTE)

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	PFT – 25 MHz XO bit 0	—	—	R	Realtime	—
1	PFT – 25 MHz XO bit 1	—	—	R	Realtime	—
2	PFT – 25 MHz XO bit 2	—	—	R	Realtime	—
3	PFT – 25 MHz XO bit 3	—	—	R	Realtime	—
4	PFT – 25 MHz XO bit 4 (Note 1)	—	—	R	Realtime	—
5	PFT – 25 MHz XO bit 5	—	—	R	Realtime	—
6	PFT – 25 MHz XO bit 6	—	—	R	Realtime	—
7	PFT – 25 MHz XO bit 7	—	—	R	Realtime	—

Note 1: Byte 4 and 5 contain frequency difference between the PFT clock and the local 25 MHz reference in two's complement format with resolution (step size) of 1 ns * (25 MHz/2^{15}) ≈ 1 ns/1.31 ms = 0.763 ppm. Byte 4 contains the least significant byte.

TABLE 3-6: BYTE 5: PFT FREQUENCY DELTA REGISTER 1 (MOST SIGNIFICANT BYTE)

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	PFT – 25 MHz XO bit 8	—	—	R	Realtime	—
1	PFT – 25 MHz XO bit 9	—	—	R	Realtime	—
2	PFT – 25 MHz XO bit 10	—	—	R	Realtime	—
3	PFT – 25 MHz XO bit 11	—	—	R	Realtime	—
4	PFT – 25 MHz XO bit 12 (Note 1)	—	—	R	Realtime	—
5	PFT – 25 MHz XO bit 13	—	—	R	Realtime	—
6	PFT – 25 MHz XO bit 14	—	—	R	Realtime	—
7	PFT – 25 MHz XO bit 15	—	—	R	Realtime	—

Note 1: Byte 4 and 5 contain frequency difference between the PFT clock and the local 25 MHz reference in two's complement format with resolution (step size) of 1 ns * (25 MHz/2^{15}) ≈ 1 ns/1.31 ms = 0.763 ppm. Byte 5 contains the most significant byte.

TABLE 3-7: BYTE 6: SSC PLL CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	SSC Select	**bit1 bit0: SSC State** 00: SSC Off 01: SSC = –0.3% 10: Reserved 11: SSC = –0.5%		RW	Latch SSC Pin on Power-Up	100M[6:0] and MXCK[8:0] if MXCK_SEL is low
1				RW	Latch SSC Pin on Power-Up	100M[6:0] and MXCK[8:0] if MXCK_SEL is low
2	SSC Pin Control	Enabled	Disabled	RW	0	100M[6:0] and MXCK[8:0] if MXCK_SEL is low
3	SSC PLL Input Source	XTAL	Filter PLL (Note 1)	RW	0	100M[6:0] and MXCK[8:0] if MXCK_SEL is low
4	Readback of SSC_ENABLE Pin	**bit1 bit0: SSC State** 00: SSC Off 01: SSC = –0.3% 10: Reserved 11: SSC = –0.5%		R	Realtime	100M[6:0] and MXCK[8:0] if MXCK_SEL is low
5				R	Realtime	100M[6:0] and MXCK[8:0] if MXCK_SEL is low
6	Reserved	—	—	—	0	Reserved
7	Reserved	—	—	—	0	Reserved

Note 1: When “SSC PLL Input Source” selects the “Filter PLL” option, there’s no guarantee the outputs will be synchronized.

TABLE 3-8: BYTE 7: OE# REALTIME READBACK CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Realtime Readback of OE_0# pin	OE_0# Low	OE_0# High	R	Realtime	100M0
1	Realtime Readback of OE_1# pin	OE_1# Low	OE_1# High	R	Realtime	100M1
2	Realtime Readback of OE_2# pin	OE_2# Low	OE_2# High	R	Realtime	100M2
3	Realtime Readback of OE_3# pin	OE_3# Low	OE_3# High	R	Realtime	100M3
4	Realtime Readback of OE_4# pin	OE_4# Low	OE_4# High	R	Realtime	100M4
5	Realtime Readback of OE_5# pin	OE_5# Low	OE_5# High	R	Realtime	100M5
6	Realtime Readback of OE_6# pin	OE_6# Low	OE_6# High	R	Realtime	100M6
7	Reserved	—	—	R	0	—

TABLE 3-9: BYTE 8: VENDOR/REVISION IDENTIFICATION CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Vendor ID Bit 0	—	—	R	1	—
1	Vendor ID Bit 1	—	—	R	1	—
2	Vendor ID Bit 2	—	—	R	0	—
3	Vendor ID Bit 3	—	—	R	0	—
4	Revision Code Bit 0	—	—	R	1	—
5	Revision Code Bit 1	—	—	R	0	—
6	Revision Code Bit 2	—	—	R	0	—
7	Revision Code Bit 3	—	—	R	0	—

TABLE 3-10: BYTE 9: DEVICE ID CONTROL REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Device ID 0	—	—	R	1	—
1	Device ID 1	—	—	R	1	—
2	Device ID 2	—	—	R	0	—
3	Device ID 3	—	—	R	1	—
4	Device ID 4	—	—	R	1	—
5	Device ID 5	—	—	R	0	—
6	Device ID 6	—	—	R	1	—
7	Device ID 7 (MSB)	—	—	R	0	—

TABLE 3-11: BYTE 10: BYTE COUNT REGISTER

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
1	BC1 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
2	BC2 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
3	BC2 - Writing to this register configures how many bytes will be read back	—	—	RW	1	—
4	BC3 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
5	BC4 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
6	Reserved	—	—	—	0	—
7	Reserved	—	—	—	0	—

TABLE 3-12: BYTE 11: SIDE-BAND INTERFACE MASK REGISTER 0

Bit	Description	If Bit = 0 (Note 1)	If Bit = 1 (Note 1)	Type	Default	Output(s) Affected
0	SBI Mask 100M0	Off	On	RW	0	100M0
1	SBI Mask 100M1	Off	On	RW	0	100M1
2	SBI Mask 100M2	Off	On	RW	0	100M2
3	SBI Mask 100M3	Off	On	RW	0	100M3
4	SBI Mask 100M4	Off	On	RW	0	100M4
5	SBI Mask 100M5	Off	On	RW	0	100M5
6	SBI Mask 100M6	Off	On	RW	0	100M6
7	SBI Mask MXCK8	Off	On	RW	0	MXCK8

Note 1: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit, or OE# pin (present only for 100M outputs).

TABLE 3-13: BYTE 12: SIDE-BAND INTERFACE MASK REGISTER 1

Bit	Description	If Bit = 0 (Note 1)	If Bit = 1 (Note 1)	Type	Default	Output(s) Affected
0	SBI Mask MXCK0	Off	On	RW	0	MXCK0
1	SBI Mask MXCK1	Off	On	RW	0	MXCK1
2	SBI Mask MXCK2	Off	On	RW	0	MXCK2
3	SBI Mask MXCK3	Off	On	RW	0	MXCK3
4	SBI Mask MXCK4	Off	On	RW	0	MXCK4
5	SBI Mask MXCK5	Off	On	RW	0	MXCK5
6	SBI Mask MXCK6	Off	On	RW	0	MXCK6
7	SBI Mask MXCK7	Off	On	RW	0	MXCK7

Note 1: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit.

TABLE 3-14: BYTE 13: SIDE-BAND INTERFACE MASK REGISTER 2

Bit	Description	If Bit = 0 (Note 1)	If Bit = 1 (Note 1)	Type	Default	Output(s) Affected
0	SBI Mask 25M0	Off	On	RW	0	25M0
1	SBI Mask 25M1	Off	On	RW	0	25M1
2	SBI Mask 25M2	Off	On	RW	0	25M2
3	SBI Mask PFT_OUT	Off	On	RW	0	PFT_OUT
4	Reserved	—	—	—	0	—
5	Reserved	—	—	—	0	—
6	Reserved	—	—	—	0	—
7	Reserved	—	—	—	0	—

Note 1: If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit.

TABLE 3-15: BYTE 14: SIDE-BAND INTERFACE READBACK REGISTER 0

Bit	Description	If Bit = 0 (Note 1)	If Bit = 1 (Note 1)	Type	Default	Output(s) Affected
0	SBI Readback 100M0	Disabled	Enabled	R	1	100M0
1	SBI Readback 100M1	Disabled	Enabled	R	1	100M1
2	SBI Readback 100M2	Disabled	Enabled	R	1	100M2
3	SBI Readback 100M3	Disabled	Enabled	R	1	100M3
4	SBI Readback 100M4	Disabled	Enabled	R	1	100M4
5	SBI Readback 100M5	Disabled	Enabled	R	1	100M5
6	SBI Readback 100M6	Disabled	Enabled	R	1	100M6
7	SBI Readback MXCK8	Disabled	Enabled	R	1	MXCK8

Note 1: If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high and OE# pin (present only for 100M outputs) is pulled low.

TABLE 3-16: BYTE 15: SIDE-BAND INTERFACE READBACK REGISTER 1

Bit	Description	If Bit = 0 (Note 1)	If Bit = 1 (Note 1)	Type	Default	Output(s) Affected
0	SBI Readback MXCK0	Disabled	Enabled	R	1	MXCK0
1	SBI Readback MXCK1	Disabled	Enabled	R	1	MXCK1
2	SBI Readback MXCK2	Disabled	Enabled	R	1	MXCK2
3	SBI Readback MXCK3	Disabled	Enabled	R	1	MXCK3
4	SBI Readback MXCK4	Disabled	Enabled	R	1	MXCK4
5	SBI Readback MXCK5	Disabled	Enabled	R	1	MXCK5
6	SBI Readback MXCK6	Disabled	Enabled	R	1	MXCK6
7	SBI Readback MXCK7	Disabled	Enabled	R	1	MXCK7

Note 1: If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled resistors unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high.

TABLE 3-17: BYTE 16: SIDE-BAND INTERFACE READBACK REGISTER 2

Bit	Description	If Bit = 0 (Note 1)	If Bit = 1 (Note 1)	Type	Default	Output(s) Affected
0	SBI Readback 25M0	Disabled	Enabled	R	1	25M0
1	SBI Readback 25M1	Disabled	Enabled	R	1	25M1
2	SBI Readback 25M2	Disabled	Enabled	R	1	25M2
3	SBI Readback PFT_OUT	Disabled	Enabled	R	1	PFT_OUT
4	Reserved	Disabled	Enabled	R	0	—
5	Reserved	Disabled	Enabled	R	0	—
6	Reserved	Disabled	Enabled	R	0	—
7	Reserved	Disabled	Enabled	R	0	—

Note 1: If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high.

4.0 ELECTRICAL CHARACTERISTICS

4.1 AC and DC Electrical Characteristics

TABLE 4-1: ABSOLUTE MAXIMUM RATINGS

Note 1, Note 2, Note 3

Parameter	Symbol	Min.	Max.	Units
3.3V Core Supply Voltage	V_{DD}	—	+3.9	V
3.3V I/O Supply Voltage	V_{DD}	—	+3.9	V
3.3V Input High Voltage (Note 4)	V_{IH}	—	+4.6	V
3.3V Input Low Voltage	V_{IL}	–0.5	—	V
Storage Temperature	T_S	–65	+150	°C
Input ESD Protection (Note 5)	V_{DD-IN}	2000	—	V

Note 1: Exceeding these values may cause permanent damage.

2: Functional operation under these conditions is not implied.

3: Voltages are with respect to ground (GND) unless otherwise stated.

4: Maximum V_{IH} is not to exceed maximum V_{DD}.

5: Human body model.

4.2 DC Electrical Specifications

TABLE 4-2: DC OPERATING CHARACTERISTICS

Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units
3.3V Core Supply Voltage	V_{DD}	2.97	3.3	3.63	V
3.3V I/O Supply Voltage	V_{DD}	2.97	3.3	3.63	V
3.3V Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V
3.3V Input Low Voltage	V_{IL}	V_{SS} – 0.3	—	0.8	V
Input Leakage Current	I_{IL}	–5	—	+5	µA
Input Low Voltage, 3-level CMOS Input	V_{IL3}	V_{SS} – 0.3	—	0.9	V
Input Midrange Voltage, 3-level CMOS Input (Note 3)	V_{IM3}	1.3	—	1.8	V
Input High Voltage, 3-level CMOS Input	V_{IH3}	2.4	—	V_{DD}	V
Input Capacitance (Note 2)	C_{IN}	—	—	4.5	pF
Input Capacitance of XIN Pin	C_{INX}	—	—	12	pF
Output Capacitance (Note 2)	C_{OUT}	—	—	4.5	pF
Output Capacitance of PFT_LOST# and XOUT pins	C_{OUTS}	—	—	12	pF
Ambient Temperature	T_A	–40	—	+85	°C

Note 1: Voltages are with respect to ground (GND) unless otherwise stated.

2: For parasitic simulation, use IBIS model.

3: V_{IM3} max. is 1.8V for V_{DD} – 5%. For V_{DD} – 10%, this value is 1.65V.

TABLE 4-3: DIFFERENTIAL DC OUTPUT CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Rising Edge Rate	—	1	2.5	4	V/ns	Note 2, Note 3
Falling Edge Rate	—	1	2.5	4	V/ns	Note 2, Note 3
Differential Output High Voltage	V_{OH}	0.6	—	0.9	V	Note 2
Differential Output Low Voltage	V_{OL}	–0.9	—	–0.6	V	Note 2
Absolute Crossing Voltage	V_{CROSS}	0.25	—	0.55	V	Note 1, Note 4, Note 5
Variation of V_{CROSS} over All Rising Clock Edges	V_{CROSS_DELTA}	—	—	0.14	V	Note 1, Note 4, Note 8
Ringback Voltage Margin	V_{RB}	–0.1	—	0.1	V	Note 2, Note 10
Time Before V_{RB} is Allowed	PCIe_t_{STABLE}	500	—	—	ps	Note 2, Note 10
Absolute Maximum Output Voltage	V_{MAX}	—	—	1.15	V	Note 1, Note 6
Absolute Minimum Output Voltage	V_{MIN}	–0.3	—	—	V	Note 1, Note 7
Output Duty Cycle (when input has 50% duty cycle and V_{IN} ≥ 200 mV)	—	45	50	55	%	Note 2
Rising to Falling Edge Matching	—	—	—	20	%	Note 1, Note 11
Clock Source DC Impedance (OUTx_p)	$Z_{C\text{-}DC\_OUT\_p}$	50 –5%	50	50 +5%	Ω	—
Clock Source DC Impedance (OUTx_n)	$Z_{C\text{-}DC\_OUT\_n}$	50 –5%	50	50 +5%	Ω	—

Note 1: Measurement taken from single-ended waveform.

2: Measurement taken from differential waveform.

3: Measured from –150 mV to +150 mV on the differential waveform (derived from OUTx_p minus OUTx_n) The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 4-7.

4: Measured at crossing point where the instantaneous voltage value of the rising edge of OUTx_p equals the falling edge of OUTx_n. See Figure 4-1.

5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 4-1.

6: Defined as the maximum instantaneous voltage including overshoot. See Figure 4-1.

7: Defined as the minimum instantaneous voltage including undershoot. See Figure 4-1.

8: Defined as the total variation of all crossing voltages of Rising OUTx_p and Falling C OUTx_n. This is the maximum allowed variance in V_{CROSS} for any particular system. See Figure 4-2.

9: System board compliance measurements must use the test load card described in Figure 4-7. Both OUTx_p and OUTx_n should be measured at the load capacitors C_{LOAD}. Single-ended probes must be used for measurements requiring single-ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load C_{LOAD} = 2 pF.

10: t_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after 20 rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 4-6.

11: Matching applies to rising edge rate for OUTx_p and falling edge rate for OUTx_n. It is measured using a ±75 mV window centered on the median cross point where OUTx_p rising meets OUTx_n falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of OUTx_p should be compared to the Fall Edge Rate of OUTx_n the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 4-3.

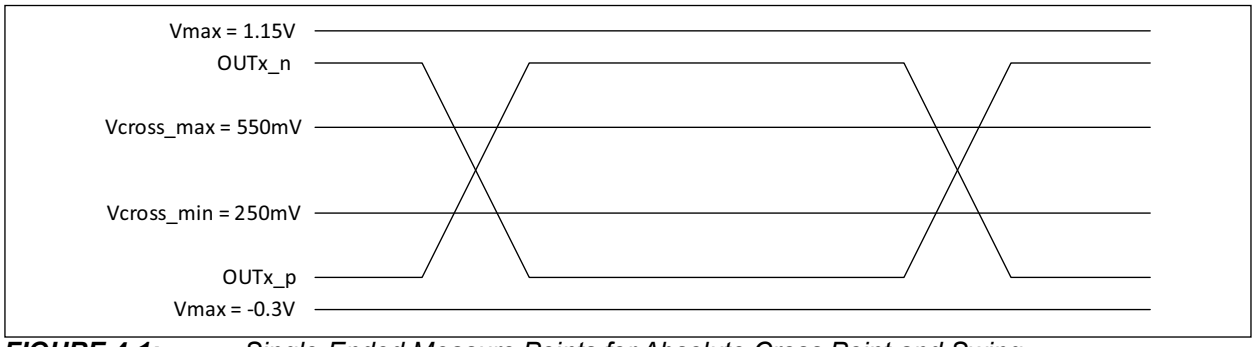


FIGURE 4-1: *Single-Ended Measure Points for Absolute Cross Point and Swing.*

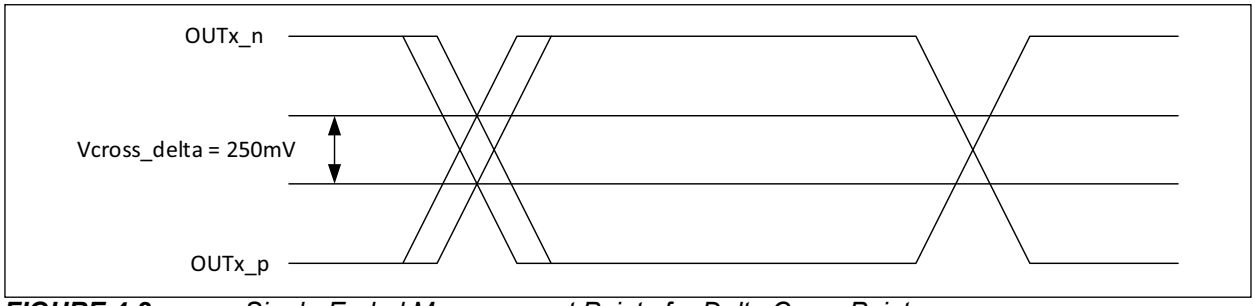


FIGURE 4-2: *Single-Ended Measurement Points for Delta Cross Point.*

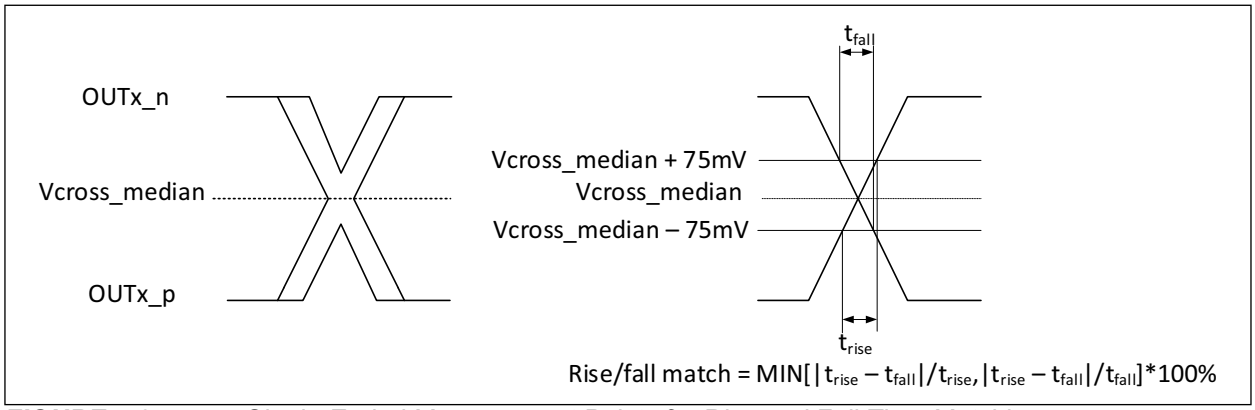


FIGURE 4-3: *Single-Ended Measurement Points for Rise and Fall Time Matching.*

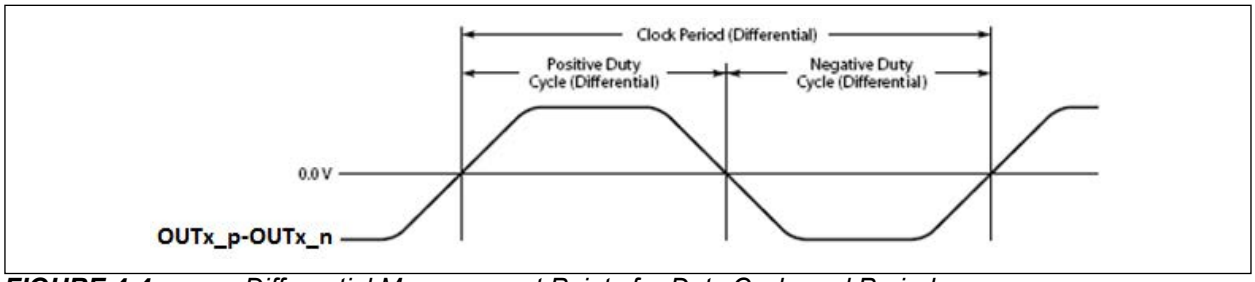


FIGURE 4-4: *Differential Measurement Points for Duty Cycle and Period.*

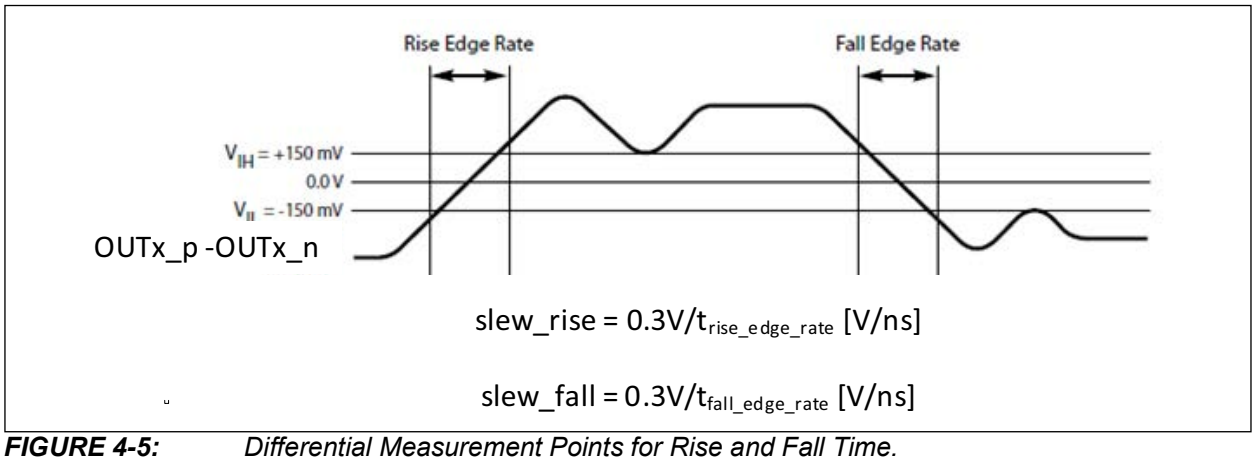


FIGURE 4-5: *Differential Measurement Points for Rise and Fall Time.*

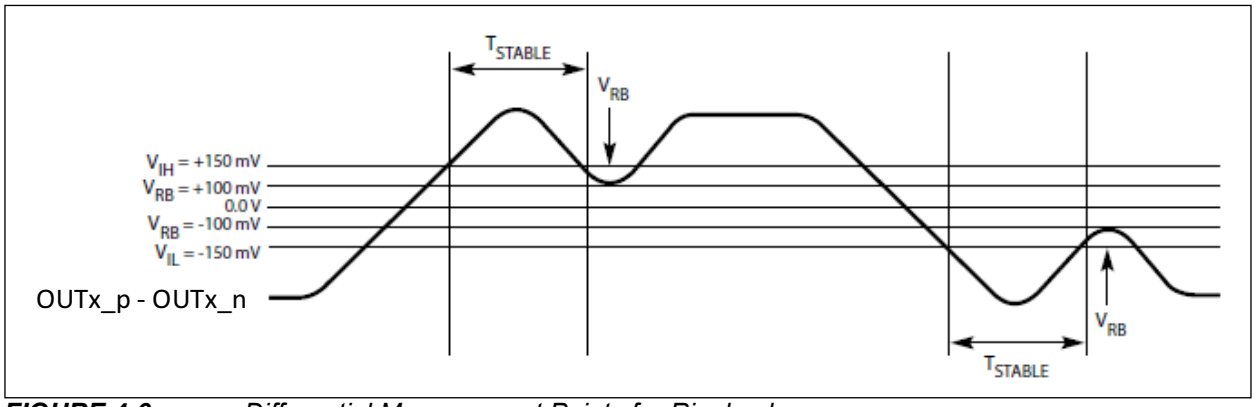


FIGURE 4-6: *Differential Measurement Points for Ringback.*

4.3 AC Electrical Specifications

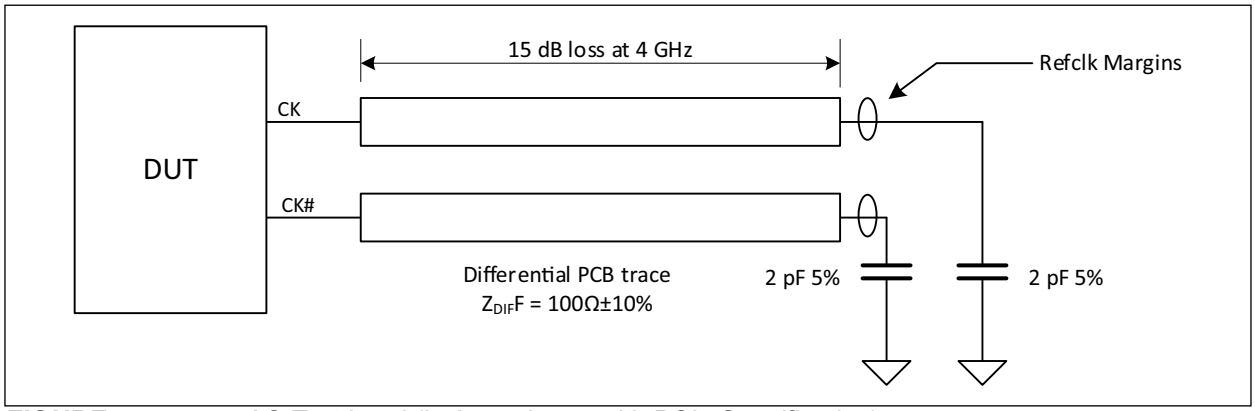


FIGURE 4-7: *AC Test Load (in Accordance with PCIe Specification).*

TABLE 4-4: DIFFERENTIAL OUTPUT CLOCK AC CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Clock Stabilization Time from PWRGD	t_{STABLE}	—	—	5	ms
Slew Rate at V_{CROSS} (Note 1)	Slew_Rate	2	—	4	V/ns
Slew Rate at V_{CROSS} (Note 1)	Rise/Fall Matching	—	—	20%	V
Duty Cycle for All 100 MHz Outputs (Note 1)	$t_{DutyCycle\_100M}$	45	—	55	%
Duty Cycle for All 25 MHz Outputs (Note 2)	$t_{DutyCycle\_25MM}$	47	—	53	%
Duty Cycle for All 25 MHz Outputs (Note 3)		43	—	57	%
Duty Cycle for All 25 MHz Outputs (Note 4)		48	—	52	%

Note 1: Measured into Figure 4-7 AC test load.

2: XTAL as source.

3: XO as source with 45% to 55% duty cycle specified.

4: XO as source with 50% duty cycle and rise/fall time of 1 ns driving 10 pF load or better (PFT_IN clock not active).

TABLE 4-5: DIFFERENTIAL INPUT CLOCK AC CHARACTERISTICS (PFT_IN/PFT_IN#)

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Slew Rate	SR_{IN}	0.7	—	—	V/ns
Input Differential Voltage Swing	V_{SWING}	200	—	2000	mV

TABLE 4-6: CURRENT CONSUMPTION

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Active Mode Supply Current	I_{DDPG_DIS}	—	90	115	mA	All outputs disabled, Note 1
	I_{DDPG_100M}	—	7.3	9		Current consumption per 100 MHz output, Note 1
	I_{DDPG_25M}	—	1.8	3		Current consumption per 25 MHz output, Note 1
Power Down Mode Supply Current	I_{DDPD}	—	—	12	mA	All outputs disabled, Note 1, Note 2, Note 3
	$I_{DDPD25MPG}$	—	35	45		All outputs disabled except 25M[2] (25MPG pulled high), Note 1, Note 2, Note 3

Note 1: V_{DD} = 3.3V + 10%.

2: Device operating in low power mode (Pin PWRGD/PWRDN# = 0).

3: SHFT_LD# is kept low during this measurement.

TABLE 4-7: SKEW AND JITTER

Electrical Characteristics: T_A = –40°C to +85°C, Supply Voltage V_{DD} = 3.3V ±10%.

Group	Description	Min.	Max.	Units	Notes
100 MHz	RMS Jitter PCIe G4 (Source: xtal, SSC off)	—	0.40	ps_{RMS}	Note 1, Note 2, Note 3
100 MHz	RMS Jitter PCIe G5 (Source: xtal, SSC off)	—	0.08	ps_{RMS}	Note 4
100 MHz	RMS Jitter PCIe G6 (Source: xtal, SSC off)	—	0.045	ps_{RMS}	Note 4
100 MHz	RMS Jitter PCIe G4 (Source: xtal, SSC: on)	—	0.40	ps_{RMS}	Note 1, Note 2, Note 3
100 MHz	RMS Jitter PCIe G5 (Source: xtal, SSC: on)	—	0.08	ps_{RMS}	Note 4

TABLE 4-7: SKEW AND JITTER (CONTINUED)

Electrical Characteristics: T_A = –40°C to +85°C, Supply Voltage V_{DD} = 3.3V ±10%.

Group	Description	Min.	Max.	Units	Notes
100 MHz	RMS Jitter PCIe G6 (Source: xtal, SSC on)	—	0.045	ps_{RMS}	Note 4
100 MHz	RMS Jitter PCIe G4 (Source: PTI, SSC: off)	—	0.40	ps_{RMS}	Note 1, Note 2, Note 3
100 MHz	RMS Jitter PCIe G5 (Source: PTI, SSC: off)	—	0.08	ps_{RMS}	Note 4
100 MHz	RMS Jitter PCIe G6 (Source: PTI, SSC: off)	—	0.045	ps_{RMS}	Note 4
100 MHz	RMS Jitter PCIe G4 (Source: PTI, SSC: on)	—	0.40	ps_{RMS}	Note 1, Note 2, Note 3
100 MHz	RMS Jitter PCIe G5 (Source: PTI, SSC: on)	—	0.08	ps_{RMS}	Note 4
100 MHz	RMS Jitter PCIe G6 (Source: PTI, SSC: on)	—	0.045	ps_{RMS}	Note 4
100 MHz	CLK to CLK Skew	—	50	ps	—
25 MHz no PFT_IN	Cycle to Cycle jitter	—	60	ps	Absolute
25 MHz	Cycle to Cycle jitter	—	1	ns	Absolute
25 MHz	CLK to CLK Skew	—	1	ns	—

Note 1: Measured into AC test load. See Figure 4-7.

2: Measured from differential cross-point to differential cross-point.

3: Measured after the measurement filter. Sample size 100k clock periods.

4: PCIe Gen5 and Gen6 transfer functions measured with Phase Noise Analyzer.

4.4 Power Noise Tolerance

The simulation model for the noise profile for each VDD pin is given by the following circuit:

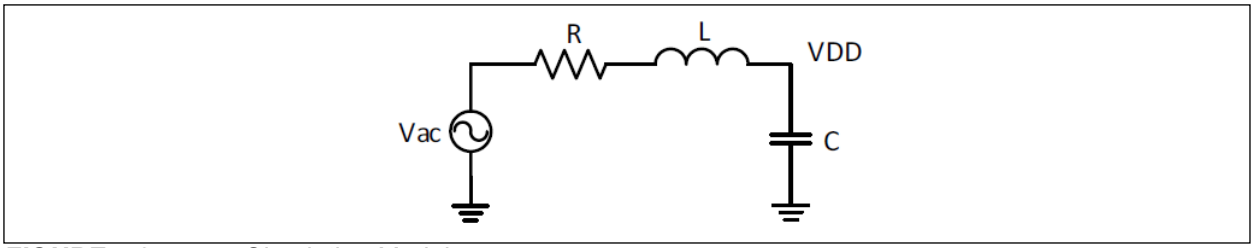


FIGURE 4-8: *Simulation Model.*

V_{AC} is a swept, single-tone sinusoid. R = ½Ω, L = 1 nH, and the decoupling capacitor is 0.1 µF.

The peak noise allowed for the VDD (or VDDA) is given in Table 4-8.

This results in the following maximum noise delivered to the pin of the device:

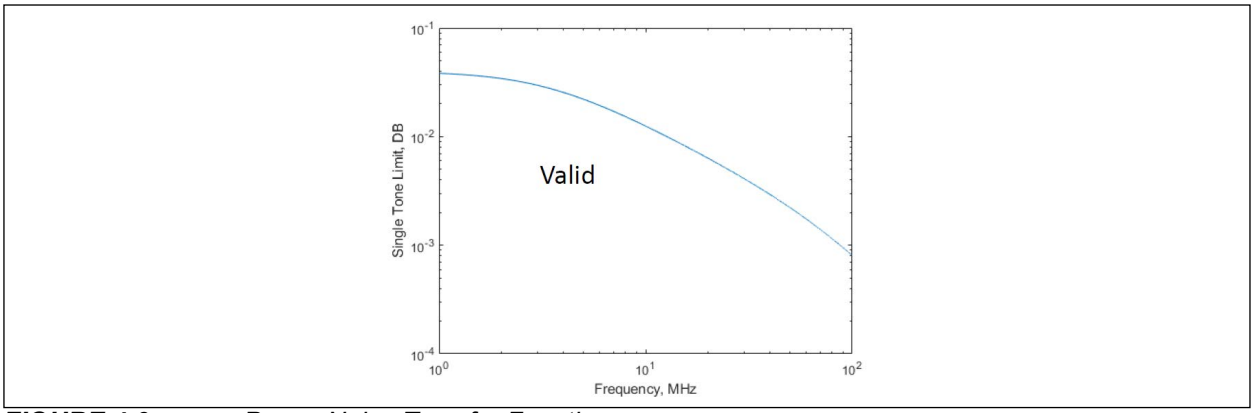


FIGURE 4-9: *Power Noise Transfer Function.*

This is based on the solution to the PDN reference circuit.

EQUATION 4-1:

$$\frac{V_{DD}}{V_{AC}} = \frac{1}{1 + j\omega RC - \omega^2 LC}$$

The jitter and electrical characteristics are met with AC noise present on any of the power pins. The values given are peak to peak electrical noise.

The device meets specification in the presence of at least this much noise on the power pins.

TABLE 4-8: POWER NOISE TOLERANCE: T_A = –40 TO +85°C; SUPPLY VOLTAGE V_{DD} = 3.3 V ±10%

V_{DD} Electrical Noise Range	Symbol	Min.	Typ.	Max.	Units	Notes
f_{NOISE} = 12 kHz to 20 MHz	N_{VDD_MID}	40	—	—	mV_{PP}	Note 1, Note 2, Note 3
f_{NOISE} > 20 MHz	N_{VDD_HIGH}	20	—	—	mV_{PP}	Note 1, Note 2, Note 3
f_{NOISE} = 12 kHz to 25 MHz	$N_{VDDXTAL}$	20	—	—	mV_{PP}	Note 1, Note 2, Note 3

Note 1: The device meets all specification in the presence of noise specified in this table.

2: Jitter and electrical characteristics are met with specified AC noise present on any of the power pins.

3: Over the specified frequency range, a single sinusoid tone should be assumed swept as the worst case.

4.5 SMBus Electrical Characteristics

TABLE 4-9: SMBUS ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Nominal Bus Voltage	VDD_{SMB}	2.7	—	5.5	V	Note 1
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Voltage	V_{IH}	2.1	—	VDD_{SMB}	V	—
Output Low Voltage	V_{OL}	—	—	0.4	V	At $I_{PULLUP(MAX)}$
Input Leakage Current	I_{LEAK}	—	—	±10	µA	—
Current Sinking at $V_{OL(MAX)}$	I_{PULLUP}	—	—	4	mA	—
Pin Capacitive Load	C_L	—	—	12	pF	—
Signal Noise Immunity from 10 MHz to 100 MHz	V_{NOISE}	300	—	—	mV_{PP}	—
Noise Spike Suppression Time	t_{SPIKE}	0	—	50	ns	Note 2
SMBus Operating Frequency	f_{SMB}	10	—	400	kHz	—
Bus Free Time between Stop and Start Condition	t_{BUF}	4.7	—	—	µs	—
Hold Time after (Repeated) Start Condition	$t_{HD:STA}$	4.0	—	—	µs	After this period, the first clock is generated.
Repeated Start Condition Setup Time	$t_{SU:STA}$	4.7	—	—	µs	—
Stop Condition Setup Time	$t_{SU:STO}$	4.0	—	—	µs	—
Data Hold Time	$t_{HD:DAT}$	300	—	—	ns	—
Data Setup Time	$t_{SU:DAT}$	250	—	—	ns	—

TABLE 4-9: SMBUS ELECTRICAL CHARACTERISTICS (CONTINUED)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Clock Low Period	t_{LOW}	4.7	—	—	µs	—
Clock High Period	t_{HIGH}	4.0	—	50	µs	—
Clock/Data Fall Time	t_F	—	—	300	ns	Note 3
Clock/Data Rise Time	t_R	—	—	1000	ns	Note 3

Note 1: 3V to 5V ±10%.

2: Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

3: Rise and fall time is defined as follows: $t_R = (V_{IL(MAX)} - 0.15)$ to $(V_{IH(MIN)} + 0.15)$; $t_F = (V_{IH(MIN)} + 0.15)$ to $(V_{IL(MAX)} - 0.15)$.

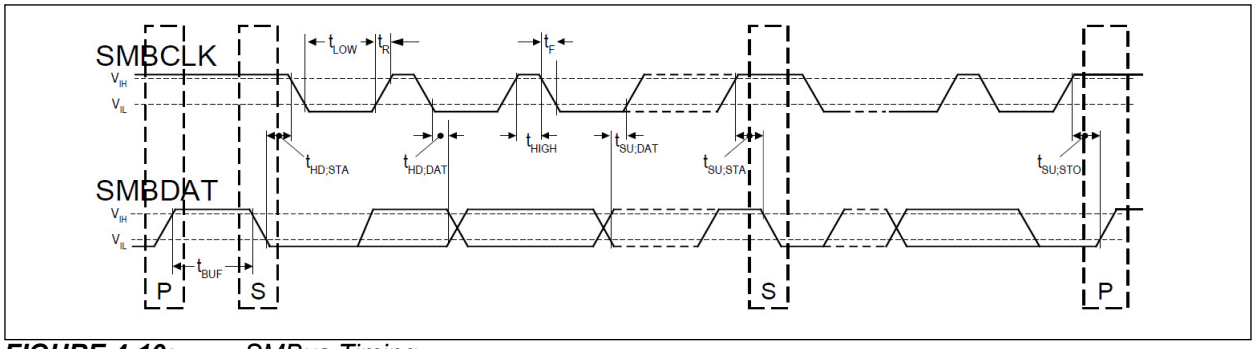


FIGURE 4-10: *SMBus Timing.*

TABLE 4-10: SIDE-BAND INTERFACE ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Clock Period	t_{PERIOD}	40	—	—	ns	—
SHFT Setup Time to Clock	t_{SETUP}	10	—	—	ns	SHFT_LD# high to SBI_CLK rising edge
SBI_IN Setup Time	t_{DSU}	5	—	—	ns	SBI_IN setup to SBI_CLK rising edge
SBI_IN Hold Time	t_{DHOLD}	2	—	—	ns	SBI_IN hold after SBI_CLK rising edge
SBI_CLK to SBI_OUT	t_{CO}	2	—	—	ns	SBI_CLK rising edge to SBI_OUT valid
SHFT Hold Time	t_{SHOLD}	10	—	—	ns	SHFT_LD# hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LD# falling edge)
Enable/Disable Time	$t_{EN/DIS}$	4	—	10	clocks	Delay from SHFT_LD# falling edge to next output configuration taking effect, Note 1
Slew Rate	t_{SLEW}	0.7	—	4	V/ns	SBI_CLK input (between 20% and 80%), Note 2
SBI_OUT Voltage Level High	$V_{SBI\_OUT\_high}$	2.4	—	—	V	SBI_OUT sources 12 mA
SBI_OUT Voltage Level Low	$V_{SBI\_OUT\_low}$	—	—	0.4	V	SBI_OUT sinks 12 mA

Note 1: Refers to the output frequency for the selected clock.

2: Control input must be monotonic from 20% to 80% of input swing.

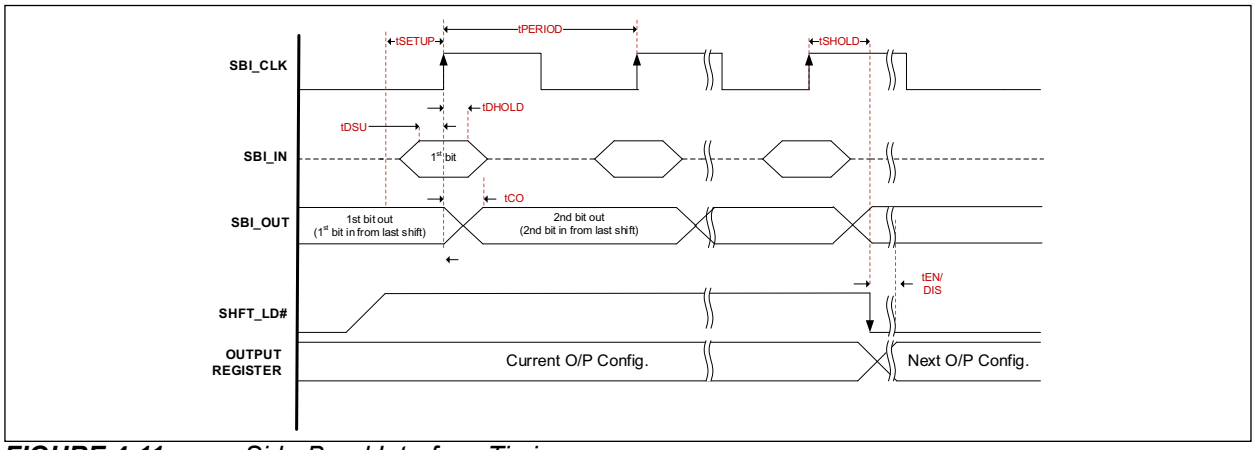


FIGURE 4-11: *Side-Band Interface Timing.*

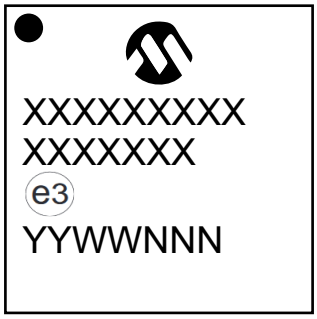
TABLE 4-11: 8 MM X 8 MM UQFN PACKAGE THERMAL PROPERTIES

Parameter	Symbol	Value	Units	Conditions
Maximum Ambient Temperature	T_A	85	°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	125	°C	—
Junction to Ambient Thermal Resistance	θ_{JA}	22.8	°C/W	Still air
		18.4	°C/W	1 m/s airflow
		17.2	°C/W	2.5 m/s airflow
Junction to Board Thermal Resistance	θ_{JB}	7.1	°C/W	—
Junction to Case Thermal Resistance	θ_{JC}	1.2	°C/W	—
Junction to Top-Center Thermal Characterization	ψ_{JT}	0.1	°C/W	Still air

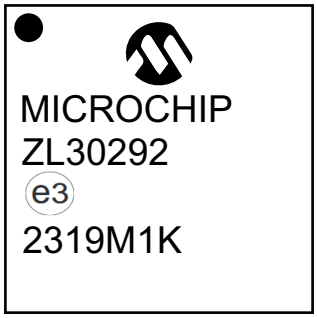
5.0 PACKAGE OUTLINE

5.1 Package Marking Information

100-Lead UQFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

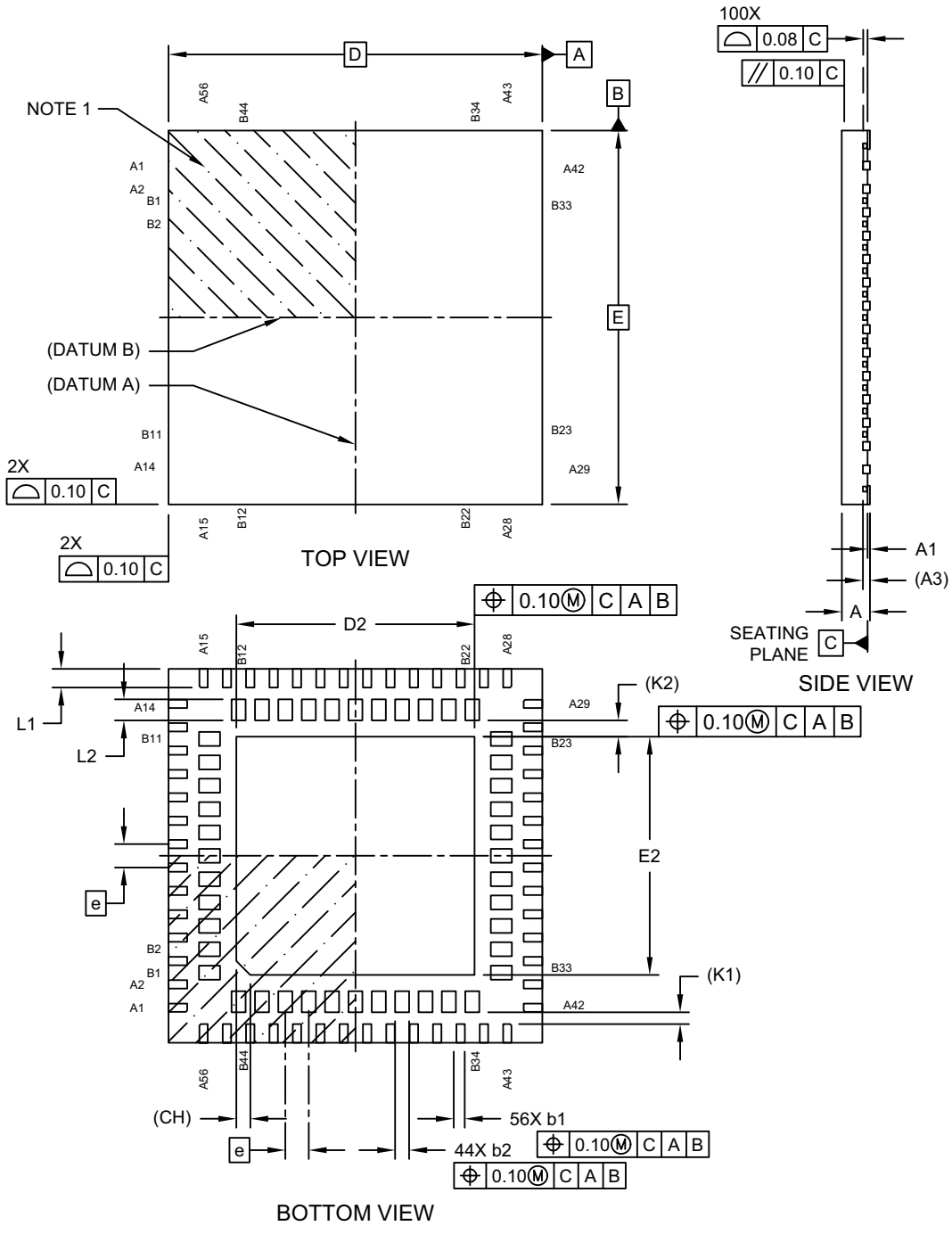
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

100-Lead 8 mm x 8 mm UQFN Package Outline and Recommended Land Pattern

100-Lead Ultra Thin Quad Flat, No Lead Package (D4C) - 8x8X0.6mm Body [UQFN] With Dual Terminal Rows and 5.10 Exposed Pad

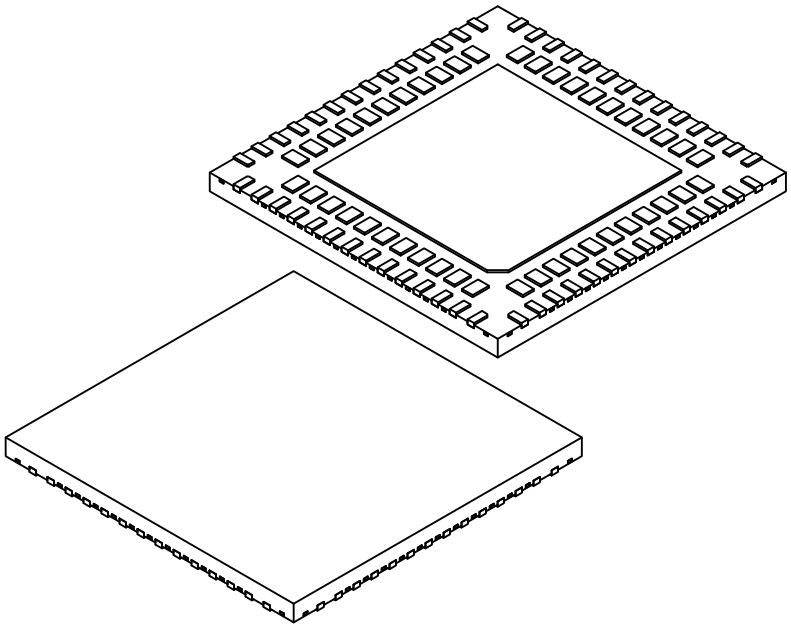
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25520 Rev B Sheet 1 of 2

100-Lead Ultra Thin Quad Flat, No Lead Package (D4C) - 8x8X0.6mm Body [UQFN] With Dual Terminal Rows and 5.10 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.15 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	5.00	5.10	5.20
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	5.00	5.10	5.20
Outer Terminal Width	b1	0.13	0.18	0.23
Inner Terminal Width	b2	0.25	0.30	0.35
Outer Terminal Length	L1	0.35	0.40	0.45
Inner Terminal Length	L2	0.40	0.45	0.50
Outer Terminal to Inner Terminal	K1		0.25 REF	
Inner Terminal-to-Exposed-Pad	K2		0.35 REF	
Exposed Pad Index Chamfer	CH		0.30 REF	

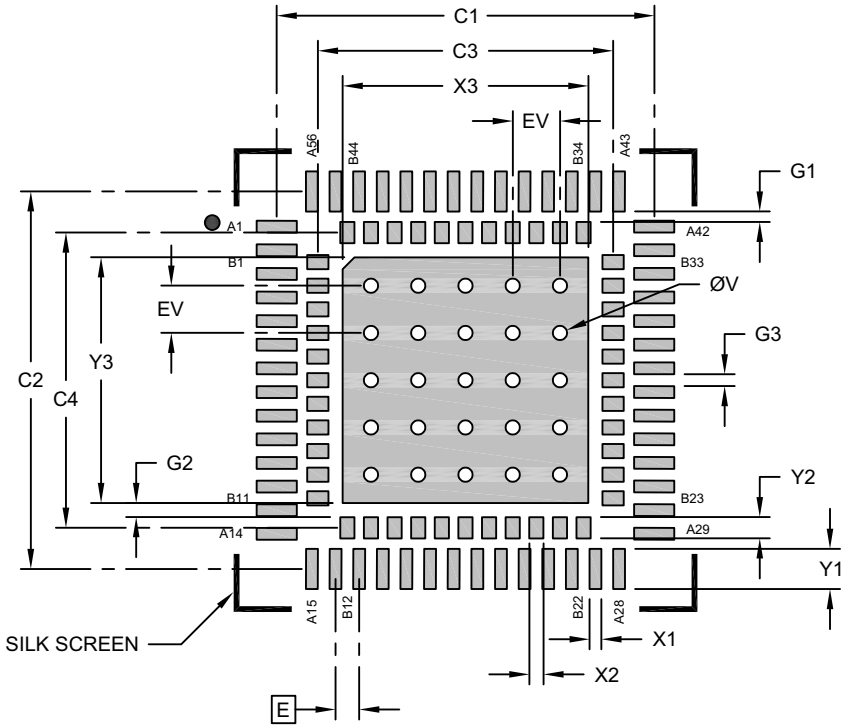
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25520 Rev B Sheet 2 of 2

100-Lead Ultra Thin Quad Flat, No Lead Package (D4C) - 8x8X0.6mm Body [UQFN] With Dual Terminal Rows and 5.10 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X3			5.20
Center Pad Length	Y3			5.20
Contact Pad Spacing Outer Row	C1		7.99	
Contact Pad Spacing Outer Row	C2		7.99	
Contact Pad Spacing Inner Row	C3		6.246	
Contact Pad Spacing Inner Row	C4		6.246	
Contact Pad Width Outer Row (X56)	X1			0.25
Contact Pad Length Outer Row (X56)	Y1			0.85
Contact Pad Width Inner Row (X44)	X2			0.30
Contact Pad Length Inner Row (X44)	Y2			0.45
Contact Pad to Center Pad	G1	0.22		
Contact Pad to Contact Pad	G2	0.30		
Contact Pad to Contact Pad	G3	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27520 Rev B

APPENDIX A: DATA SHEET REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS20006502A (01-28-22)	—	Converted Microsemi data sheet ZL30292 to Microchip DS2000502A. Minor text changes throughout.
DS20006502B (08-09-24)	Table 1-1	Updated pin information in multiple spots.
	Section 2.1	Updated section introductory text.
	Table 2-3	Updated values for first two columns.
	Section 2.14, Section 2.15	Updated * symbol in 2*7 to the ^ symbol.
	Figure 2-10 thru Figure 2-13	Updated * symbol in 2*7 to the ^ symbol.
	Table 3-9	Updated the default value for Revision Code Bit 0.
	Figure 4-1 thru Figure 4-7	Updated all images.
	Table 4-2	Added capacitance content.
	Table 4-3	Updated entire table.
	Table 4-4	Added additional Duty Cycle information.
	Table 4-6	Updated Typical values and added Max values.
	Table 4-7	Added PCI3 Gen 6 content and values.
	Section 5.0	Updated the package outline drawing with the most current version.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Device	X	X	X	X
Part Number	Chip Carrier Type	Package	Media Type	Finish

Device:	ZL30292: PCIe Gen 1/2/3/4/5/6 Clock and Platform Timing Generator
Chip Carrier Type:	L = Leadless Chip Carrier
Package:	D = 100-Lead 8 mm x 8 mm UQFN
Media Type:	F = 2,700/Reel G = 250/Tray
Finish:	1 = Pb Free with Matte Sn lead finish, RoHS e3 Compliant

Examples:

a) ZL30292LDF1:

PCIe Gen 1/2/3/4/5/6 Clock and Platform Timing Generator, Leadless Chip Carrier, 100-Lead UQFN, 2,700/Reel, Pb Free with Matte Sn lead finish, RoHS e3 Compliant

b) ZL30292LDG1:

PCIe Gen 1/2/3/4/5/6 Clock and Platform Timing Generator, Leadless Chip Carrier, 100-Lead UQFN, 250/Tray, Pb Free with Matte Sn lead finish, RoHS e3 Compliant

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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ISBN: 978-1-6683-0114-2

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