APPLICATION NOTE

Hints in Configuring the ATA5745/ATA5746

ATA5745/ATA5746

Introduction

The ATA5745/ATA5746 is a transparent receiver requiring a microprocessor to configure its settings. The block diagram of the receiver is illustrated in Figure 1 on page 2, whereas an example of an application schematic is showed in Figure 2 on page 2. One of the advantages of a transparent receiver is the flexibility offered to designers to apply their own polling scenarios. The purpose of this document is giving designers some guidance, how to configure the ATA5745/ATA5746 for certain schemes and what kind of precautions must be taken to guarantee the reliability of the system. Three receiver configuration schemes will be introduced in this document. First, a simple polling mode, in which the microprocessor switches the receiver between the standby and active mode. Second, the continuous receiving Frequency Shift Keying (FSK) modulation. The continuous receiving Amplitude Shift Keying (ASK) modulation is the last configuration. To simplify the explanation a general transmitted protocol is defined in this document as well as the “Bit Check” algorithm. Finally designers can define their own protocol, “Bit Check” algorithm and configuration, which is mostly the combination of the three introduced configurations.

Figure 1. Block Diagram of ATA5745/ATA5746

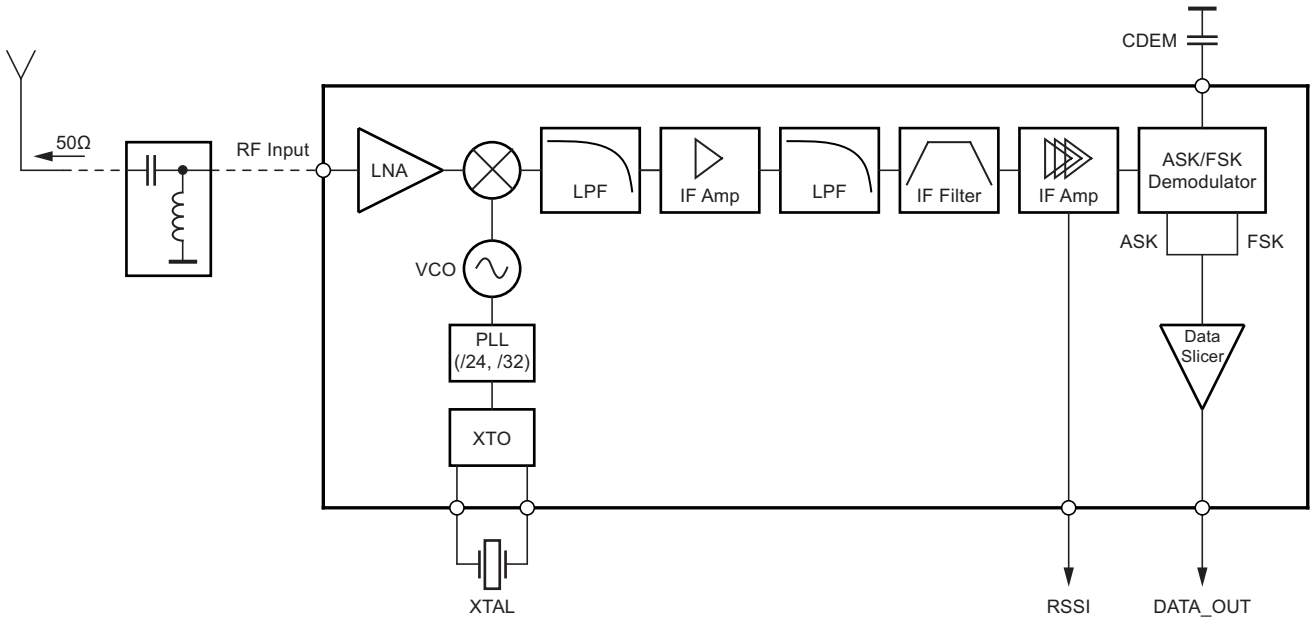
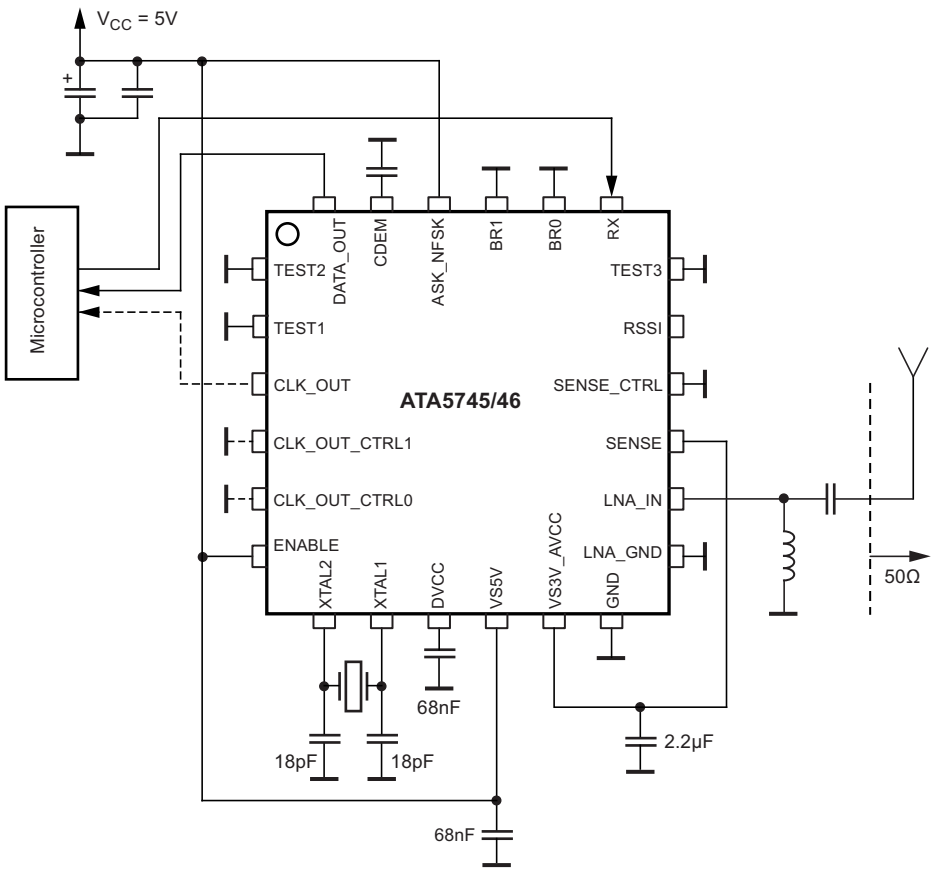


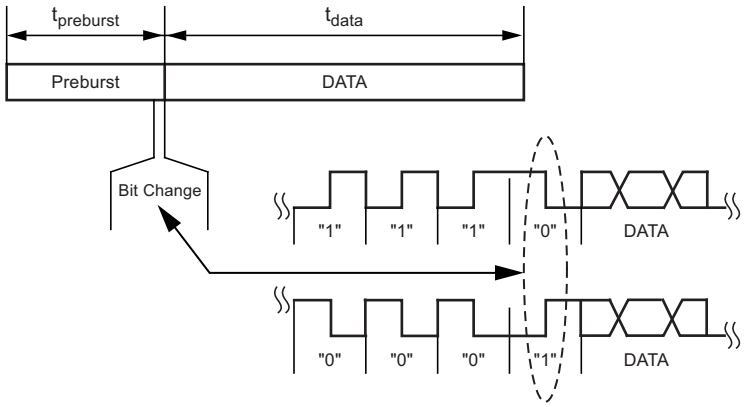
Figure 2. Application Schematic as an Example (ASK Modulation, Data Rate 1kBps (Manchester), Power Supply 5V)



1. Definition of the Transmitted Protocol

In this document the Manchester coding is used for the data communication between transmitter and receiver. The transmitted protocol is defined in Figure 1-1 and made up of preburst and data section. The preburst is defined as sequence of identical bits (“...11111...” or “...00000...”) and must be Manchester coded. In addition, between the preburst and the data there must be a bit change as a synchronization point.

Figure 1-1. Definition of the Transmitted Protocol



2. A Simple Polling Scenario

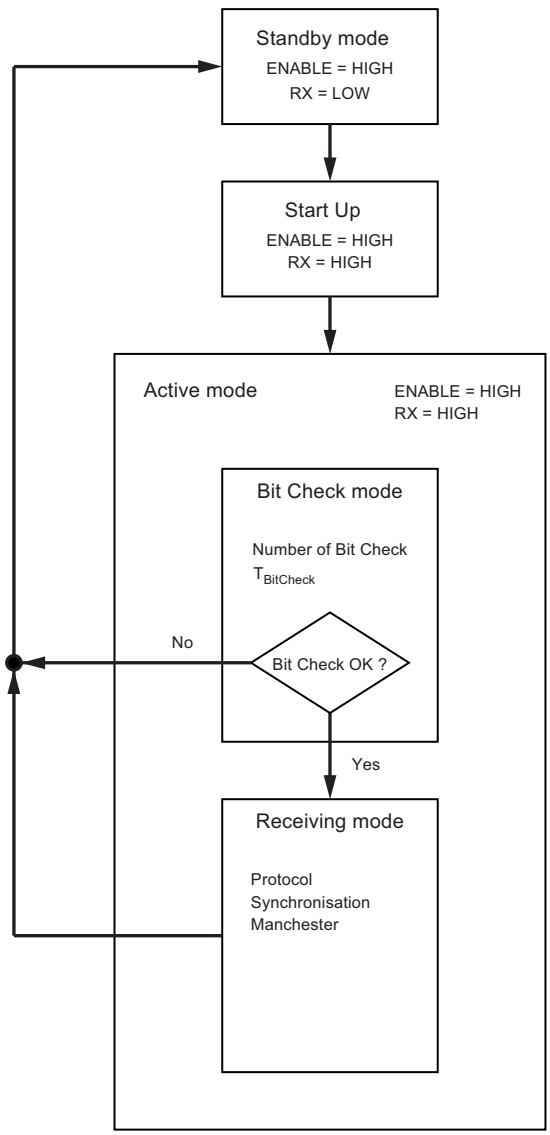
The definition of “polling” is alternating between stand by mode and active mode in the application of the receiver. A microprocessor is necessary to configure the ATA5745/ATA5746 in this polling mode, because the receiver does not have any internal polling logic circuitry (transparent receiver). With the polling method the current consumption will be heavily reduced as the whole receiver's circuit is not continuously active.

As soon as the ATA5745/ATA5746 is activated, the receiver will receive and process “any” signal, which is recognized at the antenna and thus RF input. Undefined pulses (we defined as “digital noise”) will be observed on the DATA_OUT pin, in case that no (valid) signal occurs at the antenna (RF input). A simple “Bit Check” algorithm for the microprocessor to detect the valid protocol in the “digital noise” will be introduced.

Figure 2-1 on page 4 shows the flow chart of this simple polling scenario. The polling scenario is subdivided in three sections. It begins with stand by mode followed by receiver’s start up activity and at last the active mode. “Bit Check” process will be performed at the beginning of the active mode to decide whether the receiver will be set into stand by mode or it has to receive a data. After receiving the data, the microprocessor sets the receiver in stand by mode again.

The details of each mode will be described in the next sections.

Figure 2-1. Flow Chart of the Polling Scenario



2.1 Stand by Mode

If ENABLE pin is set to HIGH and RX pin to LOW, the ATA5745/ATA5746 is programmed in stand by mode. In this mode all the circuit of the receiver except the crystal oscillator (XTO) is deactivated. In this mode the receiver can generate a clock signal at CLK_OUT pin, which can be configured by CLK_OUT_CTRL0 pin and CLK_OUT_CTRL1 pin. Three different clock frequencies with a crystal precision can be used for an external microprocessor as a reference. More detailed information can be read in the ATA5745/ATA5746 datasheet, section 3.1.

2.2 Start Up

As soon as both pins ENABLE and RX are set to HIGH, the receiver will be started up beginning at the Phase Locked Loop (PLL) circuit and followed by the analog signal processing section. During the start up process the ATA5745/ATA5746 is not able to receive any signal, therefore, the timing for the start up of PLL as well as of the analog signal processing unit must be taken into account in the system configuration. The timing of the receiver's start up can be obtained from Table 2-1.

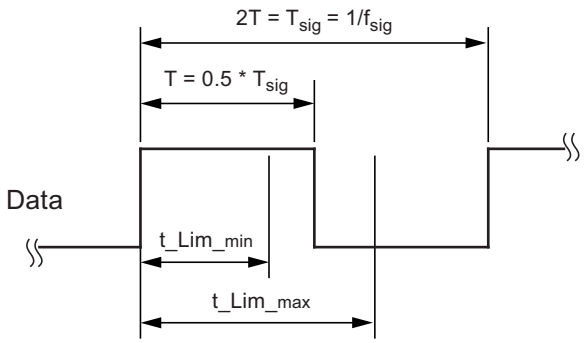
Table 2-1. Start-up Time

BR1	BR0	ATA5745 (433.92MHz)		ATA5746 (315MHz)	
		$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$	$T_{Startup\_PLL}$	$T_{Startup\_Sig\_Proc}$
0	0	261µs	1096µs	269µs	1132µs
0	1		644µs		665µs
1	0		417µs		431µs
1	1		304µs		324µs

2.3 Active Mode

As previously mentioned at the beginning of the active mode the "Bit Check" process will be performed. The principle of the "Bit Check" is scanning for a valid preburst in the "digital noise". After the microprocessor found the valid preburst (Bit Check is successful) the receiver will receive the data further. Two conditions bring the receiver to the stand by mode again, first if the Bit Check is not successfully performed and second if the whole data is received.

Figure 2-2. Valid Time Window for Bit Check



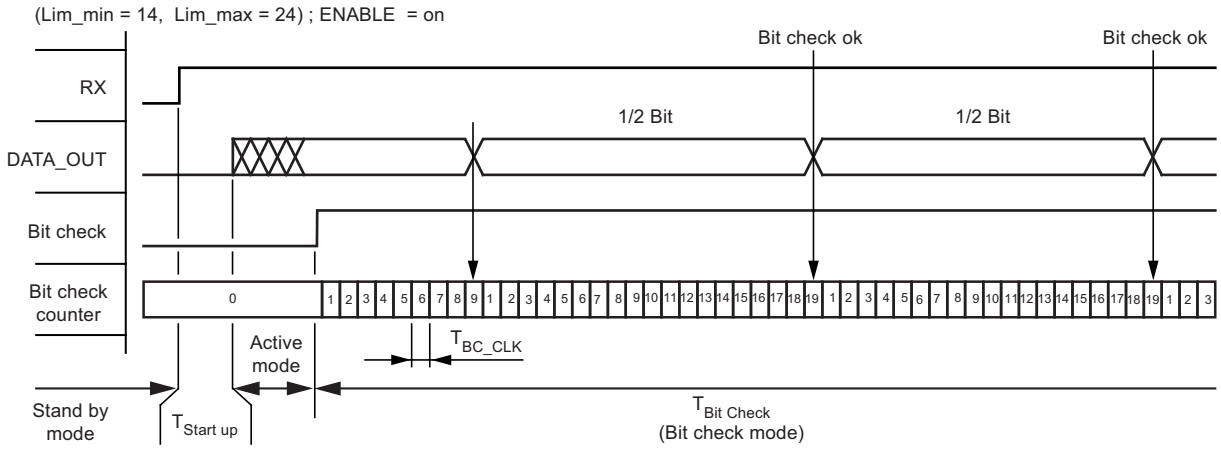
2.3.1 Bit Check Processing

In this mode the microprocessor measures the edge to edge time (T) of the found pulses on the DATA_OUT pin. The measured edge to edge time must be within a defined time range for a valid Bit Check. The Figure 2-2 on page 5 describes the valid time window for a Bit Check.

Notes and definition for the Bit Check process,

- The value f_{sig} is the frequency of the signal data to be received and thus T_{sig} is the period of the signal.
- The edge to edge time (T) is the half of signal period (T_{sig}), this means $T = 0.5 \times T_{sig}$.
- The correlation t_Lim_min < T < t_Lim_max must be fulfilled in the Bit Check process.

Figure 2-3. Timing Diagram During Bit Check



For the Bit Check processing three variables must be defined in the microprocessor, first is the Bit Check counter and second, the basic clock signal (T_{BC_CLK}) for the counter. Last but not least is the number of bits (N) to be checked.

- The correlation between the basic clock signal (T_{BC_CLK}) and valid time window is $t\_Lim\_min = Lim\_min \times T_{BC\_CLK}$; $t\_Lim\_max = Lim\_max \times T_{BC\_CLK}$
- CV is the counted value by the Bit Check Counter, $T = CV \times T_{BC\_CLK}$
- A half bit is valid, if Lim_min < CV < Lim_max
- The “Bit Check” is successful, if the edge to edge time for the whole N bits is valid.

The number of bits (N) to be checked have to be defined very carefully, because the wake up frequency of the receiver depends on this value. The Bit Check number 9 is recommended. If the transmitted protocol does not allow such a long time for “Bit Check”, at least 3 Manchester Bits must be verified. As an example, a Bit Check number of 3 is used for the further explanation.

The Bit Check counter must be restarted if an edge is detected. If the “Bit Check” fails for the first edge to edge time, the microcontroller sets the receiver into the stand by mode. Figure 2-3 on page 6, Figure 2-4 on page 7, Figure 2-5 on page 7 and Figure 2-6 on page 7 illustrate the Bit Check process by the microcontroller.Figure 2-7 on page 8 shows the flow chart of the Bit Check processing.

Figure 2-4. Timing Diagram for Failed Bit Check (CV < Lim_min)

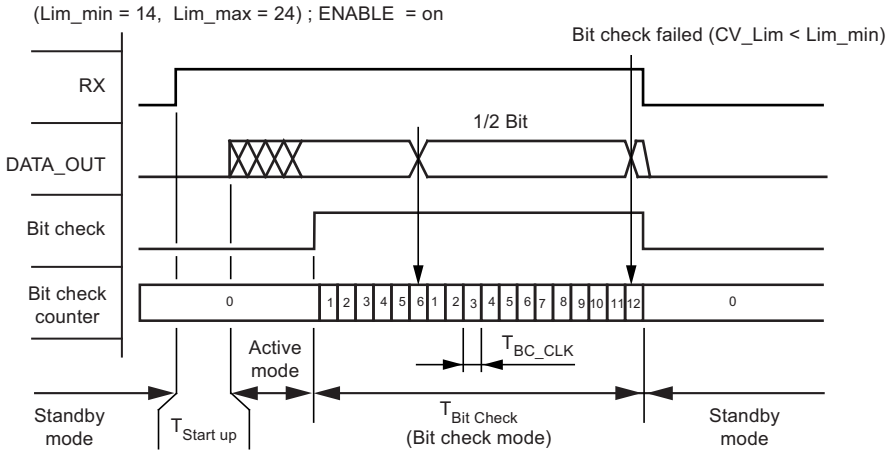


Figure 2-5. Timing Diagram for Failed Bit Check (CV ≥ Lim_max)

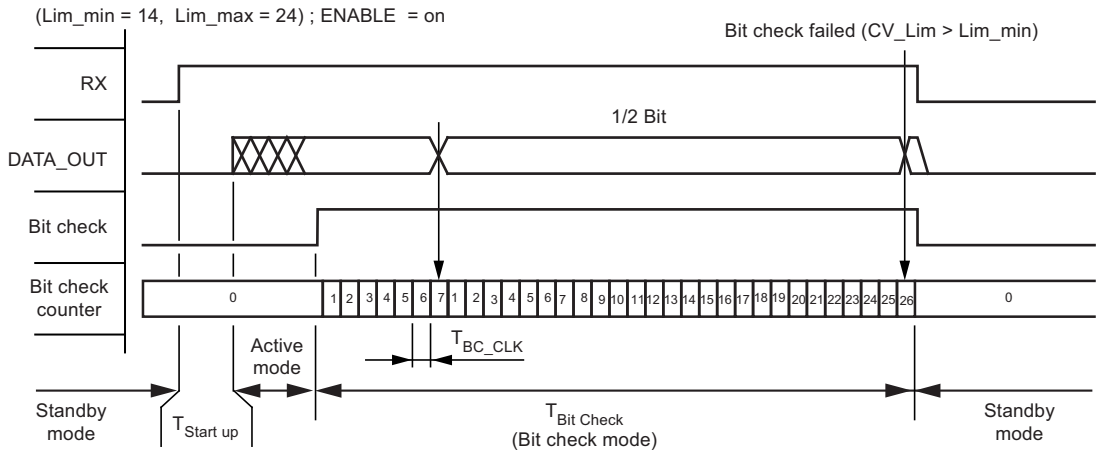


Figure 2-6. Timing Diagram for Successful Bit Check (Number of Bits to Be Checked is 3)

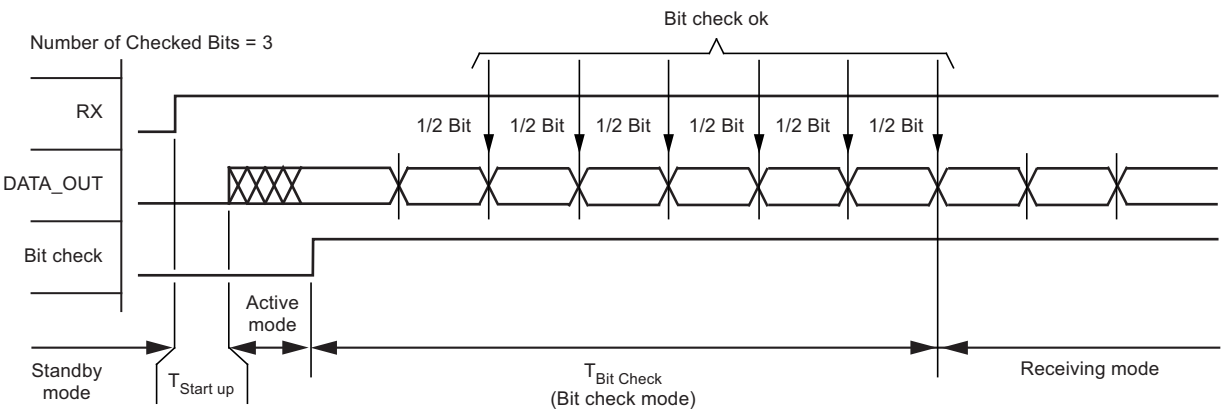
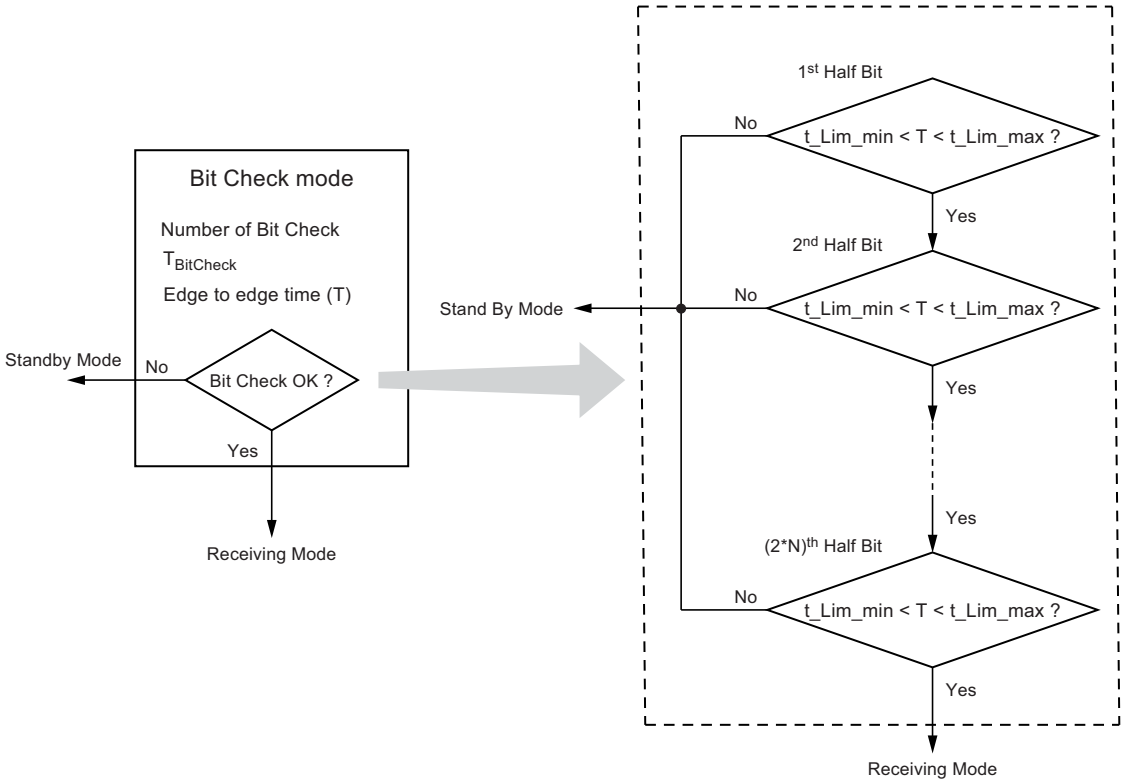
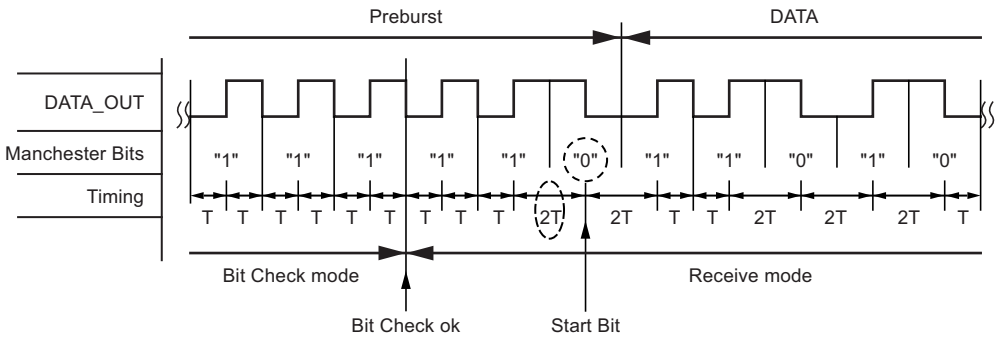


Figure 2-7. The Principle Flow Chart of the Bit Check Processing



2.3.2 Receiving Mode

Figure 2-8. The Synchronization of the Received Data Stream

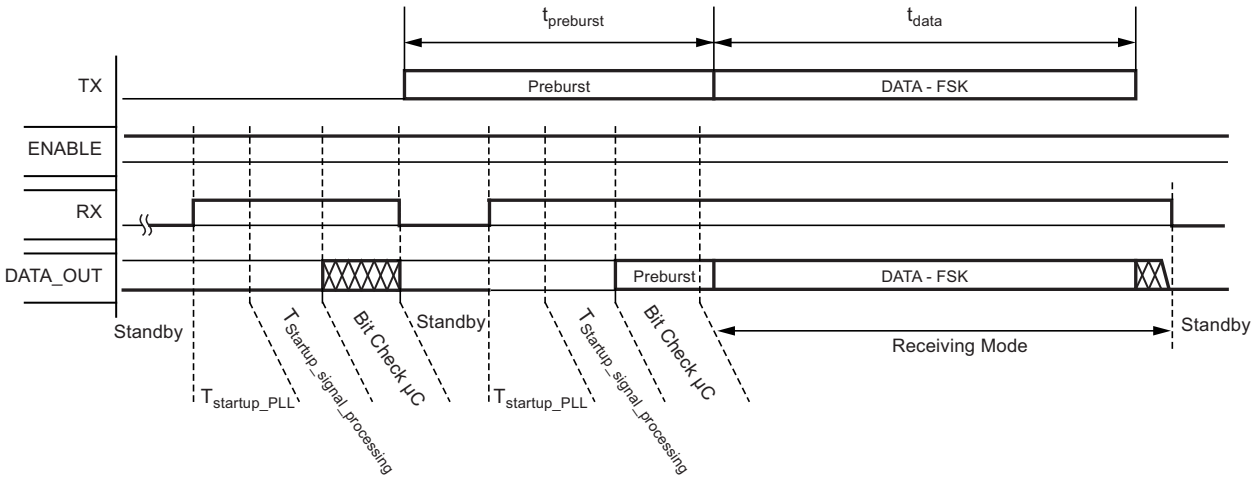


After the Bit Check is successfully verified the data stream on the pin DATA_OUT must be processed further. The Bit Change in the protocol (see Figure 2-8) is very useful on this step as a synchronization point (this bit change is defined as Start Bit) to determine the beginning of the real data. This method allows also a convenient Manchester decoding. After the complete data stream is processed the receiver will be set into stand by mode. Figure 2-9 on page 9 shows the principle of receiving a data stream.

2.3.3 Required Protocol's Preburst Length

Important for the system reliability is the calculation of the protocol's preburst length in regard of the polling mode timing. The following correlation must be fulfilled, $t_{preburst} \geq T_{stand\ By} + T_{start\ up} + T_{Bit\ Check}$ (assumed the microcontroller is continuously active).

Figure 2-9. The Principle of the Receiving Data Stream

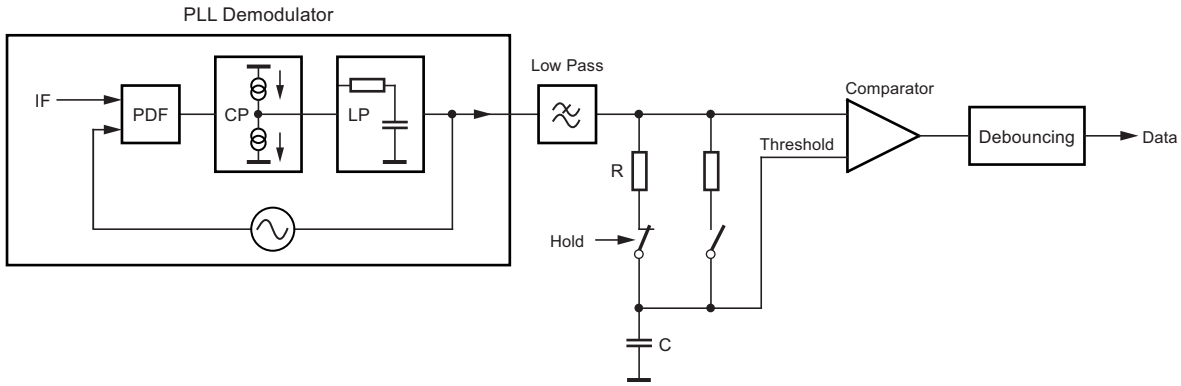


3. Continuous Receiving FSK Modulation

Because a PLL circuit is implemented at the ATA5745 and ATA5746's FSK demodulator (caution: this is not the PLL for the RF section), in the application of a continuous FSK receiving a precaution must be taken by the designer to prevent a data loss. The principle of FSK analog signal processing of the receiver is illustrated in Figure 3-1 on page 10. If there is no FSK signal at the RF input and thus at the intermediate frequency (IF) input of the PLL demodulator, the PLL demodulator will lock to an “undefined” frequency. In certain cases, the reference frequency of the PLL demodulator stays on the edge of the VCO’s frequency range and hence the demodulator will not be able to track the valid incoming signal properly or in worst case not at all. In this event, a HIGH or LOW level on the DATA pin will be observed and the receiver will lose the data. In order to avoid the loss of data in the application the demodulator must be reinitiated. Reinitializing of the analog signal processing for ATA5745/46 can be started by toggling the ASK_NFSK pin.

In case of FSK continuous receiving of the ATA5745/ATA5746, a toggling on the ASK_NFSK pin is necessary to avoid any loss of data. With this toggling method, the analog signal processing section of the receiver is initiated periodically.

Figure 3-1. FSK Analog Signal Processing of ATA5745/ATA5746



3.1 Reinitializing the Analog Signal Processing by Toggling the ASK_NFSK Pin

As mentioned previously, a toggling on the ASK_NFSK pin is required in FSK continuous receiving mode to prevent data loss. Figure 3-2 shows the principle of receiving the transmitted protocol using a toggling method on the ASK_NFSK pin. The Enable, RX, BR0, and BR1 pins are all set to HIGH. The TX row in Figure 3-1 shows the transmitted data.

Toggling the ASK_NFSK pin initiates the receiver's analog signal processing. This takes 304µs ($T_{startup\_sig\_proc}$) for the BR_Range3. For more information, please see the data sheet ATA5745/ATA5746.

Figure 3-2. Receiving the Transmitted Protocol Using Toggling Method on ASK_NFSK Pin

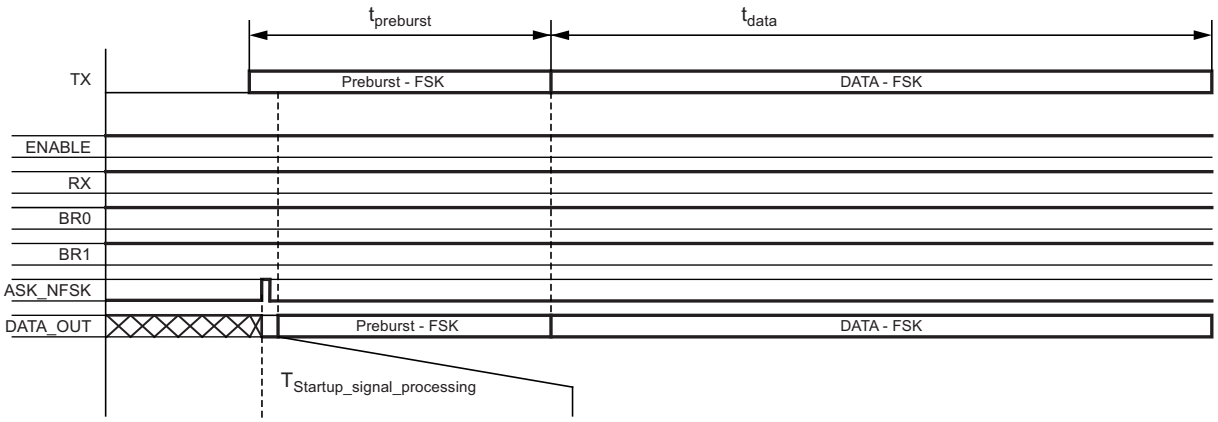


Figure 3-3 illustrates the pulse width (t_w) of the toggle signal on the ASK_NFSK pin. The pulse width must be short in comparison to the start-up timing of the signal processing. In our example, BR_Range3, the start up timing of the signal processing is 304µs. In this case, a pulse width of 10µs can be chosen.

Figure 3-3. Toggle Signal (t_w) on the ASK_NFSK Pin and Start-up Timing for Signal Processing

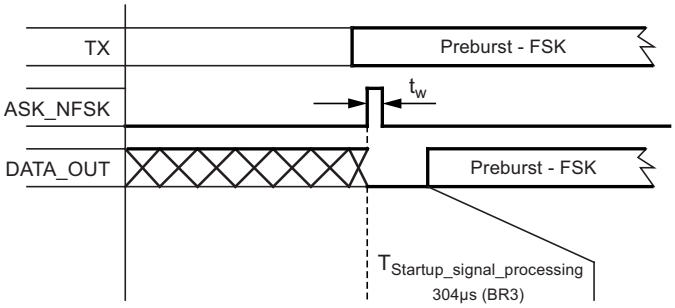
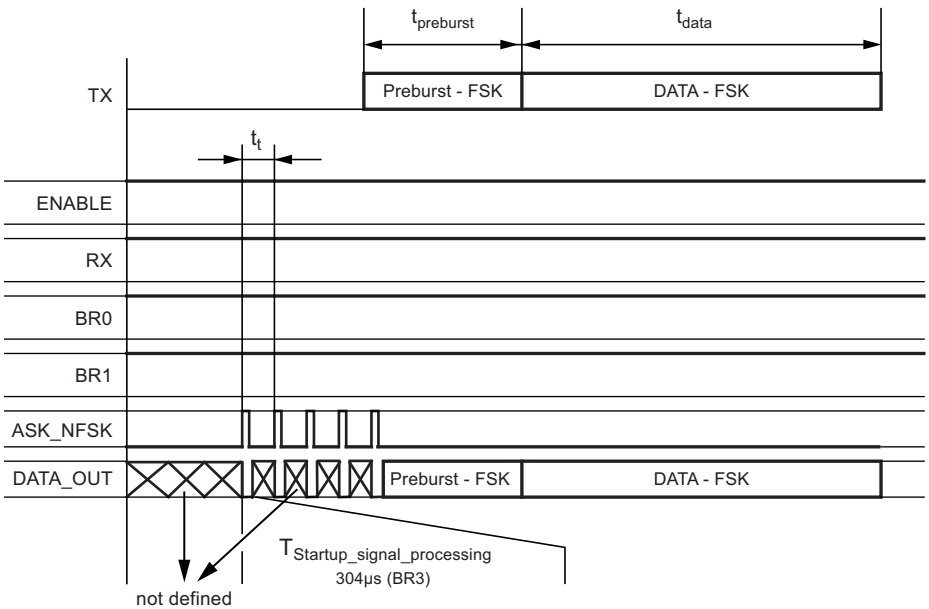


Figure 3-4 shows the toggling scheme of the ASK_NFSK pin and the principle of the receiving valid incoming signal. The value t_t is the time between two toggling pulses. This value consists of the start-up time for signal processing and the timing for the Bit Check performed by the microprocessor. The “Bit Check” process is addressed in the Section 2.3.1 on page 6 this document.

Figure 3-4. Receiving the Transmitted Protocol Using Toggling on the ASK_NFSK Pin Including Timing between Two Toggling pulses (t_t)



3.2 Example for t_t Calculations

As an example, the microprocessor will check only 3 bits of the preburst, which takes a period of 364.6µs (3.5/9600). In this case, the value of t_t is calculated as:

t_t = 304µs + 364.6µs = 668.6µs ≈ 669µs

Note: The value 3.5 is chosen to guarantee the maximum Bit Check timing for 3 bits to be checked.

If the number of bits to be checked is 9 the value of t_t is calculated as:

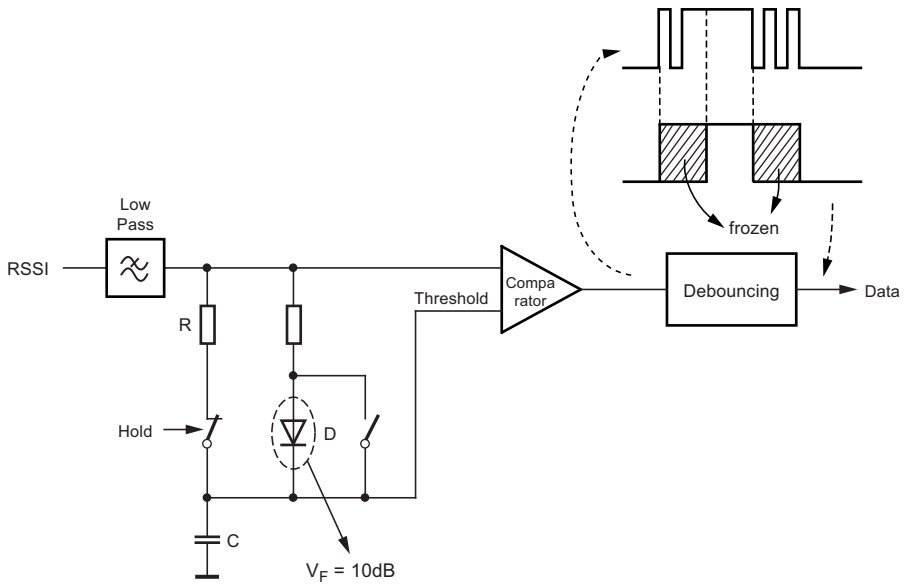
t_t = 304µs + 989.6µs = 1293.6µs ≈ 1.3ms.

4. Continuous Receiving ASK Modulation

Figure 4-1 shows the equivalent circuit of the ASK signal processing in ATA5745/ATA5746. The description starts after the RSSI signal evaluation. The RSSI signal will be passed to the comparator through a low pass filter. The threshold of the comparator is automatically determined by the circuits whose functionality is simplified by resistor R, capacitor C and diode D (assumption: VF is 10dB).

Note: The capacitor C is the capacitor, which is connected on CDEM pin.

Figure 4-1. The Simplified Equivalent Circuit for the ASK Signal Processing



The voltage on CDEM pin is very important for the demodulating process, since this voltage is decisive in setting the threshold value. The voltage on CDEM will be charged by powering the capacitor with current (ICDEM).

Because of the threshold value will be automatically processed, in absence of a RF signal (no carrier), also known as “blanking time”, the threshold value will be determined from the noise floor. This will cause “digital noise” to occur on the demodulator output (data output) if no countermeasure is implemented.

To handle the blanking time in ASK mode, the voltage of CDEM will be “frozen”. So the data filter will be stable during the blanking period and the receiver can demodulate the incoming protocol after the break (blanking time) outright. The principle of this “HOLD” function is described in the Figure 3-4 on page 11. This method allows the ATA5745/ATA5746 to demodulate protocols, which contain a blanking time within the protocol. ATA5745/ATA5746 can process such kind of protocol with a blanking time up to 52ms. A time out for this freezing functionality is not implemented in ATA5745/ATA5746. The worst case is, after receiving the complete data the ASK signal disappears abruptly. Hence, the threshold value is frozen. If, during this time, a ASK signal returns with a lower power than the last signal, the receiver will not detect it. In order to prevent the loss of data in worst case this kind of application requires a microprocessor which monitors the DATA_OUT pin and implements a kind of time out for the freezing functionality. After receiving the complete protocol the microprocessor has to toggle the pin ASK_NFSK to start up the analog signal processing.

5. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4995C-AUTO-05/15	• Put document in the latest template
4995B-AUTO-02/08	• Section 4.1 “Reinitializing the Analog Signal Processing by Toggling the ASK_NFSK Pin” on page 10 updated

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**