MICROCHIP

USB82514

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip USB82514. These checklist items should be followed when utilizing the USB82514 in a new design. A summary of these items is provided in Section 9.0, "Hardware Checklist Summary," on page 11. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "USB Signals"
- Section 5.0, "USB Connectors"
- Section 6.0, "Clock Circuit"
- Section 7.0, "Power and Startup"
- Section 8.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

- The ePad, **VSS**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

2.3 USB-IF-Compliant USB Connectors

- The USB82514 upstream facing port is Type-B. The hub downstream facing ports are Type-A. USB-IF-certified USB connectors with a valid Test ID (TID) are required for all USB products to be compliant and pass USB-IF product certification.

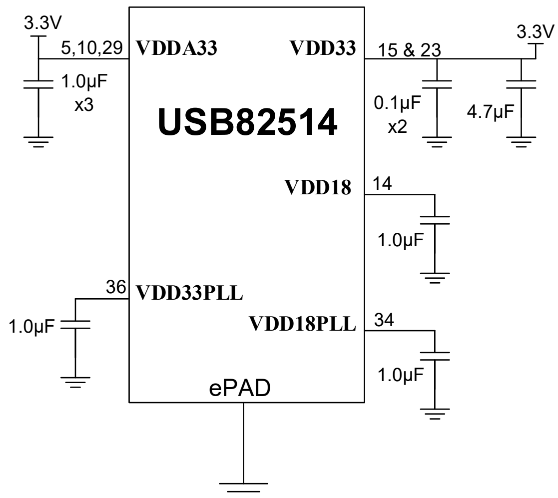
3.0 POWER

3.1 Power and Bypass Capacitance

- The **VDD33** pins (pins 15 and 23) require 1.0 µF bypass capacitors (x2).
- The **VDDA33** pins (pins 5, 10, and 29) should include a 1.0 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **VDD33PLL** pin (pin 36) requires a 1.0 µF bypass capacitor to VSS.
- The **VDD18** pin (pin 14) must have a 1.0 µF capacitor to VSS.
- The **VDD18PLL** pin (pin 34) must have a 1.0 µF filter capacitor to VSS.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



4.0 USB SIGNALS

4.1 USB PHY Interface

- **USBUP_DP** (pin 31): This pin is the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D+/DP pin of a USB connector.
- **USBUP_DM** (pin 30): This pin is the negative (–) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. This pin can connect directly to the D–/DM pin of a USB connector.
- **USBDN[4:1]_DP** (pins 2, 4, 7, and 9): These pins are the positive (+) signal of the upstream USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D+/DP pin of a USB connector.
- **USBDN[4:1]_DM** (pins 1, 3, 6, and 8): These pins are the negative (–) signal of the downstream port 1 USB2.0 differential pair. All necessary USB terminations and resistors are included in the IC. These pins can connect directly to the D–/DM pin of a USB connector.

Note: The polarity of any of the USB2.0 differential pairs may be inverted either intentionally due to design constraints or to correct a design error using the Microchip PortSwap feature. This feature may be configured via SMBus/I^2C configuration registers.

The transmit and receive channel connection details, refer to Figure 4-1 and Figure 4-2.

FIGURE 4-1: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS UPSTREAM USB PORTS

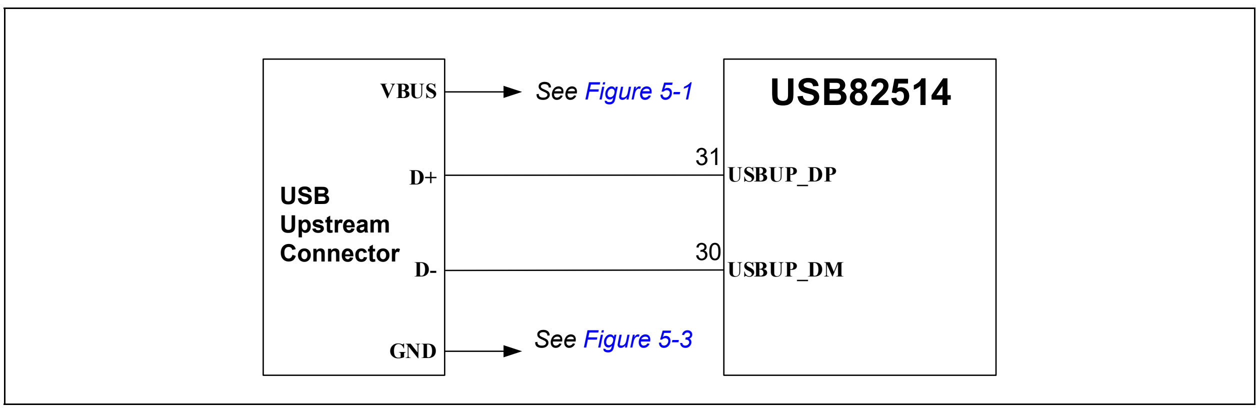
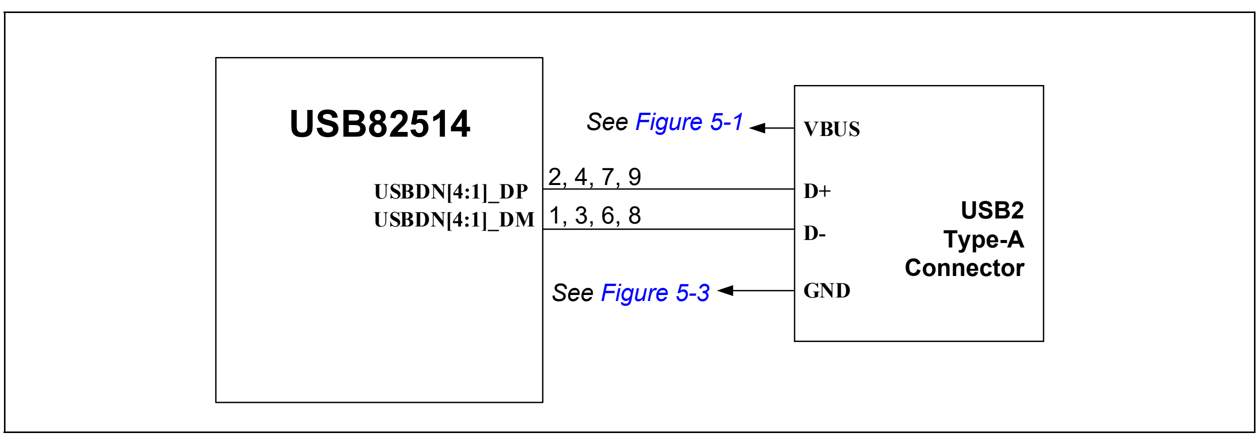


FIGURE 4-2: TRANSMIT AND RECEIVE CHANNEL CONNECTIONS DOWNSTREAM USB PORTS



4.1.1 DISABLE DOWNSTREAM PORTS IF UNUSED

If downstream ports are unused, they should be disabled. This can be achieved through a port disable strap option.

If using the port disable strap option, the USBDNx_DP and USBDNx_DM signals should be pulled high to 3.3V. This connection can be made directly to the 3.3V power net, or through a pull-up resistor.

4.2 USB Protection

The use of external protection circuitry may be required to provide additional ESD protection beyond what is included in the hub IC. These generally are grouped into three categories:

- TVS protection diodes
  - ESD protection for IEC-61000-4-2 system-level tests
- Application-targeted protection ICs or galvanic isolation devices
  - DC overvoltage protection for short-to-battery protection
- Common-mode chokes
  - For EMI reduction

The USB82514 can be used in conjunction with these types of devices, but it is important to understand the negative effect that these devices may have on USB signal integrity and to select components accordingly and to follow the implementation guidelines from the manufacturer of these devices. The following general guidelines may also be used for implementing these devices:

- Select only devices that are designed specifically for high-speed applications. Per the USB specification, a total of 5 pF is budgeted for connector, PCB traces, and protection circuitry.
- Place these devices as close as possible to the USB connector.
- Never branch the USB signals to reach protection devices. Always place the protection devices directly on top of the USB differential traces.
- Always ensure a very low impedance path to a large ground plane. The effectiveness of TVS devices depends heavily on effective grounding.
- Place TVS diodes on the same layer as the USB signal trace. Avoid vias or place vias behind the TVS device if possible.

Note: Microchip PHYBoost, VariSense™, and High-Speed Disconnect Threshold adjustment configuration options are available for compensating the negative effects of these devices. These features can help to overcome marginal failures. It is simplest to determine the appropriate setting using lab experiments, such as USB eye diagram tests, on physical hardware.

5.0 USB CONNECTORS

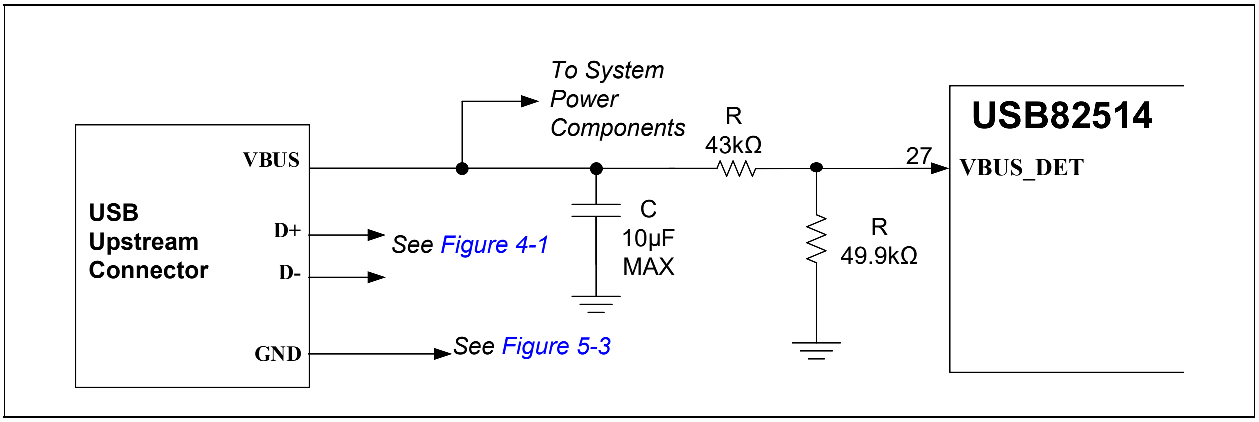
5.1 Upstream Port VBUS and VBUS_DET

The upstream port VBUS line must have no more than 10 µF of total capacitance connected.

The USB82514 uses the VBUS_DET signal to detect the presence of a USB host.

The recommended implementation is shown in Figure 5-1.

FIGURE 5-1: RECOMMENDED UPSTREAM PORT VBUS CONNECTIONS



5.2 Downstream Port VBUS and PRTPWR/OCS_N

The **PRTPWR** and **OCS_N** pins are hybrid I/O pins that support the following states:

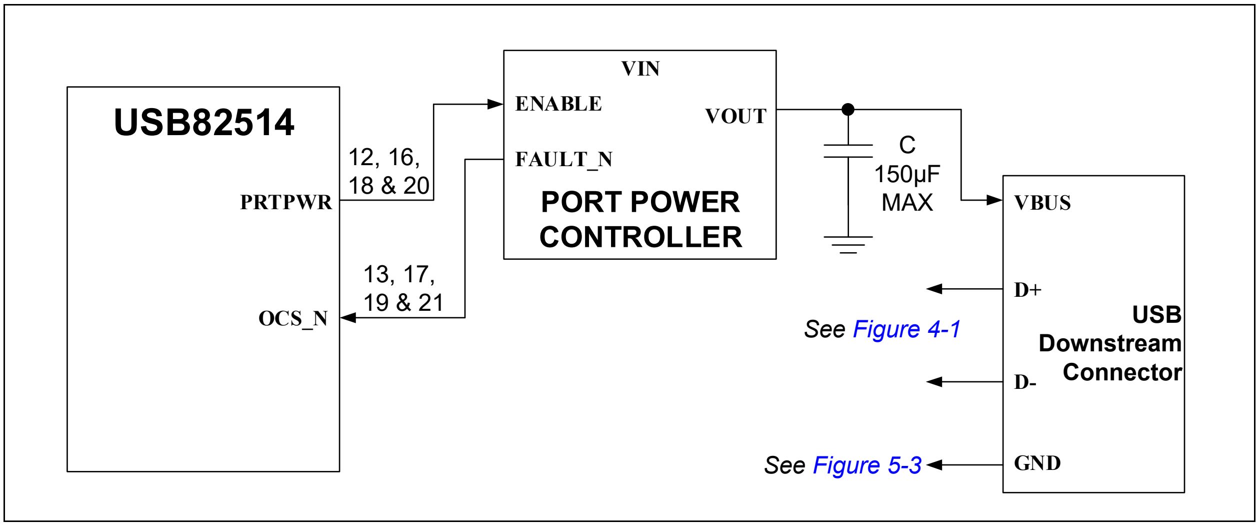
- *PORT OFF*: **PRTPWR** is an output and drives low. The **PRTPWR** pin only transitions to the PORT ON state through a specific command from the USB host.
- *PORT ON*: The **OCS_N** is an input buffer that monitors overcurrent events, which are indicated by the port power controller by pulling the OCS_N line low. Once an overcurrent event is detected, the **PRTPWR** automatically moves to the PORT OFF state until the USB host can be notified of the overcurrent event.

When connecting the **PRTPWR** and **OCS_N** pins to a port power controller, the signals should be connected to both the Enable pin and the fault indicator pins of the port power controller. Do not place an external pull-up resistor on the line.

> **Note:** The overcurrent detect debounce parameters are configurable and may be adjusted if required to operate properly with the selected port power controller.

A typical implementation is shown in Figure 5-2.

FIGURE 5-2: DOWNSTREAM VBUS AND PRTCTL CONNECTIONS



Note: The implementation as shown in Figure 5-2 assumes that the port power controller has an active-high Enable input, and an active-low, open-drain style fault indicator. External polarity inversion through buffers or FETs may be required if the port power controller has different I/O characteristics.

5.3 GND and EARTH Recommendations

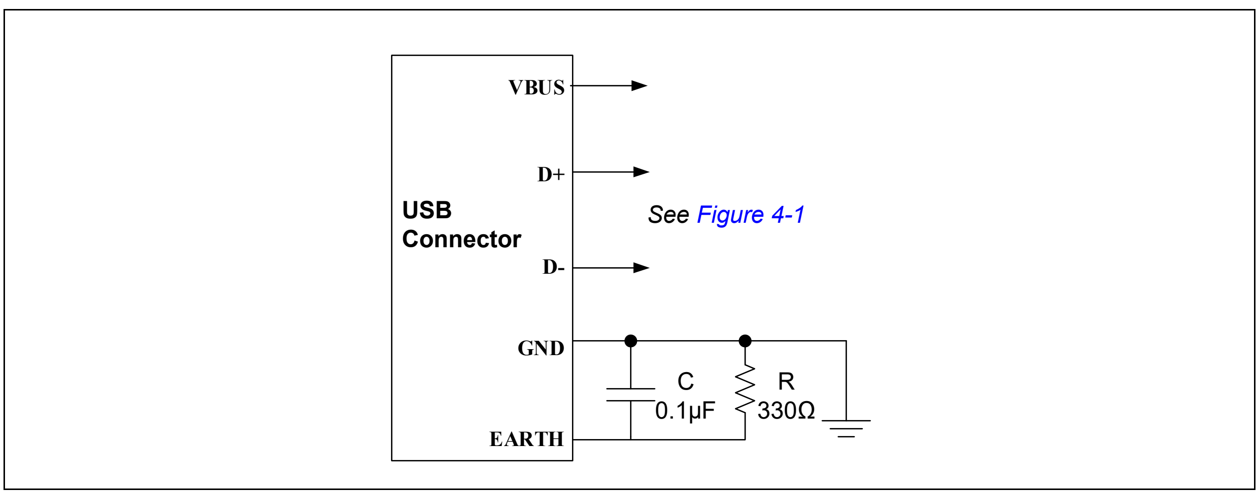
The GND pins of the USB connector must be connected to the PCB with a low impedance path directly to a large GND plane.

The EARTH pins of the USB connector may be connected in one of two ways:

- (*Recommended*) To GND through a resistor and capacitor in parallel. An RC filter can help to decouple and minimize EMI between a PCB and a USB cable.
- Directly to the GND plane.

The recommended implementation is shown in Figure 5-3.

FIGURE 5-3: RECOMMENDED USB CONNECTOR GND AND EARTH CONNECTIONS



6.0 CLOCK CIRCUIT

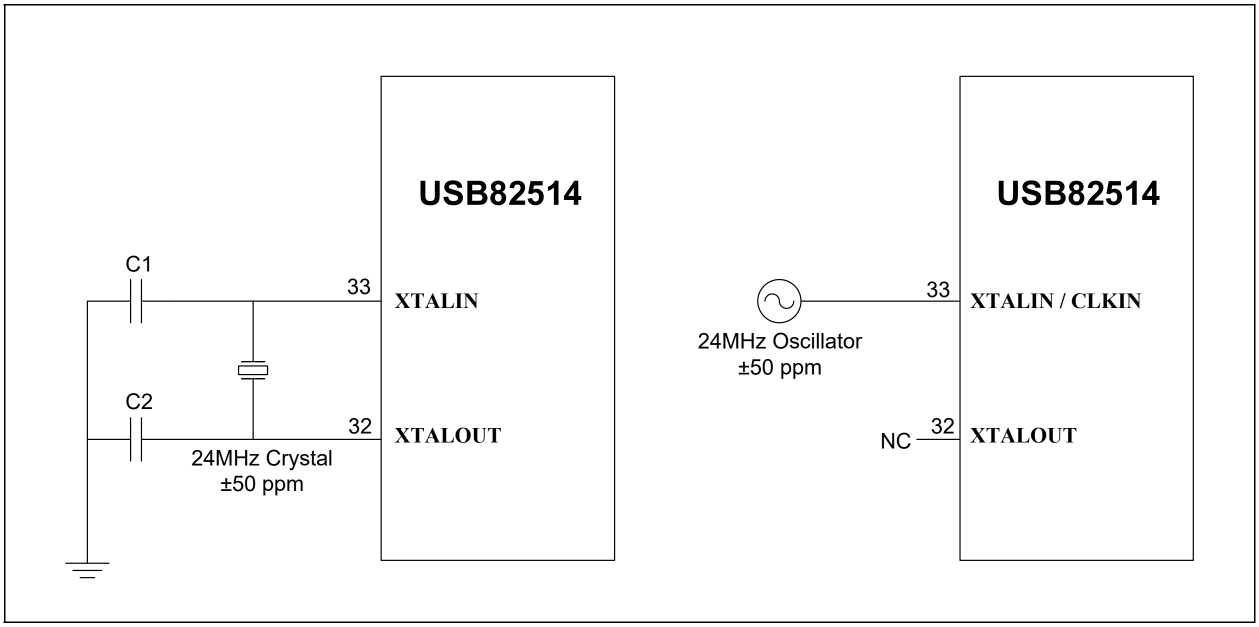
6.1 External Clock Connection

The REFCLK reference clock is the source for the USB interface and for all other functions of the device.

For exact specifications and tolerances, refer to the latest revision of the *USB82514 Data Sheet*.

- **XTALIN/CLKIN** (pin 33) is the crystal/external clock circuit input for the USB82514.
- **XTALOUT** (pin 32) is the clock circuit output for the USB82514. When an external clock source is used to drive **XTALIN/CLKIN**, leave this pin unconnected.

FIGURE 6-1: OSCILLATOR CONNECTIONS



7.0 POWER AND STARTUP

7.1 Board Power Supplies

7.1.1 POWER RISE TIME

The power rail voltage and rise time should adhere to the supply rise time specification as defined in the *USB82514 Data Sheet*.

If a monotonic/fast power rail rise cannot be assured, then the RESET_N signal should be controlled by a reset supervisor and only released when the power rail has reached a stable level.

7.1.2 CURRENT CAPABILITY

It is important to size the 5V and 3.3V power rails appropriately. Please refer to the product data sheet for the power requirements for the specific device. The 5V power supply must be capable of supplying 500 mA (if BC1.2 is not enabled), 1.5A (if BC1.2 is enabled), or up to 2.4A (if certain vendor-specific current negotiation with the USB host is enabled) to the USB downstream port VBUS without dropping below the minimum voltage permissible in the USB Specification.

The 3.3V power supply must be able to supply enough power to the USB hub IC. It is recommend that 3.3V power rail be sized, such that it is able to supply the maximum power consumption specification as displayed in the *USB82514 Data Sheet*.

7.2 Reset Circuit

RESET_N (pin 26) is an active-low reset input. This signal resets all logic and registers within the USB82514. A hardware reset (RESET_N assertion) is not required following power-up. Please refer to the latest copy of the *USB82514 Data Sheet* for reset timing requirements. Figure 7-1 shows a recommended reset circuit for powering up the USB82514 when reset is triggered by the power supply.

FIGURE 7-1: RESET TRIGGERED BY POWER SUPPLY

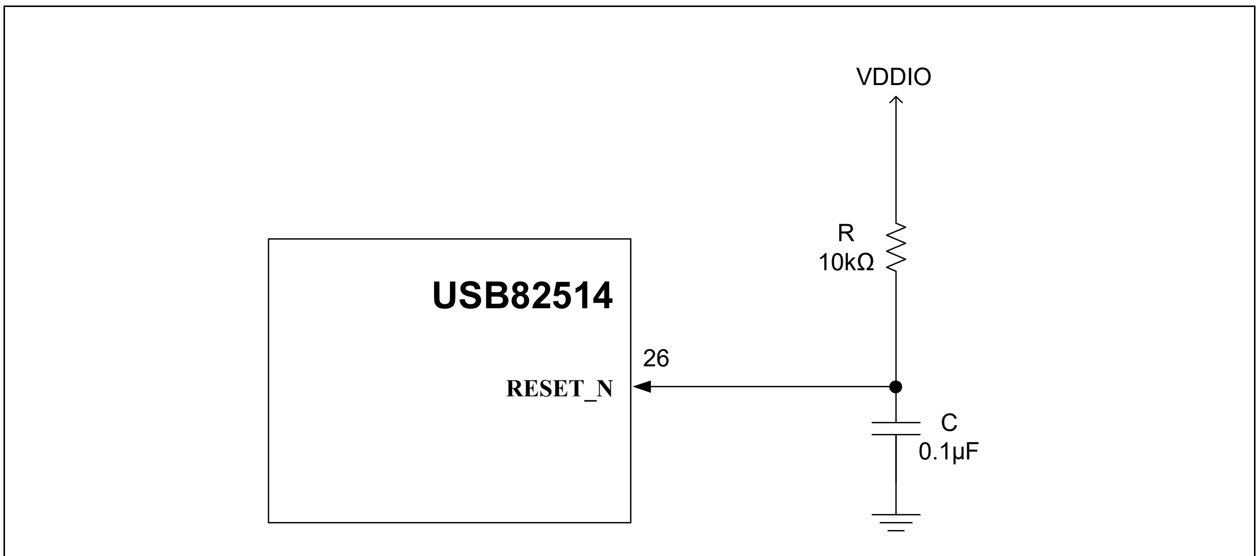
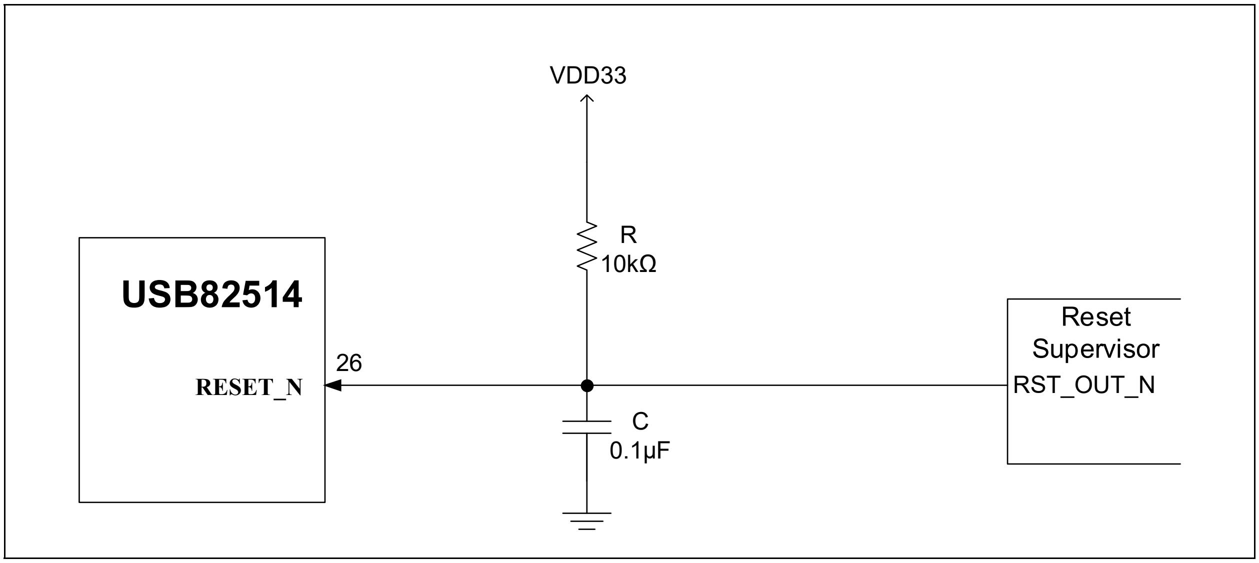


Figure 7-2 details the recommended reset circuit for applications where reset is driven by an external CPU/MCU. The reset out pin (**RST_OUT_N**) from the CPU/MCU provides the warm reset after power-up.

FIGURE 7-2: RESET CIRCUIT INTERFACE WITH CPU/MCU RESET OUTPUT



8.0 MISCELLANEOUS

8.1 Self-Powered/Bus-Powered Settings

In a typical USB82514 application, the hub should be configured as self-powered, which is the default configuration setting.

The following guidelines can be used to determine which setting to use:

- If the entire system (hub included) is powered completely from the Upstream USB connector's **VBUS** pin, and the system is designed to operate using standard USB cabling and any standard USB host, then the hub system is *bus-powered*.
- If the entire system (hub included) is always powered by a separate power connector, then the hub system is *self-powered*.
- If the hub included is part of a larger embedded system with fixed cabling and a fixed USB host, then the hub system is most likely *self-powered* (even if all of the power is derived from the upstream USB connector's **VBUS** pin).

Note: The self-powered/bus-powered device settings do not impact the operation of the hub in any way. The settings only modify select USB descriptors, which the USB host will use to budget power accordingly. Since a standard USB2.0 port is required to supply 500 mA to the downstream port, a self-powered hub and all of its downstream ports must continue to operate within that 500 mA budget. A USB host will typically limit the downstream ports of a bus-powered hub to 100 mA. Any device that connects to a bus-powered hub which declares it needs more than 100 mA will be prevented from operating by the USB host.

9.0 HARDWARE CHECKLIST SUMMARY

TABLE 9-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
	Section 2.3, "USB-IF-Compliant USB Connectors"	If present, verify that USB-IF-compliant USB connectors with an assigned TID are used in the design (if USB compliance is required for the design).		
Section 3.0, "Power"	Section 3.1, "Power and Bypass Capacitance"	• Ensure **VDD33** is in the range 3.0V to 3.6V and has 1.0 µF capacitors on these pins. • Ensure **VDDA33** is in the range 3.0V to 3.6V and has 1.0 µF capacitors on these pins. • Ensure **VDD33PLL** is in the range 3.0V to 3.6V and has a 1.0 µF capacitor on this pin. • Ensure that **VDD18** has a 1.0 µF capacitor on this pin. • Ensure that **VDD18PLL** has a 1.0 µF capacitor on this pin.		
Section 4.0, "USB Signals"	Section 4.1, "USB PHY Interface"	Verify that the USB data pins are correctly routed to the USB connectors. Pay special attention to the polarity of the USB2.0 D+ and D– data lines.		
	Section 4.2, "USB Protection"	Verify that ESD/EMI protection devices are designed specifically for high-speed data applications and that the combined parasitic capacitance the protection devices, USB traces, and USB connector do not exceed 5 pF on each USB trace.		
Section 5.0, "USB Connectors"	Section 5.1, "Upstream Port VBUS and VBUS_DET"	Verify that the upstream port VBUS has no more than 10 µF capacitance and that the VBUS signal is properly divided down to a 3.3V signal and connected to the **VBUS_DET** pin of the hub.		
	Section 5.2, "Downstream Port VBUS and PRTPWR/OCS_N"	Verify that **PRT_CTL** is properly connected to both the Enable pin of the downstream port power controller. Verify that **OCS_N** is properly connected to both the Fault pin of the port power controller.		
	Section 5.3, "GND and EARTH Recommendations"	Verify that the USB connector is properly connected to PCB ground on both the **GND** pins and the **SHIELD** pins. It is recommended that an RC filter be placed between the **SHIELD** pins and PCB ground.		
Section 6.0, "Clock Circuit"	Section 6.1, "External Clock Connection"	Confirm the **REFCLK** input is connected to a positive square wave clock source from 0V to 3.6V.		

TABLE 9-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 7.0, "Power and Startup"	Section 7.1, "Board Power Supplies"	Verify that the board power supplies deliver 3.0V-3.6V to the hub power rails, and that the power-on rise time meets the requirement of the hub as defined in the data sheet. If the rise time requirement cannot be met, ensure that the RESET_N line is held low until the power regulators reach a steady state.		
	Section 7.2, "Reset Circuit"	Ensure that the RESET_N signal has an external pull-up resistor, or is otherwise properly controlled by an external SOC, MCU, or Reset supervisor device.		
Section 8.0, "Miscellaneous"	Section 8.1, "Self-Powered/Bus-Powered Settings"	Verify the application requirements for Self-Powered or Bus-Powered operation. If self-powered operation is required, then no additional configuration or circuitry is required. If bus-powered operation is required, then the hub must be configured via OTP or I^2C/SMBus.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004461A (03-24-22)	Initial release	

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