AN2000

USB to UART Bridging with Microchip USB 3.1 Gen 1 Hubs

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INTRODUCTION

The USB to UART bridging feature of Microchip's USB 3.1 Gen 1 hubs provides system designers expanded system control and potential BOM reductions. When using this feature, a separate USB to UART device is no longer required and a downstream USB port is not lost, as occurs when a standalone USB to UART device is implemented. This feature is available on the Microchip USB5734 USB3.1 Gen 1 Hub, which contains the internal Hub Feature Controller.

Commands may be sent from the USB Host to the internal Hub Feature Controller device in the Microchip hub to perform the following functions:

- Enable/Disable UART Interface
- Set UART Interface Baud Rate
- UART Write
- UART Read

Sections

References

Consult the following documents for details on the specific parts referred to in this document:

- *USB5734 Data Sheet*
- *Microchip AN1903 Configuration Options for the USB5734 and USB5744*

1.0 GENERAL INFORMATION

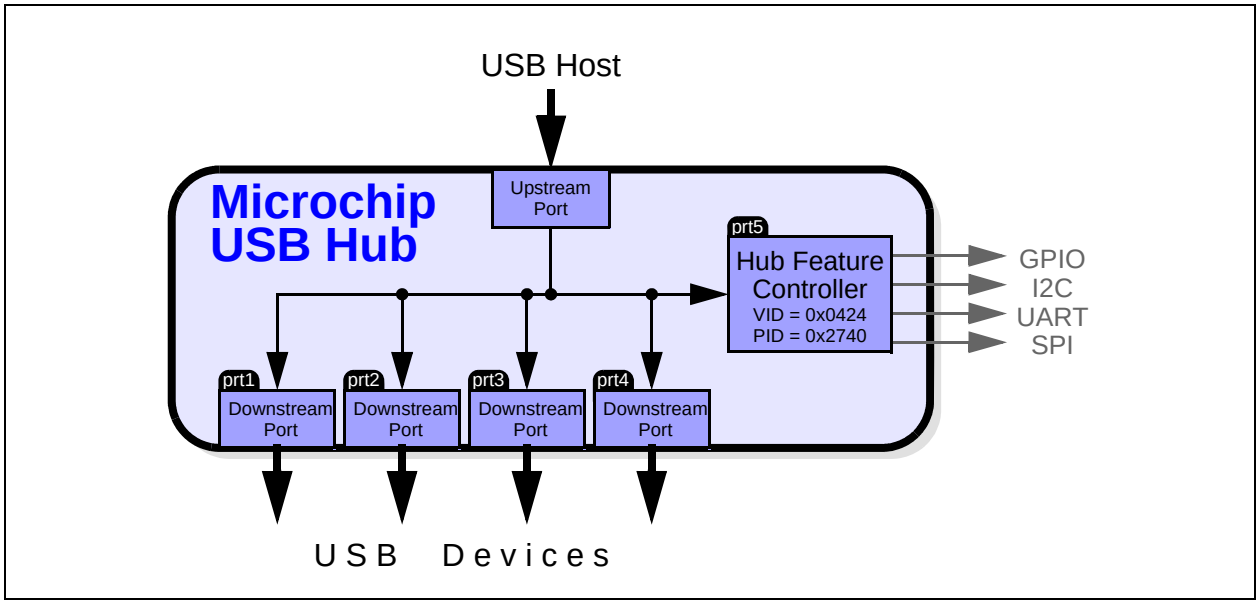
Microchip's USB hub bridging features operate via host commands sent to a Hub Feature Controller embedded within the device, located on an additional internal USB port. In order for the bridging features to work correctly, this internal Hub Feature Controller must be enabled by default. Table 1 provides details on default Hub Feature Controller settings per device.

TABLE 1: DEFAULT SETTINGS FOR HUB FEATURE CONTROLLER ENABLE

Part Number	Part Summary	Hub Feature Controller Default Setting
USB5734	4-Port USB3.1 Gen 1 Hub	Enabled by default

The Hub Feature Controller is connected to an extra internal port in the hub. For example, in a hub with four ports enabled, the Hub Feature Controller is connected to port 5. The Product ID (PID) for the Hub Feature Controller is 0x2740. All bridging commands are addressed to the Hub Feature Controller, not the Hub.

FIGURE 1: MICROCHIP HUB FEATURE CONTROLLER BLOCK DIAGRAM



1.1 UART Bridging Commands

The following UART Functions are supported:

- Enable/Disable UART Pass-Through Interface
- Set UART Baud Rate
- UART Write
- UART Read

1.1.1 ENABLE/DISABLE THE UART INTERFACE

A single command to enable the UART interface is required before performing any UART Write or Read commands. The UART interface has a variable baud rate which can be adjusted via a bridging command. The UART interface may be disabled after writing/reading to the device is complete.

1.1.2 SET UART BAUD RATE

The UART baud rate may adjusted via a bridging command. The suggested standard baud rate values are 600Hz, 1.2kHz, 2.4kHz, 4.8kHz, 9.6kHz, 19.2kHz, 38.4kHz, 57.6kHz, or 115.2kHz.

1.1.3 UART WRITE

Transfer data through the UART serial port to a connected serial peripheral.

1.1.4 UART READ

Synchronously receive data through a serial port from a connected serial peripheral.

1.2 UART Interface Details

1.2.1 UART INTERFACE

The device incorporates a fully programmable, universal asynchronous receiver/transmitter (UART) that is functionally compatible with the NS 16550AF, 16450, 16450 ACE registers and the 16C550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. Two sets of baud rates are provided: 24 Mhz and 16 MHz. When the 24 Mhz source clock is selected, standard baud rates from 50 to 115.2 K are available. When the source clock is 16 MHz, baud rates from 125 K to 1,000 K are available. The character options are programmable for the transmission of data in word lengths of from five to eight, 1 start bit; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is cap able of dividing the input clock or crystal by a number from 1 to 65535. The UART is also capable of supporting the MIDI data rate.

1.2.2 TRANSMIT OPERATION

Transmission is initiated by writing the data to be sent to the TX Holding Register or TX FIFO (if enabled). The data is then transferred to the TX Shift Register together with a start bit and parity and stop bits as determined by settings in the Line Control Register. The bits to be transmitted are then shifted out of the TX Shift Register in the order Start bit, Data bits (LSB first), Parity bit, Stop bit, using the output from the Baud Rate Generator (divided by 16) as the clock.

If enabled, a TX Holding Register Empty interrupt will be generated when the TX Holding Register or the TX FIFO (if enabled) becomes empty.

When FIFOs are enabled (i.e. bit 0 of the FIFO Control Register is set), the UART can store up to 16 bytes of data for transmission at a time. Transmission will continue until the TX FIFO is empty. The FIFO's readiness to accept more data is indicated by interrupt.

1.2.3 RECEIVE OPERATION

Data is sampled into the RX Shift Register using the Receive clock, divided by 16. The Receive clock is provided by the Baud Rate Generator. A filter is used to remove spurious inputs that last for less than two periods of the Receive clock. When the complete word has been clocked into the receiver, the data bits are transferred to the RX Buffer Register or to the RX FIFO (if enabled) to be read by the CPU. (The first bit of the data to be received is placed in bit 0 of this register.) The receiver also checks that the parity bit and stop bits are as specified by the Line Control Register.

If enabled, an RX Data Received interrupt will be generated when the data has been transferred to the RX Buffer Register or, if FIFOs are enabled, when the RX Trigger Level has been reached. Interrupts can also be generated to signal RX FIFO Character Timeout, incorrect parity, a missing stop bit (frame error) or other Line Status errors.

When FIFOs are enabled (i.e. bit 0 of the FIFO Control Register is set), the UART can store up to 16 bytes of received data at a time. Depending on the selected RX Trigger Level, interrupt will go active to indicate that data is available when the RX FIFO contains 1, 4, 8 or 14 bytes of data.

2.0 PART NUMBER SPECIFIC INFORMATION

2.1 Part Summary

The following tables display the UART interface pins by part number as well as any notes on those pins.

2.2 USB5734

TABLE 2: USB5734 UART INTERFACE PINS

Pin #	Name	Notes
42	UART_RX/(SPI_CLK)	UART Receive This pin must not have a pull-down or pull-up resistor present at POR in order to enter UART Mode.
43	UART_TX/(SPI_DO)	UART Transmit This pin must have a 10kΩ pull-down resistor present at POR in order to enter UART Mode.

3.0 PROTOUCH2 DLL IMPLEMENTATION

The simplest method for implementing the USB to UART bridging functions is to use the publicly available DLL which is distributed with the ProTouch2 configuration tool. The DLL is compatible with Windows operating systems. Visit the USB5734 product page on microchip.com to download ProTouch2 with the DLL package. Using the libraries available in the DLL library, the bridging features can be implemented in C-code.

The PT2 DLL library package contains the following:

- User's Manual (Protouch2 DLL User's Guide) with detailed description of how to use the DLL and call each function
- Release notes
- Library Files:
  - For Windows: A ".dll" and a ".lib" file
- Example code

3.1 Commands included in the DLL Library

- **MchpUsbEnableUARTBridging:** Enables or Disables the UART interface.
- **MchpUsbSetUARTBaudrate:** Sets the Baud rate of the interface.
- **MchpUsbUartRead:** Read from a connected serial peripheral.
- **MchpUsbUartWrite:** Write to a connected serial peripheral.

For additional details on how to use the DLL Library to implement USB to UART bridging, download the ProTouch2 package and read the User's Manual.

4.0 MANUAL IMPLEMENTATION

The UART bridge interface automatically appears as a standard serial COM port when the UART interface is enabled via pin strapping (10kΩ pull-down resistor on UART_TX). The USB to UART bridge may be sent commands using the standard COM port drivers that are native to all PCs. No special drivers or USB commands are required. Thus, the USB to UART interface does not require any special software development or the use of the ProTouch2 DLL library.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002000A (09-11-15)	All	Initial release.

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