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Schematic Checklist for the LAN9215, 100-pin LFBGA Package

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Schematic Checklist for LAN9215

Information Particular for the 100-pin LFBGA Package

LAN9215 LFBGA Phy Interface:

1. TPO+ (pin A10); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. TPO- (pin A11); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. TPI+ (pin A8); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. TPI- (pin A9); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD_A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

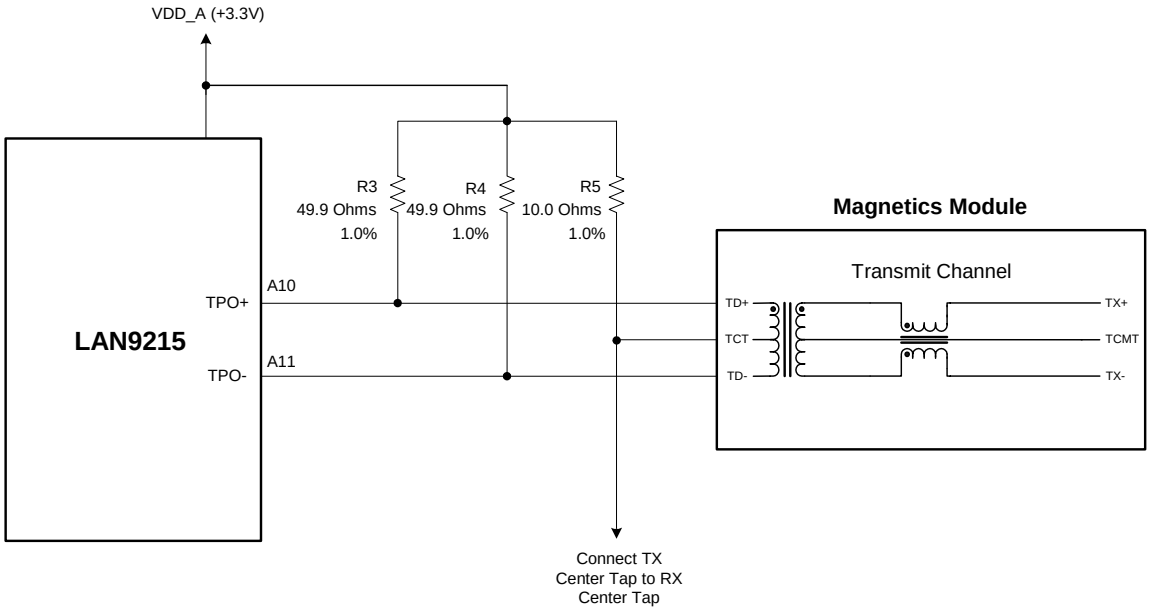

Figure 1 – Transmit Channel Connections and Terminations

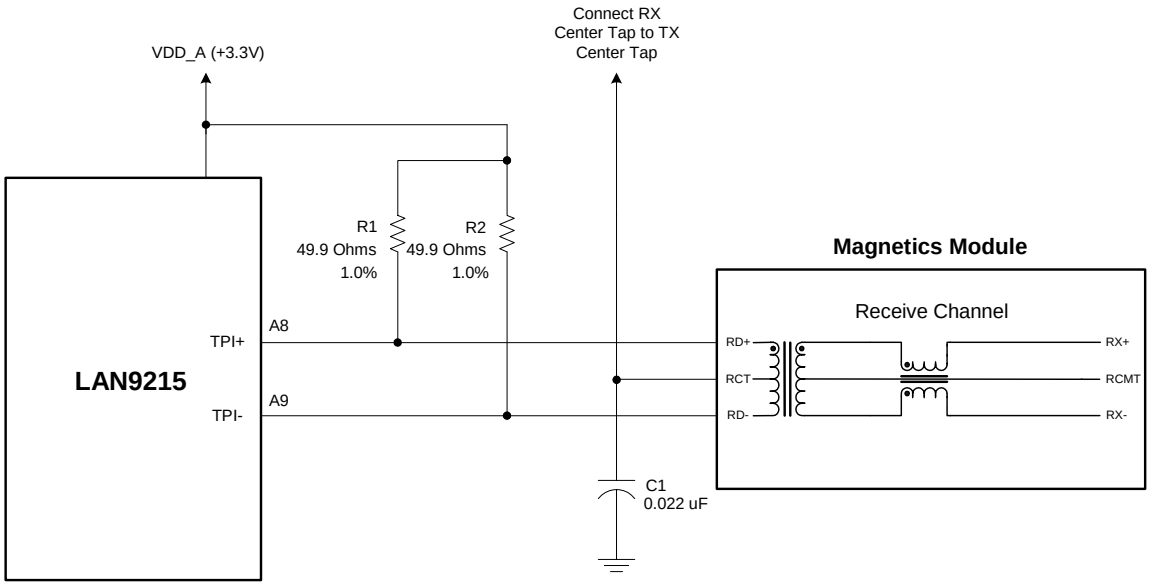

Figure 2 - Receive Channel Connections and Terminations

LAN9215 LFBGA Magnetics:

1. The center tap connection on the LAN9215 side for the transmit channel must be connected to VDD_A (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN9215 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TPO+ (pin A10) of the LAN9215 LFBGA.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TPO- (pin A11) of the LAN9215 LFBGA.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to TPI+ (pin A8) of the LAN9215 LFBGA.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to TPI- (pin A9) of the LAN9215 LFBGA.

10. When using the SMSC LAN921x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

Power Supply Connections:

1. The digital supply (VDD_IO) pins on the LAN9215 LFBGA are B4, B9, C3, C10, D2, D11, J2, J11, K3, K10, L4 & L9. They require a connection to +3.3V.

2. Each power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD_A) pins on the LAN9215 LFBGA are A6, B7 & B10. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD_A pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215. The capacitor size should be SMD_0603 or smaller.

5. Pin A1 (VREG) is a supply voltage for the two separate internal +1.8V regulators. This pin must be connected to +3.3V.

6. The VREG pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215. The capacitor size should be SMD_0603 or smaller.

7. VDD_REF (pin C1), this pin serves as a voltage supply for the internal PLL of the LAN9215. This pin must always be at the same potential as the VDD_IO (+3.3V) power supply pins.

8. The VDD_REF pin should have one .01 μF (or smaller) capacitor to decouple the LAN9215. The capacitor size should be SMD_0603 or smaller.

Ground Connections:

1. The digital ground pins (GND) on the LAN9215 LFBGA are E5, E6, E7, E8, F5, F8, G5, G8, H5, H6, H7 & H8. They need to be connected directly to a solid, contiguous ground plane.

2. We recommend that the Digital Ground pins and the all ground pins be tied together to the same ground plane. We do not recommend running separate ground planes for any of our LAN products.

Voltage Reference Inputs:

1. ATEST (pin D1), this pin serves as a plus voltage reference input to the LAN9215. This pin must always be at the same potential as the VDD_REF pin (pin C1,+3.3V).

VDD_CORE:

1. VDD_CORE (pins D3, D10, J3 & J10), these four pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin D3 requires a bulk capacitor placed as close as possible to pin D3. The bulk capacitor must have a value of at least 10 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD_CORE to VDD_PLL.

Caution: This +1.8V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.

VDD_PLL:

1. VDD_PLL (pin C2), this pin is used to provide an external supply decoupling capacitor to the internal +1.8V PLL regulator. A 0.01 μF decoupling capacitor must be attached to this pin. The capacitor should be located as close as possible to pin C2, and must be attached without using vias. In addition, a bulk capacitor must also be attached to this pin. The bulk capacitor must have a value of at least 10 μF, and must have a very low ESR (equivalent series resistance) of less than 2.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: Even though both are +1.8V levels, **Do Not Connect** VDD_PLL to VDD_CORE.

Caution: This +1.8V supply is for internal logic only. **Do Not** power other circuits or devices with this supply.

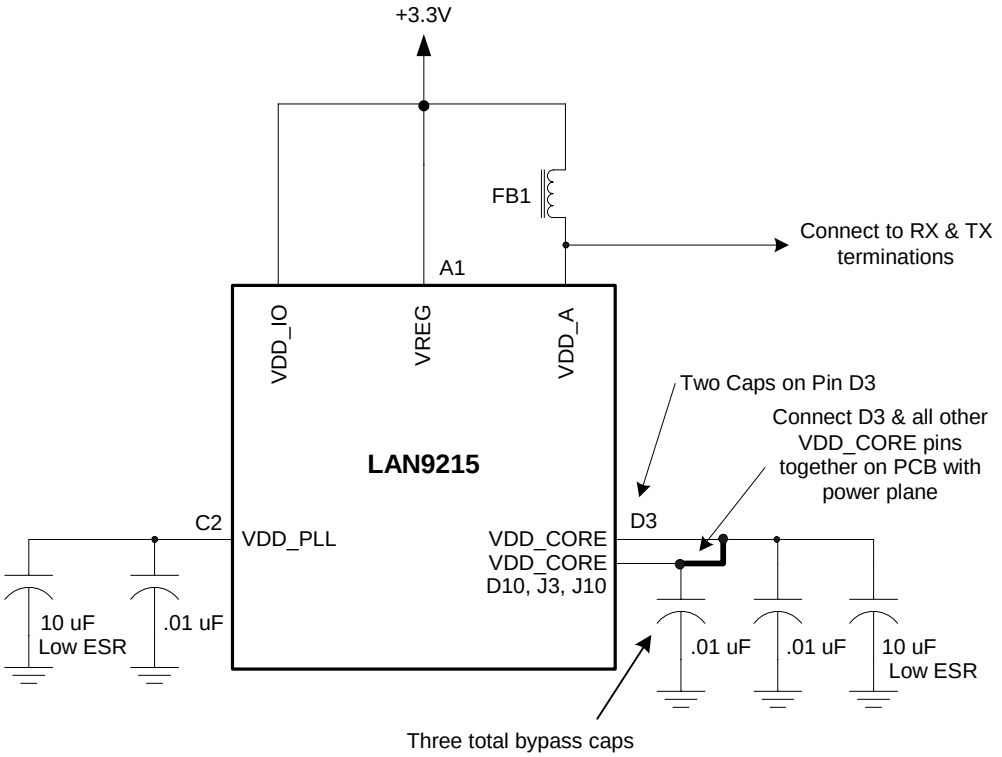

Figure 3 - LAN9215 Power Connections

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN9215 LFBGA. For exact specifications and tolerances refer to the latest revision LAN9215 data sheet.

2. XTAL1 (pin B1) on the LAN9215 LFBGA is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin B2) on the LAN9215 LFBGA is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional 1.0M Ω resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

EEPROM Interface:

1. EECS (pin F11) on the LAN9215 LFBGA connects to the external EEPROM's CS pin.

2. EECLK (pin E12) on the LAN9215 LFBGA connects to the external EEPROM's serial clock pin.

   Caution: To ensure normal device operation, the EECLK pin must be high during any power-up and/or hardware reset event. Do not add any type of external pull-down or grounding connection to this pin as this will result in configuring the device disabled.

3. EEDIO (pin F12) on the LAN9215 LFBGA connects to the external EEPROM's Data In pin. This pin on the LAN9215 is a bi-directional pin and it also connects to the EEPROM's Data Out pin through a 1.0K Ω resistor.

4. Be sure to select a 3-wire style 1K EEPROM that is organized for 128 x 8-bit or the ability to be strapped for 128 x 8-bit operation. Recommended EEPROMs can be found in our LAN9118 Designing with the LAN9118 - Getting Started design guide, application note AN 12.5.

RBIAS Resistor:

1. RBIAS (pin E2) on the LAN9215 LFBGA should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the internal PLL of the LAN9215.

EXRES1 Resistor:

1. EXRES1 (pin A7) on the LAN9215 LFBGA should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

MII Interface:

1. When utilizing either an external MII Phy or an MII Connector, the following table indicates the proper connections for the 17 signals.

From:	Connects To:	
LAN9215 LFBGA	**MII Physical Device**	**MII Connector**
RXD0 (pin B11)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin K1)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin K2)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin L1)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin M2)	RX_DV	RX_DV (contact 8)
RX_ER (pin L2)	RX_ER	RX_ER (contact 10)
RX_CLK (pin M1)	RX_CLK	RX_CLK (contact 9)
TXD0 (pin M7)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin M6)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin L6)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin M5)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin J1)	TX_EN	TX_EN (contact 13)
TX_CLK (pin L7)	TX_CLK	TX_CLK (contact 12)
CRS (pin M4)	CRS	CRS (contact 19)
COL (pin L5)	COL	COL (contact 18)
MDIO (pin L3)	MDIO	MDIO (contact 2)
MDC (pin M3)	MDC	MDC (contact 3)

2. If the MII interface is not used by the system, do not terminate on the board level. These pins have the proper internal terminations and should be left as no-connects.

Required External Pull-ups/Pull-downs:

1. IRQ (pin C12) may require an external pull-up resistor if this output is programmed as an Open Drain type.

2. PME (pin E11) may require an external pull-up resistor if this output is programmed as an Open Drain type.

3. GPIO0/nLED1 (pin A3) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates what speed (10/100) the Ethernet phy is currently set for. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output.

4. GPIO1/nLED2 (pin B3) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates Link & Activity status of the Ethernet phy. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output.

5. GPIO2/nLED3 (pin A2) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates what duplex mode (half/full) the Ethernet phy is currently set for. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output.

6. When using the MII interface of the LAN9215 LFBGA with an external Physical device on board, a pull-up resistor on the signal MDIO must be incorporated. A pull-up resistor of 1.5KΩ to +5V/+3.3V is required for this application. If the LAN9215 LFBGA is used with the industry standard MII connector, the 1.5KΩ is not required as this pull-up will be on the plug-in MII PCB.

7. RXD0 (pin B11) must be pulled or driven to a valid state at all times. An external 10KΩ pull-down resistor is required on this pin.

CPU Interface:

1. A1 – A7 Address Bus: Please refer to the latest revision of the LAN9215 Application Note for exact implementation of the CPU interface selected.

2. D0 – D15 Data Bus: Please refer to the latest revision of the LAN9215 Application Note for exact implementation of the CPU interface selected.

3. Control Signals: Please refer to the latest revision of the LAN9215 Application Note for exact implementation of the CPU interface selected.

4. The LAN9215 is a Little Endian LAN device. It is the designers' responsibility to ensure that the selected CPU has compatible Endianess, as this may affect Data Bus connections to the LAN9215. For example, if a Big Endian processor is used in conjunction with the LAN9215, it may be necessary to swap data bus byte lanes in order to ensure proper system operation. Please refer to the latest LAN9215 data sheet and design guides to determine compatibility.

Miscellaneous:

1. There are two No-Connect pins on the LAN9215. It is very important that these pins remain as no-connects. These pins are B8 & D12.

2. SPEED_SEL (pin B12), upon deassertion of reset, the Default Ethernet Settings are established.

   If this pin is high, the LAN9215 will default to 100BASE-TX, Half Duplex mode with Auto Negotiation enabled. This pin has a weak internal pull-up resistor, so, for this mode, this pin can be left as a no-connect.

   With this pin low, the default setting will be 10BASE-T, Half Duplex with Auto Negotiation disabled. A 1.0K Ω pull-down resistor should be used for this purpose.

3. FIFO_SEL (pin A12), when driven high, all accesses to the LAN9215 are to the RX or TX Data FIFOs. In this mode, the address input is ignored. Typical use will involve connecting an upper address line (A11 is recommended) to this pin to determine functionality. For normal operation (FIFO_SEL disabled), a 1.0K Ω external pull-down resistor must be attached to this pin.

4. MDIO / External Phy Detect (pin L3), this pin is used as a strap to indicate the presence of an external phy. The level of this pin is latched upon power-up or hard reset. This pin has no effect on the internal logic of the LAN9215. It is only intended to provide a mechanism to the system designer to inform the software application that an external phy is present. The MII functionality (enable & disable) is completely register based. See the LAN9215 Data Sheet, HW_CFG – Hardware Configuration Register, Bit 3 for specific details.

5. nRESET (pin A4), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9215. This signal is pulled high with a weak internal pull-up resistor. If nRESET is left unconnected the LAN9215 will rely on its internal power-on reset circuitry.

6. AMDIX_EN (pin C11), this pin enables the HP Auto MDIX feature of the LAN9215. To take advantage of the Auto MDIX feature (Auto MDIX enabled), a 1.0K Ω external pull-up resistor must be attached to this pin. This pin has a weak internal pull-down, so this pin can be left as a no-connection in order to disable the Auto MDIX feature (default mode of operation).

7. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

8. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

LAN9215 LFBGA QuickCheck Pinout Table:

Use the following table to check the LAN9215 LFBGA shape in your schematic.

LAN9215 LFBGA							
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	VREG	C2	VDD_PLL	G1	A4	K12	D5
A2	nLED3	C3	VDD_IO	G2	A3	L1	RXD3
A3	nLED1	C10	VDD_IO	G5	GND	L2	RX_ER
A4	nRESET	C11	AMDIX_EN	G8	GND	L3	MDIO
A5	nWR	C12	IRQ	G11	D1	L4	VDD_IO
A6	VDD_A	D1	ATEST	G12	D0	L5	COL
A7	EXRES1	D2	VDD_IO	H1	A2	L6	TXD2
A8	TPI+	D3	VDD_CORE	H2	A1	L7	TX_CLK
A9	TPI-	D10	VDD_CORE	H5	GND	L8	D14
A10	TPO+	D11	VDD_IO	H6	GND	L9	VDD_IO
A11	TPO-	D12	NC2	H7	GND	L10	D11
A12	FIFO_SEL	E1	A7	H8	GND	L11	D8
B1	XTAL1	E2	RBIAS	H11	D3	L12	D7
B2	XTAL2	E5	GND	H12	D2	M1	RX_CLK
B3	nLED2	E6	GND	J1	TX_EN	M2	RX_DV
B4	VDD_IO	E7	GND	J2	VDD_IO	M3	MDC
B5	nCS	E8	GND	J3	VDD_CORE	M4	CRS
B6	nRD	E11	PME	J10	VDD_CORE	M5	TXD3
B7	VDD_A	E12	EECLK	J11	VDD_IO	M6	TXD1
B8	NC1	F1	A5	J12	D4	M7	TXD0
B9	VDD_IO	F2	A6	K1	RXD1	M8	D15
B10	VDD_A	F5	GND	K2	RXD2	M9	D13
B11	RXD0	F8	GND	K3	VDD_IO	M10	D12
B12	SPEED_SEL	F11	EECS	K10	VDD_IO	M11	D10
C1	VDD_REF	F12	EEDIO	K11	D6	M12	D9

Notes:

Reference Material:

1. SMSC LAN9215 Data Sheet; check web site for latest revision.

2. SMSC LAN9215 EVB Schematic, Assembly No. xxxx ; check web site for latest revision.

3. SMSC LAN9215 EVB PCB, Assembly No. xxxx ; order PCB from web site.

4. SMSC LAN9215 EVB PCB Bill of Materials, Assembly No. xxxx ; check web site for latest revision.

5. SMSC LAN9118 Design Guide, Designing with the LAN9118I – Getting Started, Application Note AN 12.5; check web site for latest revision.

6. SMSC LAN9118 Programmers Reference Guide, Application Note AN 12.12; check web site for latest revision.

7. Migrating from the LAN9118 to the LAN9218I, Application Note AN 14.10; check web site for latest revision.

8. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.