ENT-AN1170 Application Note
Using Start of Frame Indications in the VSC8541 Gigabit Ethernet Copper PHY

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VPPD- 04179. 1.0 5/16

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Application Note

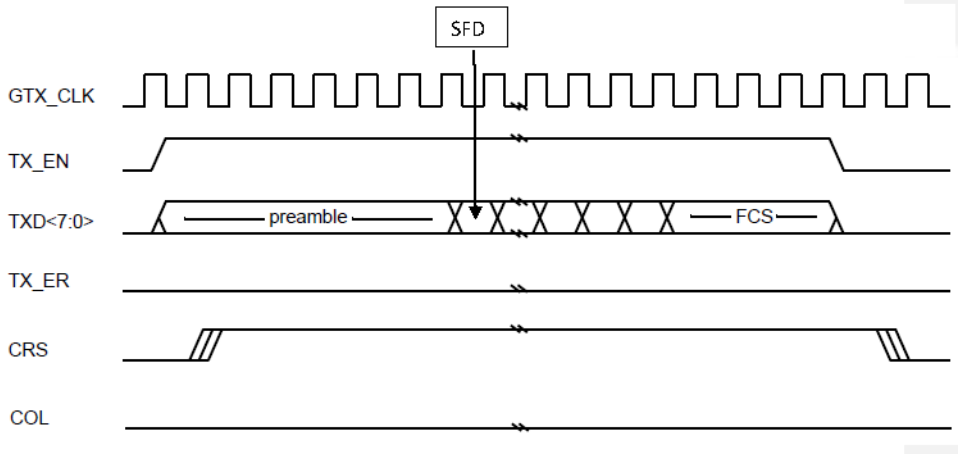
The VSC8541 Gigabit Ethernet Copper (Cu) PHY can output a pulse indication of the actual time that the Start of Frame Delimiter (SFD) is processed inside the Physical Coding Sublayer (PCS). With appropriate compensation, this provides an accurate indication of packet arrival at the Medium Dependent Interface (MDI) of the Cu PHY suitable for IEEE 1588 Precision Time Protocol (PTP) applications. A PTP host can use this pulse for a system-level time stamp reference point in processing PTP packets. This Start of Frame (SOF) indication affords improved variability for host time stamp generation when compared to time stamping packets inside the Ethernet MAC, at a modest increase to PTP system complexity.

2.1 SOF Indication: Ethernet Frame Format and the SFD

An IEEE 802.3 Ethernet data stream begins with a preamble, which is followed by the SFD, the MAC destination address, MAC source address, and other information. The SFD consists of an octet of 0xD5, which indicates the start of a frame at the logical interface between a media access controller (MAC) and physical-signal processor (PHY).

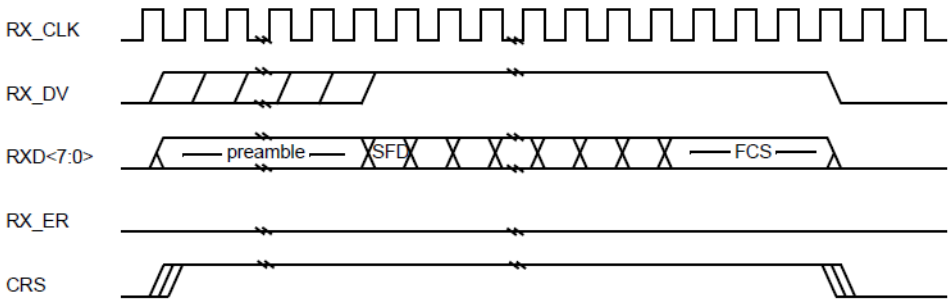
The following figure shows the SFD at the GMII boundary between a gigabit Ethernet MAC and PHY during frame transmission.

Figure 1 • **SFD at the GMII Boundary**



The following figure shows the SFD at frame reception.

Figure 2 • **SFD at Frame Reception**



Thus, the SFD is an intuitive reference point for time stamping Ethernet packets that provide synchronization services such as IEEE 1588.

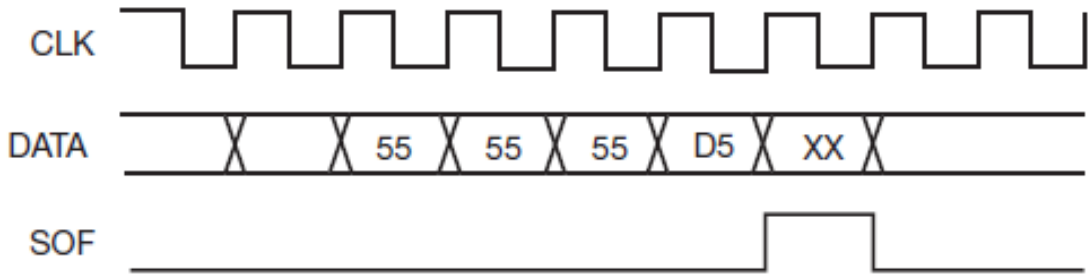
2.2 SOF Delimiter Processing in VSC8541

The VSC8541 device generates a pulse when the SFD octet 0xD5 is processed by the PCS engine. The pulse is generated on the MAC-PHY electrical interface and indicates the actual time the SFD symbol is received at the PCS inside the VSC8541 device. There is a fixed timing relationship from the time the SFD arrives inside the PCS relative to its appearance on the CAT5 wire in the receive or transmit direction.

In contrast, the SFD appearance on the CAT5 wire varies with respect to the TX_EN/RX_DV signals (as shown in Figure 1, page 2) and results in per-packet delay variation because the GTX_CLK and RX_CLK signals are not phase-aligned with the PHY's MDI clock. Use of the SOF signal as a packet time stamping reference avoids variability in timing between the GMII to the PCS due to clock domain crossings.

The SOF pulse is generated in both transmit and receive directions, along with associated clocks from the PCS, to the GMII pins as shown in the following figure.

Figure 3 • **SOF Indication**



2.3 Signal Interface Description and Configuration

The signals are multiplexed onto the most-significant GMII data bit pins, and are only available when the VSC8541 device is configured for a reduced GMII MAC mode.

The following table provides the pin description of the multiplexed SOF indication function.

Table 1 • **SOF Indication**

Pin	Signal
RXD7	RX_SOF
RXD6	RX_SOF_CLK
RXD5	TX_SOF
RXD4	TX_SOF_CLK

To enable SOF functionality (assuming the PHY is in non-GMII MAC interface mode), set register bit 20E2.12 to 1.