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PCB Layout Guide for MEC170x

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INTRODUCTION

This application note provides information on design considerations for a printed circuit board (PCB) for the Microchip MEC170x device.

The design of the PCB requires care to provide good supply and ground paths; in addition, other design issues are addressed in this document.

The functional blocks in the MEC170x have different requirements for routing and external connections, which are also outlined in this application note.

Please see References for device-level information such as VTR power planes, and mechanical package information for the 144-Pin WFBGA, 169-Pin WFBGA and 169-Pin XFBGA.

This document includes the following topics:

Audience

This document is written for a reader that is familiar with hardware design. The goal of this application note is to provide information about sensitive areas of the MEC170x PCB layout.

References

The following documents should be referenced when using this application note. Please contact your Microchip representative for availability.

- Microchip MEC170x Data Sheet
- Microchip MEC170x EVBs, TBD
- PCI Local Bus Specification (see www.pcisig.com)
- I^2C-bus specification and user manual, Rev. 6 - 4 April, 2014 or later (see www.nxp.com/documents/user_manual/UM10204.pdf)
- Intel, Enhanced Serial Peripheral Interface (eSPI) Specification (for Client Platform)
- Microchip “eSPI Controller” Specification

Package Information

The MEC170x device is currently available in the following package:

- MEC170x for 144-pin, WFBGA
- MEC170x for 169-pin, WFBGA
- MEC170x for 169-pin, XFBGA

1.0 GENERAL LAYOUT CONSIDERATIONS

This section describes layout considerations for the MEC170x device. This includes the following topics:

1.1 Decoupling Capacitors

This section includes the following topics:

Decoupling capacitors should be placed as close to the chip as possible to keep series inductance low. When the capacitors are mounted on the bottom side of the PCB, the capacitors are connected to the ground plane from the bottom layer directly using the shortest path to the device. Each VTR pin should have a 0.1 μF capacitor located as close to the pin as possible. Bypass capacitors should be placed close to the supply pins of the MEC170x with short and wide traces.

The MEC170x has an integrated voltage regulator to supply the core circuitry. Decoupling this regulator requires a critical capacitor of 1μF on the CAP pin. ESR of this 1μF capacitor, including the routing resistance, must be less than 100 mOhm.

Capacitors may carry large currents that generate magnetic fields, inducing noise on nearby traces. Sensitive traces such as the 32kHz crystal should be separated by at least five times the trace width from decoupling capacitors when possible.

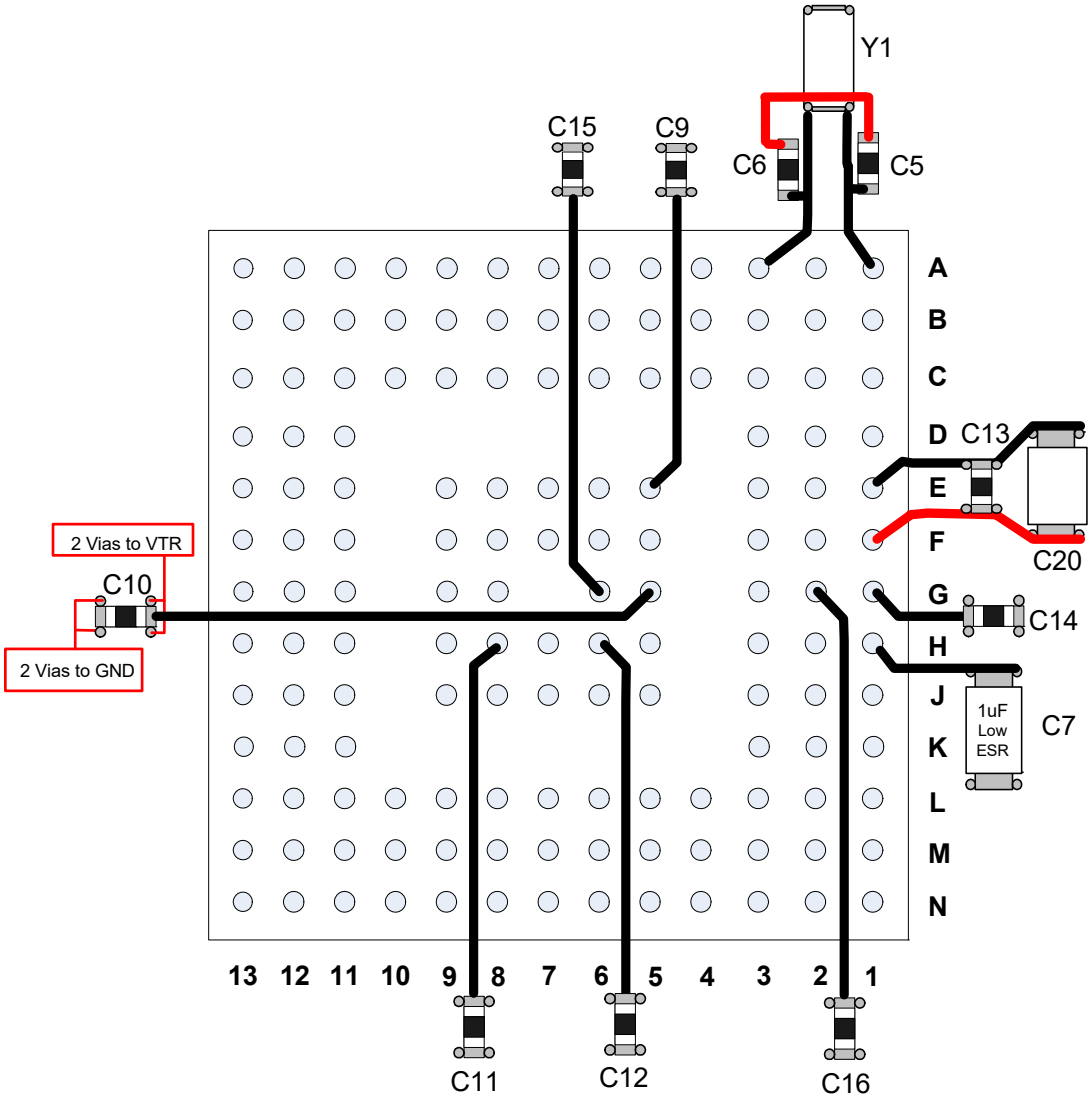
Connecting decoupling caps to power and ground planes using two vias per pad will reduce series inductance.

1.1.1 MEC170X 144 PIN WFBGA CAPACITORS

- Figure 1-1 shows decoupling for the MEC170x 144-pin WFBGA package.

Note:	The capacitors can use any typical 16V 10% ceramic.

FIGURE 1-1: MEC170X DECOUPLING IN 144-PIN WFBGA PACKAGE



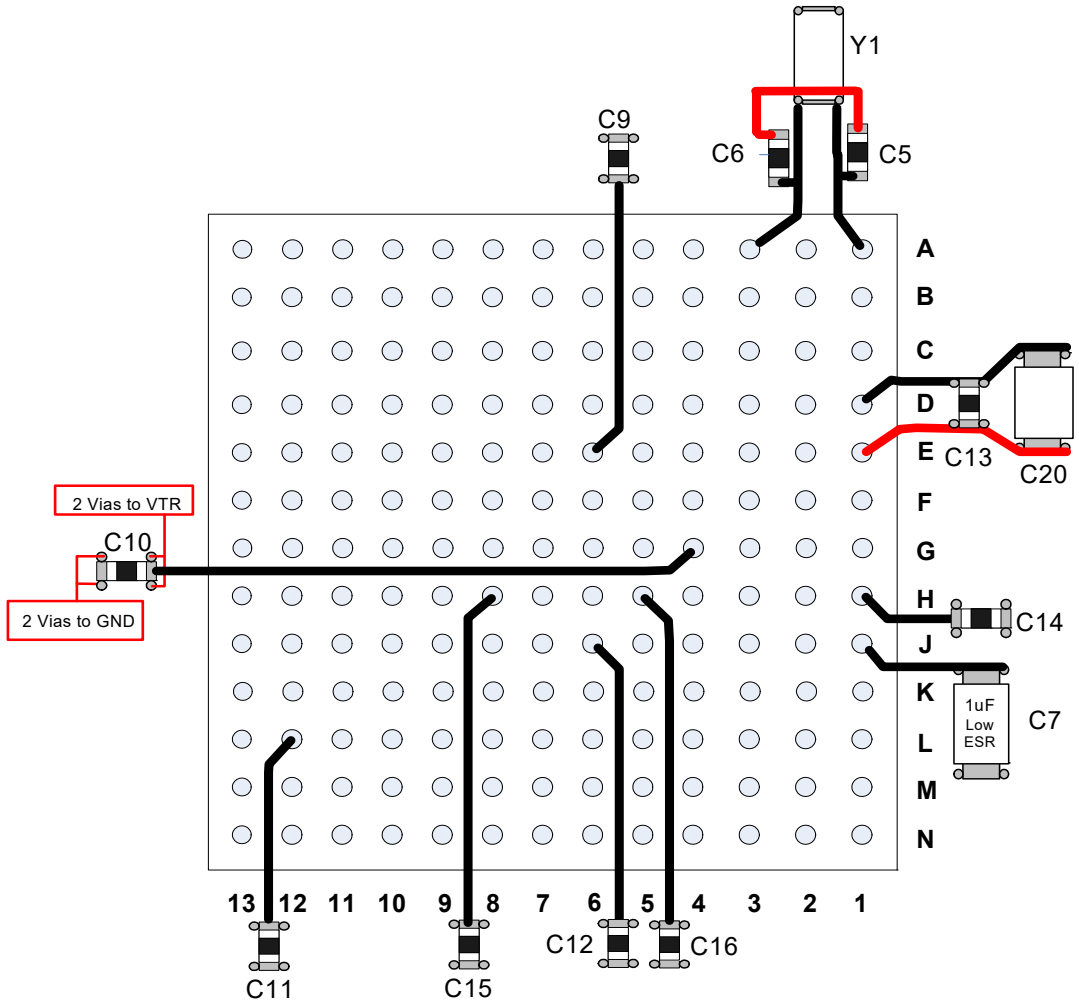
MEC170x 144 Pin WFBGA (Bottom View)
Note: (For Part Numbers see MEC170x DC Schematic)
C9 = 0.1uF on VBAT
C10 = 0.1uF on VTR1
C11 = 0.1uF on VTR2
C12 = 0.1uF on VTR3
C14 = 0.1uF on VTR_REG
C15 = 0.1uF on VTR_ANALOG
C16 = 0.1uF on VREF_ADC
C13 = 0.1uF & C20 = 22uF between VTR_PLL & VFLT_PLL
C7 = 1uF Low ESR +/-20% <100 mOhm on CAP (X5R or X7R)
Y1 = 9pF load crystal, C5/C6 are 10pF

1.1.2 MEC170X 169 PIN WFBGA CAPACITORS

- Figure 1-2 shows decoupling for the MEC170x 169-pin WFBGA package.

Note:	The capacitors can use any typical 16V 10% ceramic.

FIGURE 1-2: MEC170X DECOUPLING IN 169-PIN WFBGA PACKAGE



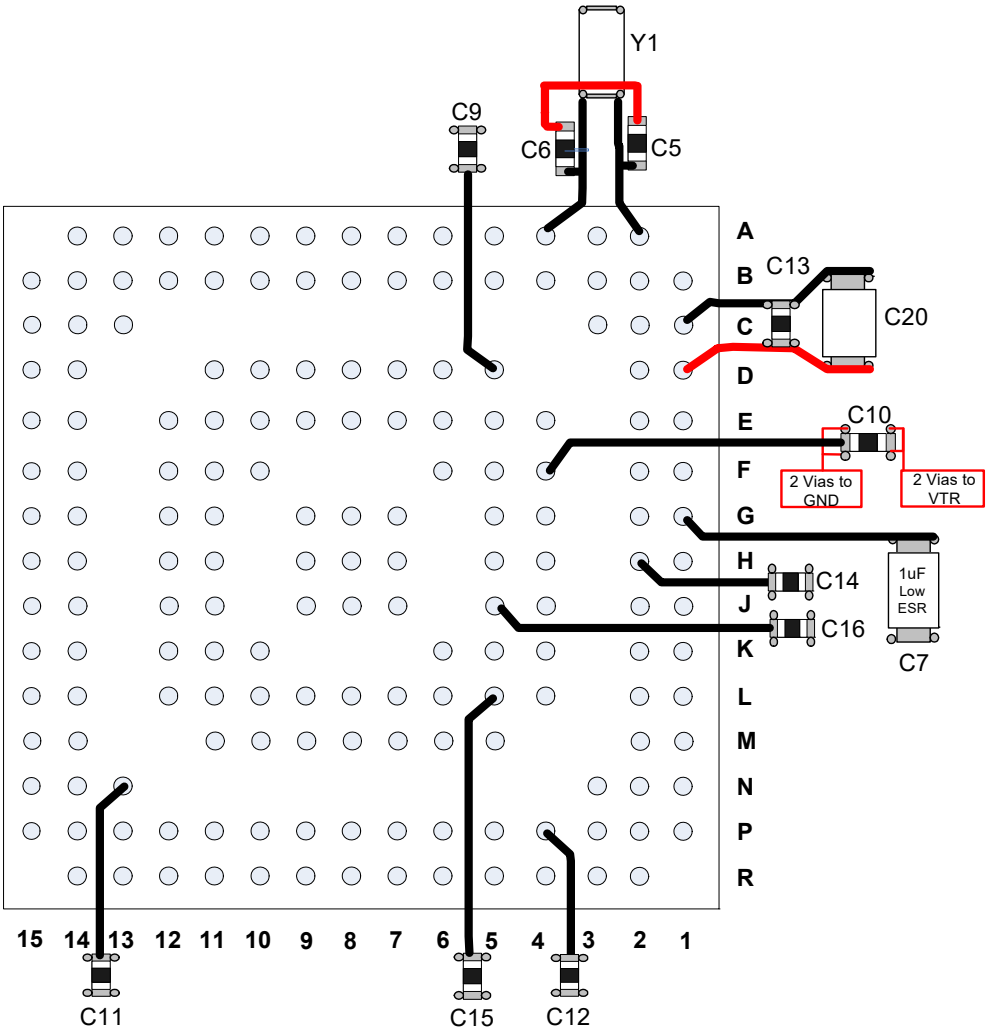
MEC170x 169 Pin WFBGA (Bottom View)
Note: (For Part Numbers see MEC170x DC Schematic)
C9 = 0.1uF on VBAT
C10 = 0.1uF on VTR1
C11 = 0.1uF on VTR2
C12 = 0.1uF on VTR3
C14 = 0.1uF on VTR_REG
C15 = 0.1uF on VTR_ANALOG
C16 = 0.1uF on VREF_ADC
C13 = 0.1uF & C20 = 22uF between VTR_PLL & VFLT_PLL
C7 = 1uF Low ESR +/-20% <100 mOhm on CAP (X5R or X7R)
Y1 = 9pF load crystal, C5/C6 are 10pF

1.1.3 MEC170X 169 PIN XFBGA CAPACITORS

- Figure 1-3 shows decoupling for the MEC170x 169-pin XFBGA package.

Note:	The capacitors can use any typical 16V 10% ceramic.

FIGURE 1-3: MEC170X DECOUPLING IN 169-PIN XFBGA PACKAGE



MEC170x 169 Pin XFBGA (Bottom View)
Note: (For Part Numbers see MEC170x DC Schematic)
C9 = 0.1uF on VBAT
C10 = 0.1uF on VTR1
C11 = 0.1uF on VTR2
C12 = 0.1uF on VTR3
C14 = 0.1uF on VTR_REG
C15 = 0.1uF on VTR_ANALOG
C16 = 0.1uF on VREF_ADC
C13 = 0.1uF & C20 = 22uF between VTR_PLL & VFLT_PLL
C7 = 1uF Low ESR +/-20% <100 mOhm on CAP (X5R or X7R)
Y1 = 9pF load crystal, C5/C6 are 10pF

1.2 32.768kHz Crystal Oscillator

This section describes specific layout and design considerations for the 32.768kHz crystal oscillator; this can be used to source the internal 32kHz clock domain, in lieu of the silicon oscillator or an external pin. The crystal implementation is required to support the RTC function within the MEC170x.

1.2.1 32.768KHZ CRYSTAL OSCILLATOR LAYOUT

The MEC170x 32kHz crystal oscillator is designed to generate a synchronous on-chip clock signal with an appropriate external oscillator crystal. The design has been optimized for low power (1.5 µW typical), stability and minimum jitter using a general purpose parallel resonant 32kHz crystal. For a suggested part number, please see the MEC170x EVB schematic (see References).

This unique low power crystal oscillator drive circuit means that a standard inverter crystal layout should not be used. The design has been characterized to allow a variation of 4pF to 18pF on each pin. Based on the following load capacitance calculation, Microchip recommends 10pf load capacitors with a crystal that has a 9pf Cl rating. Other than these capacitors, no additional external components are required for normal operation of the clock circuit.

$$Effective\ Load\ Capacitance = C1 = \frac{[C11 + Cpin\_xtal2][C12 + Cpin\_xtal1]}{C11 + Cpin\_xtal2 + C12 + Cpin\_xtal1} + Cbrd$$

Where:

- C12 is the cap from pin XTAL1 to ground.
- C13 is the cap from pin XTAL2 to ground.
- Cpin_xtal2 is the pin capacitance of pin XTAL2. This is estimated to be 5pf (Note 1-1).
- Cpin_xtal1 is the pin capacitance of pin XTAL1. This is estimated to be 3pf (Note 1-1).
- Cbrd is estimated at 1.5pF.

Note 1-1 At the time of publication, the MEC170x silicon has not been characterized. Please check with your Microchip FAE for final pin capacitance values after silicon validation is complete. Any variation from the estimates provided here could change the crystal Cl value requirement.

1.2.2 CRYSTAL ACCURACY

The accuracy of the 32kHz input translates directly into accuracy of the internal clock and the functions in the MEC170x using the 32kHz: 32KHZ_OUT, week timer, hibernation timers, and so forth.

The accuracy, with regard to actual error in time can be illustrated as such: +/-1ppm of error in frequency corresponds to 32.768 kHz x 1ppm x 10^{-6} = +/-0.032768 Hz. This translates into ~1 µsec/sec or ~+/-0.086 sec/day.

Based on customer RTC accuracy timer requirements, Microchip recommends using a +/-20ppm crystal. This would equal approximately +/-2 sec/day, other factors discounted.

For arguments sake, it is safe to say that stray capacitance is difficult to calculate exactly. So, as an exercise in completeness, this calculation describes the effect of each picofarad of additional capacitance over/under the crystal C_{load} value:

$$ppm/pF = \frac{C_1\ x\ 10^6}{2(C_O + C_L)^2}$$

where C_0 is the shunt capacitance, C_1 is the motional capacitance and C_L is the load capacitance of the chosen crystal (these numbers can be found in the crystal data sheet). For example, using a crystal with C_0 = 0.8pF, C_1 = 0.0019pF, C_L = 12.5pF, we get a shift of 5.37ppm/pF. So, in terms of time, each pF of added/subtracted capacitance is approximately 5.37 x 0.086 = +/-462 msec/day for this particular crystal.

This example is meant to illustrate the magnitude of the potential error. In practice, slight capacitance mismatch does not equate to many seconds a day.

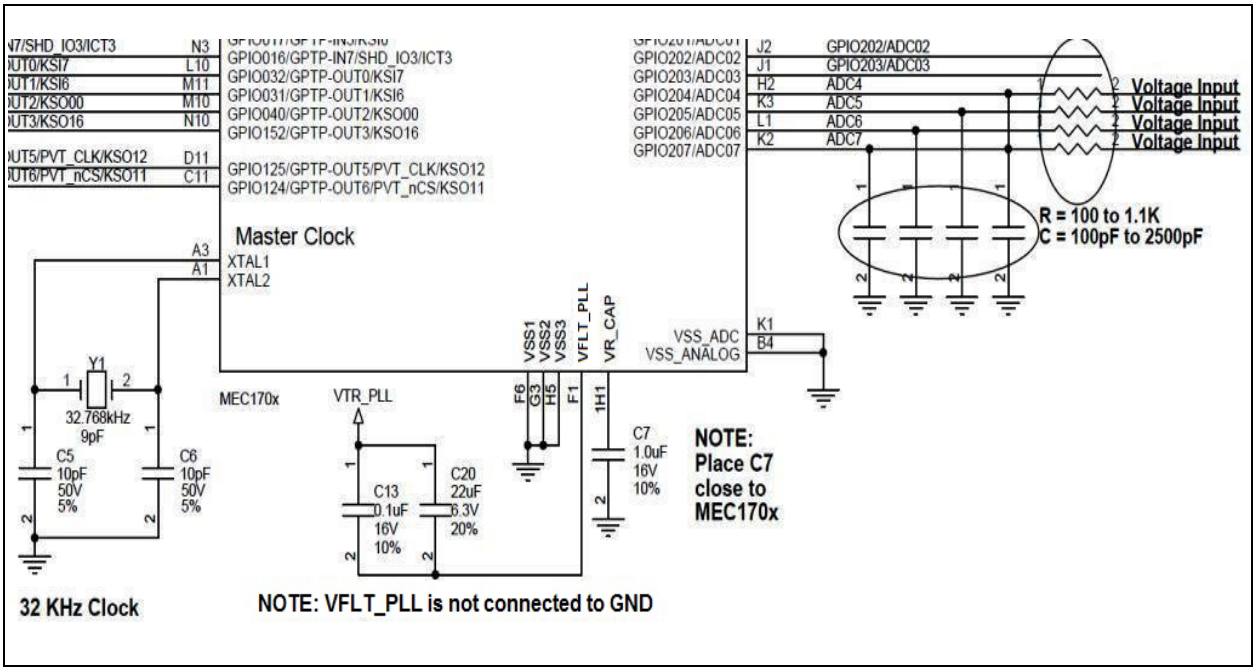
1.2.3 SINGLE ENDED CLOCKING

An external clock source (maximum voltage of 3.3V) may be applied to the XTAL2 pin if the XOSEL bit in Clock Enable Register configures as a single-ended 32.768 kHz clock input (SUSCLK). The XTAL1 pin should be left floating. If an external clock source is used, the designer must ensure that the source is available in all desired power states in which the EC will be active.

1.3 CAP Pins, AVSS/GND Connection

The recommended filtering for the CAP pin on the MEC170x is shown in Figure 1-4, for WFBGA connections. The filtering components shown should be placed close to the device and away from noise sources.

FIGURE 1-4: 144 WFBGA CAP PIN REFERENCE AND AVSS DIRECTLY CONNECTED TO GND



1.4 PCB Mounted Analog Power Supply Filter for PLL Usage

To achieve a reasonable level of long term jitter, it is vital to deliver an analog-grade power supply to the PLL.Typically an R-C or R-L-C filter is usually used, with the "C" being composed of multiple devices to achieve a wide spectrum of noise absorption. Although the circuit is simple, there are specific board layout requirements if it is to work at all.

The series resistance of this filter is limited for DC reasons; generally we like to see <<5% voltage drop across this device under worst-case conditions. High quality series inductors should not be used without a series resistor lest a high gain series resonator is created.

To achieve good low-frequency cut off there should be an electrolytic capacitor in the filter design. As the filter also needs to sustain its attenuation into moderately high frequencies, so there will additionally be at least one non-electrolytic capacitor in parallel. The leads of the high frequency capacitor(s) must be kept short. In some applications the electrolytic capacitor is not required, but it is better to have a space for in on the board which you later leave vacant, rather than have a jittering PLL and no-where to put the cap. Cursory analysis suggests that a third, very high frequency, capacitor should help reduce noise – but experimental data has not shown any jitter benefit in real applications.

Board layout around the high-frequency capacitor and the path from there to the pads is critical. It is vital that the quiet ground and power are treated like analog signals.

The power (VDD) path must be a single wire from the IC package pin to the high frequency cap, then to the low frequency cap, and then through the series element (e.g. resistor) then to board power (VDD). The distance from the IC pin to the high frequency cap should be as short as possible.

Similarly, the ground (VSS) path should be from the IC pin to the high frequency cap, to the low frequency cap, with the distance from IC pin to high frequency cap being very short. Modern PLLs will have the DC ground connection made on chip, so the external ground connection must not be connected to PCB ground. With some older designs, where the DC ground connection is not on-chip, a trace would be run from the low frequency cap to board ground, near the VDD connection – be aware of this difference if converting an old board design.

In all applications, **the power and ground traces should be short, and run close and parallel** as far as is possible, with large spacing to adjacent traces. **On no account should any connection be made from VDD or VFLT_PLL to board power planes**; only connect as described above.

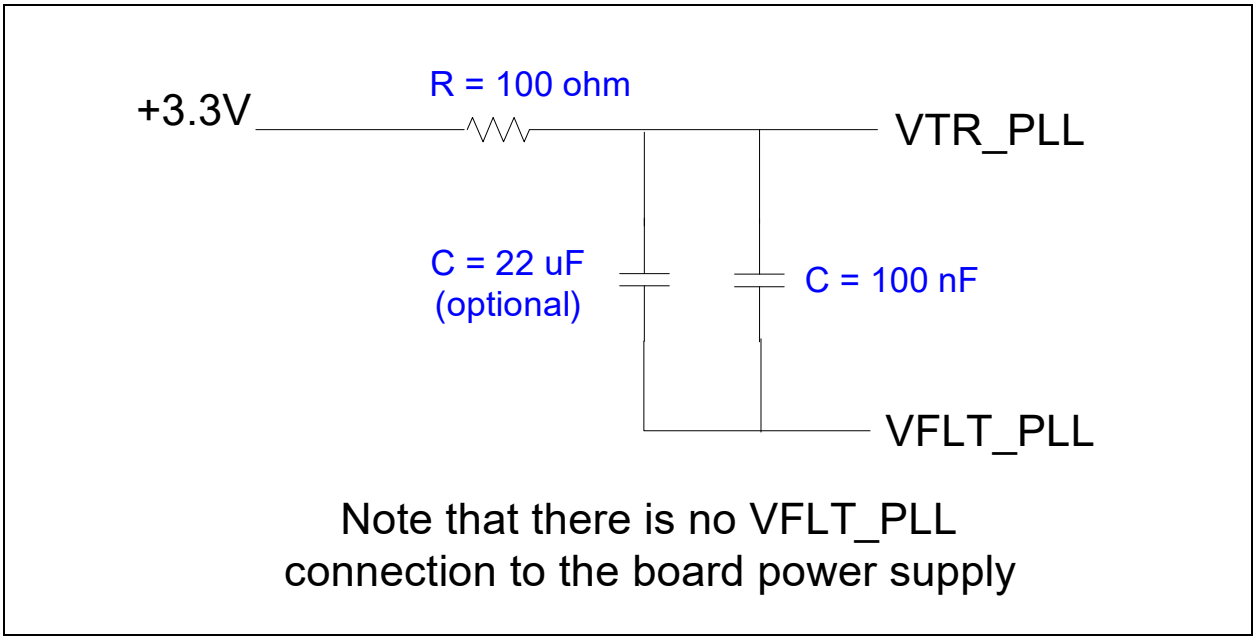
1.4.1 REAL WORLD COMPONENT SELECTION

Throughout the attenuating frequency range, there should be no resonant non-absorptions. This means that the series element will either be a resistor or a very poor (i.e. resistive) inductor.

Having got the series element with the most impedance as we can, the filter requires the highest value high frequency capacitor we can find in a small package (often 100nF). In applications with a low PLL reference frequency and environment with significant low frequency components, it is often beneficial to add a large value capacitor such as an electrolytic which fits nicely on the board (often 22uF).

The Figure 1-5 as shown below is reference schematic represents both the circuity and the device placement. The component values are only illustrative.

FIGURE 1-5: POWER SUPPLY FILTER FOR VTR_PLL



1.5 BGA Package PCB Layout Considerations

The MEC170x devices have BGA RoHS-Compliant package as follows:

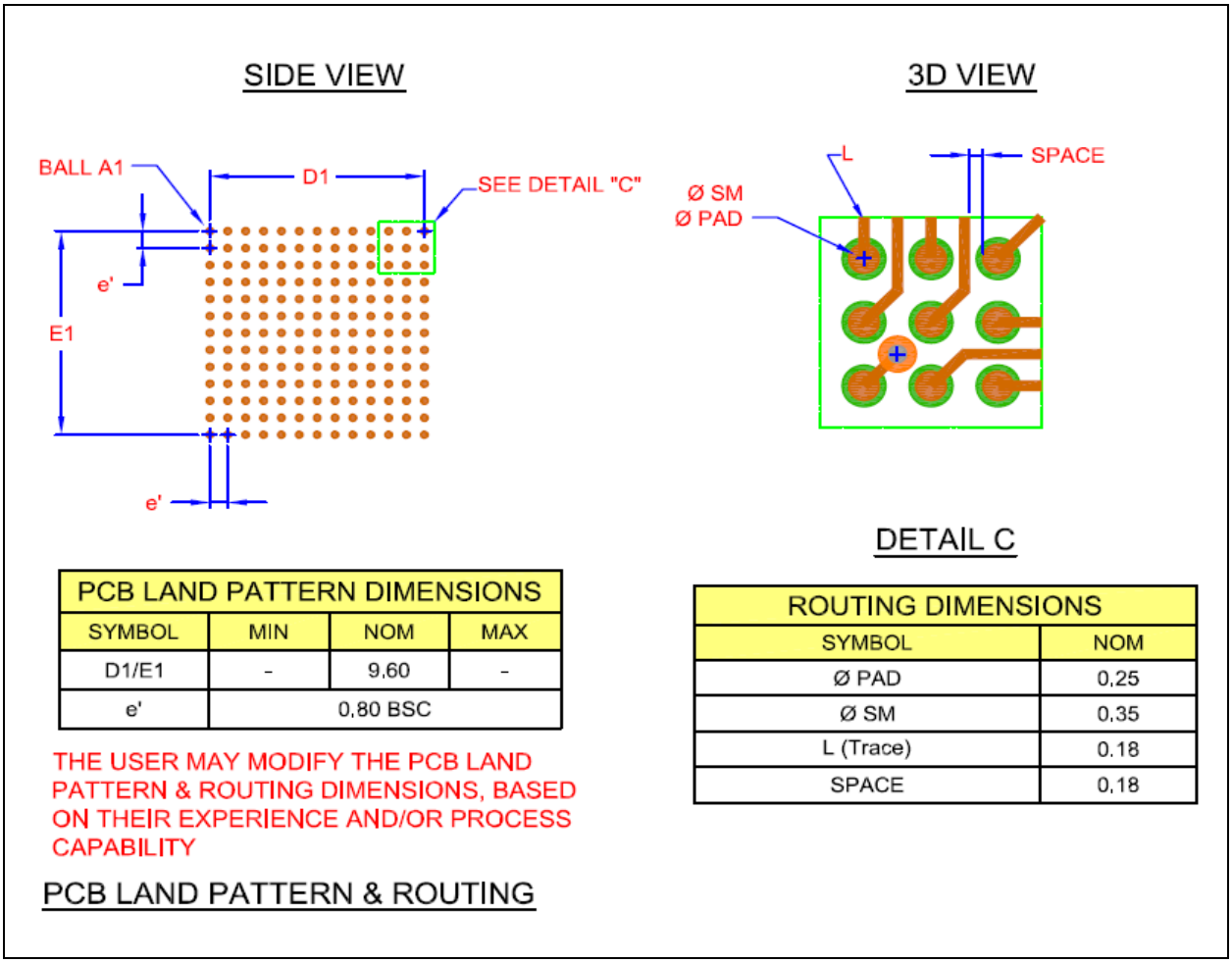
- 169-pin WFBGA: 11mm x 11mm, 0.8mm ball pitch (see Figure 1-6)
- 169-pin XFBGA: 8mm x 8mm, 0.5mm ball pitch (see Figure 1-7)
- 144-pin WFBGA: 9mm x 9mm, 0.65mm ball pitch (see Figure 1-8)

Note:	Please refer to the latest data sheet for most up-to-date PCB LAND pattern information.

The following list summarizes BGA routing guidelines, but it is understood that final layout is process- dependent and your design should reflect your needs:

- Through-hole vias technology is not recommended for pitches less than 0.8mm (unless the ball matrix is depopulated in the center)
- NSMD ball pads for pitches 0.8mm – 0.4mm
- Solder Mask to be 1:1 scale of the land size, when routing 0.5mm pitch ball pads
- μVias – next generation PCB technology for tighter pitches
- Eliminate through-hole vias
- Increase routing density & enhance electrical performance
- Decrease routing layers
- Provide fan-out solutions for multiple layers (stacked Vias)

FIGURE 1-6: LAND PATTERN DIMENSIONS, 169-WFBGA, 0.8MM BALL PITCH



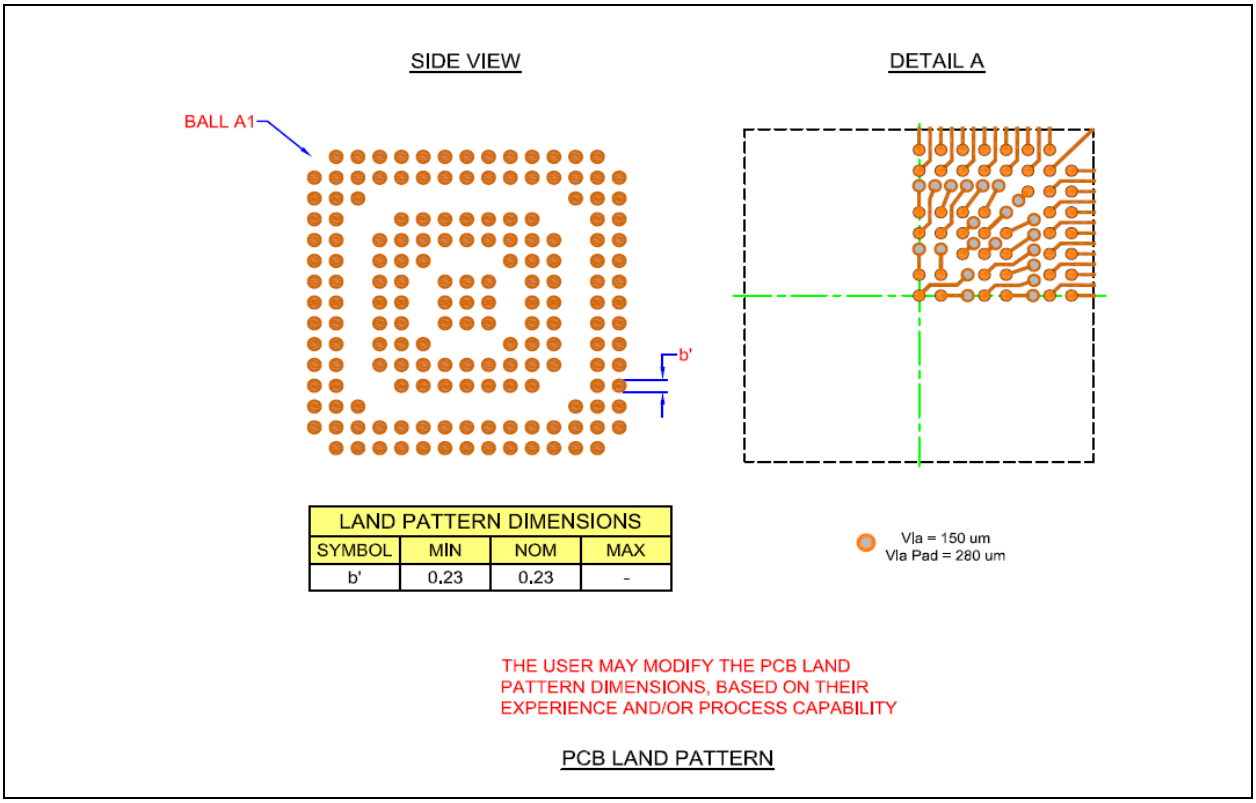
PCB LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1/E1	-	9,60	-
e'	0,80 BSC		

ROUTING DIMENSIONS	
SYMBOL	NOM
Ø PAD	0,25
Ø SM	0,35
L (Trace)	0.18
SPACE	0,18

THE USER MAY MODIFY THE PCB LAND PATTERN & ROUTING DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

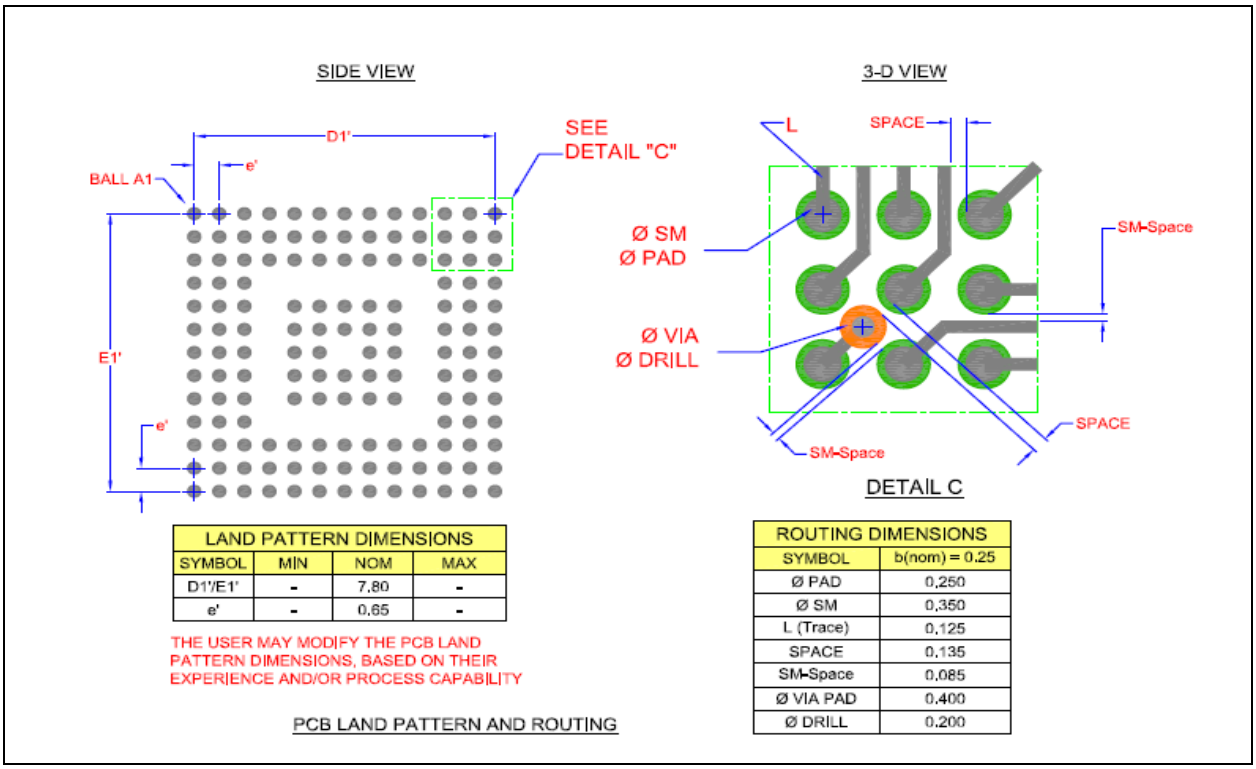
PCB LAND PATTERN & ROUTING

FIGURE 1-7: LAND PATTERN DIMENSIONS, 169-XFBGA, 0.5MM BALL PITCH



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
b'	0.23	0.23	-

FIGURE 1-8: LAND PATTERN DIMENSIONS, 144-WFBGA, 0.65MM BALL PITCH



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
D1'/E1'	-	7.80	-
e'	-	0.65	-

ROUTING DIMENSIONS	
SYMBOL	b(nom) = 0.25
Ø PAD	0.250
Ø SM	0.350
L (Trace)	0.125
SPACE	0.135
SM-Space	0.085
Ø VIA PAD	0.400
Ø DRILL	0.200

2.0 MISCELLANEOUS CONSIDERATIONS

This section covers a variety of layout topics:

2.1 Strapping Options

Table 2-1 describes the MEC170x strap option pins.

TABLE 2-1: MEC170X STRAP OPTIONS

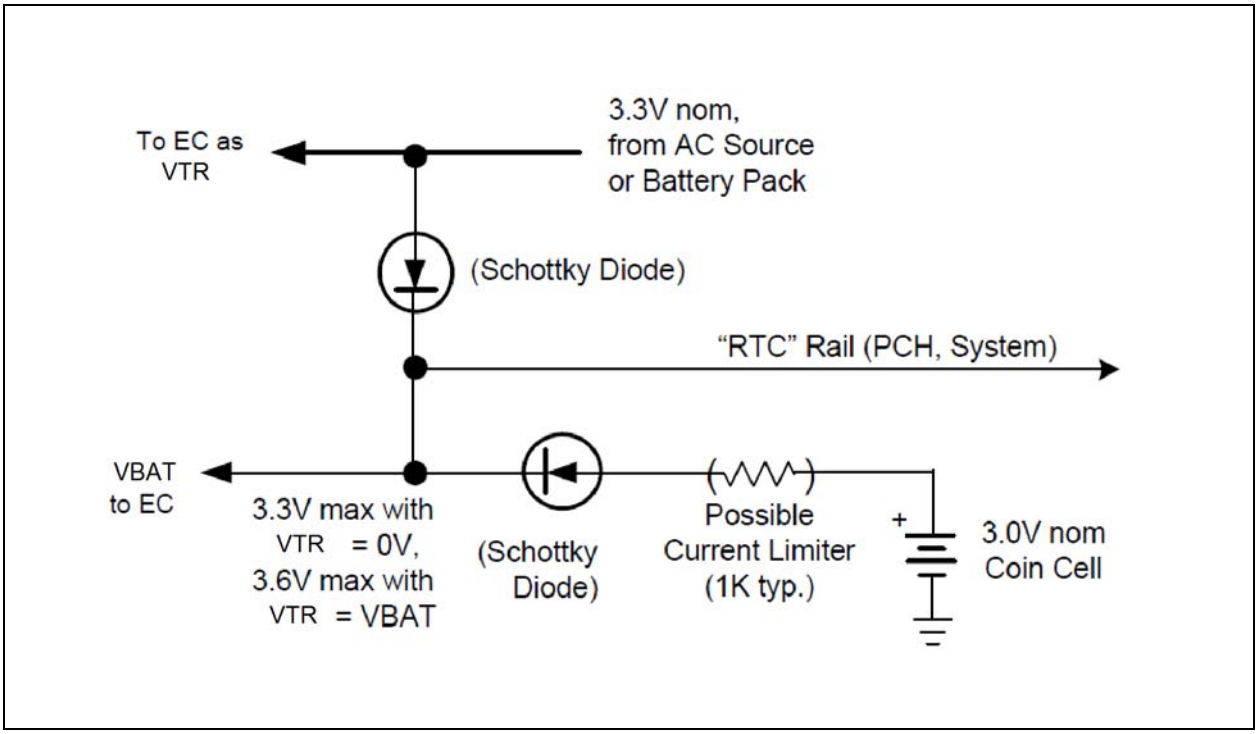
GPIO	Strap Name	Description	Pull High	Pull Low
GPIO045	Private SPI Selection	This strap option is sampled by the Boot ROM to select firmware loading from Private SPI flash or select by GPIO055.	Use the GPIO055 to determine loading selection.	Use the Private SPI pins for boot.
GPIO055	Shared SPI vs. eSPI Selection	This strap option is sampled by the Boot ROM to select firmware loading from Shared SPI flash or eSPI flash channel.	Use the Shared SPI pins for boot.	Use the eSPI Flash channel for boot.
GPIO171	TAP Controller Select Strap	This strap option is sampled on VTR power up, and is not affected by a Watchdog Timer reset. If any of the MEC170x JTAG TAP controllers are used, GPIO171 must be configured as an output to a VTR-powered external function. GPIO171 may only be configured as an input when the JTAG TAP controllers are not needed or when an external driver does not violate the Slave Select Timing.	(Default) Internal pull high selects Boundary Scan TAP Controller	External pull Low, selects Debug TAP Controller
		See the MEC170x Data Sheet, “Tap Controller Select Strap Option,” for further details.		

2.2 Battery Circuit

Please see the Power Sources section of the MEC170x Data Sheet.

For the battery circuity requirement, VBAT must always be present if VTR is present. The following circuit is recommended to fulfill this requirement.

FIGURE 2-1: RECOMMENDED BATTERY CIRCUIT



2.3 LPC Interface

The firmware must configure the GPIO Pin Control Registers for the LPC alternate function, configure the LPC Base Address Register, and activate the LPC block.

2.3.1 VTRX POWER PIN

The LPC Interface may be operated at either 1.8V or 3.3V by the VTR3 pin.

Several sideband signals associated with the LPC bus are aliased on two pins, one that is powered by VTR3 which is the same with LPC bus signals, and the second powered by VTR2. By connecting VTR3 to 3.3V, VTR2 to 1.8V and aliasing the sideband signals to the pins in the VTR2 region, the LPC bus can operate at 3.3V while sideband signals can operate at 1.8V, which is corresponds to Intel Atom platforms architecture. The aliased signals are SER_IRQ, LRESET#, LPCPD#, nSMI, and nEC_SCI.

2.3.2 HOST RESET SELECT

The platform reset signal that will be used to assert nSIO_RSET is determined by the POWER RESET CONTROL Register (40080114h) Bit 8 = 1 - LRESET# pin.

2.3.3 LAD[3:0] /LFRAME#/ LDRQ#/SERIRQ

The AC and DC specifications for these signals are set the same as defined for AD[31:0] in Section 4.2.2 of the "*PCI Local Bus Specification, Rev 2.1*". That section contains the specifications for the 3.3V signaling environment. LAD[3:0] must go high during the TAR phase. The last device driving the LAD[3:0] is responsible to drive the signals high during the first clock of the TAR phase. During the 2nd clock, LAD[3:0] is floated and maintained high by weak pullup resistors (approximately 100 k Ω). These pullups are not included in the MEC170x, but may be included in the chipset.

2.3.4 OTHER SIGNALS

All the other LPC I/F signals are connected to other PCI signals that are already present in the system. The MEC170x use 3.3V or 1.8V signaling for all LPC signals, including the PCI Reset and Clock, designers need to determine the voltage selection for all LPC & sideband signals by VTR3 and VTR2.

2.4 eSPI Interface

The firmware must configure the GPIO Pin Control Registers for the eSPI alternate function, configure the eSPI I/O Component Base Address Register, and activate the eSPI block.

2.4.1 VTRX POWER PIN

The eSPI Interface signals require the VTR3 power pin to be connected to the 1.8V rail.

2.4.2 HOST RESET SELECT

The platform reset signal that will be used to assert nSIO_RSET is determined by the POWER RESET CONTROL Register (40080114h) Bit 8 = 0 - eSPI_PLTRST# pin.

2.4.3 OTHER SIGNALS

All the eSPI I/F signals are connected to other eSPI signals that are already present in the system. The MEC170x use 1.8V signaling for all eSPI signals. Please refer to the Intel Skylake Ultrabook Platform U-Series RVP Customer Reference Board Schematic, Microchip MEC170x Evaluation Board Schematic, and reworks instruction for detailed information.

Few design notes as below:

- LPC_AD0_ESPI_IO0, LPC_AD1_ESPI_IO1, LPC_AD2_ESPI_IO2, LPC_AD3_ESPI_IO3, LPC_-FRAME_ESPI_CS#, and LPC_CLK_0_ESPI_CLK signals have 15 ohm series resistor close to each chipset pin and another 15 ohm series resistor close to the MEC170x for eSPI mode.
- GPP_C5/SML0ALERT# (Intel Skylake chipset pin W1) is used as strapping pin to determine either LPC mode (Low) or eSPI mode (High).

2.5 PS/2 Interface

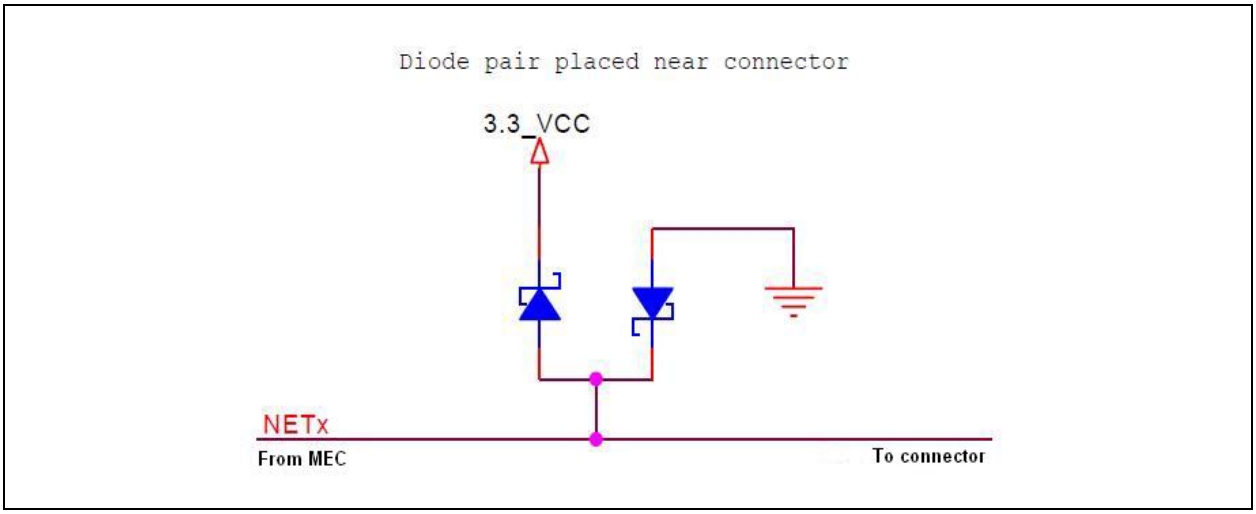
The routing of the PS/2 interface is also not critical, except that it should not be routed next to rapidly switching signals. The Clock and Data pins are Open Drain and require pullup resistors. A small 10 - 100pF (typ) capacitor to ground and 4.7kΩ (typ) pullups are recommended. The power pin of the PS/2 pin should be decoupled with a capacitor that is large enough to adequately filter the supply to PS/2 devices. Unused PS/2 clock and data pins should be pulled up to VTR with a 10kΩ (typ) resistor.

Note:	Two PS/2 ports are 5V tolerant when in 3.3V mode. The other three PS/2 ports are not.

2.6 EOS Considerations

For SMBus signals that terminate external to the main system board (for example, Smart Battery) the designer should take care in protecting these signals from EOS (Note 2-1) and ESD (Note 2-2). Please refer to the SMBus 2.0 specification, section 3.1.2.2 for appropriate guidelines. The specification recommends a series protection resistor and an optional ESD transorb on these nets. In addition to the SMBus specification recommendation, past experience shows that using 2 high speed diodes on each SMBus trace (instead of the transorb in the SMBus spec) is an effective way to improve immunity to EOS and ESD events. A Schottky diode pair is a good example. Figure 2-2 shows the suggested circuit implementation for each net that goes to a connector.

FIGURE 2-2: SCHOTTKY DIODE PAIR EXAMPLE



It should also be noted that any other signal that goes to an external connector should also be considered for EOS/ESD susceptibility. For instance, an ID pin (tied to a GPIO) that might seem benign, but is routed near high voltage sources could suffer transient EOS events. A similar protection scheme should be considered for these nets.

Note 2-1 EOS is defined as damage to the part caused by the application of voltages (to any pin) beyond the power supply rails, usually forward biasing internal protection diodes and resulting in high levels of current flow. This typically induces open failures by damaging the metal inside the part. EOS is typically a low voltage, high current situation.

Note 2-2 ESD is the applied reverse bias to the PN junction -- heat due to power dissipation melts the silicon in the part. ESD is typically a high transient voltage spike with low current situation.

2.7 ADC Input Layout Requirements for Regular Sampling

ADC has a large internal resistance.

Every ADC input terminal has a gate switch.

This gate switch is protected by diodes.

It is natural for diodes have leakage current.

At sampling time: (Gate switch closed)

Input voltage is charged and sampled at sample point A.

Sampling time is affected by RC time constant defined by internal resistor and internal capacitor.

In continuous mode, the sampling time is too fast for sample point A to discharge sampled value. In this case, glitch will not be observed.

In one shot mode or in long report mode, the sampling time is long enough for point A to discharge sampled value.

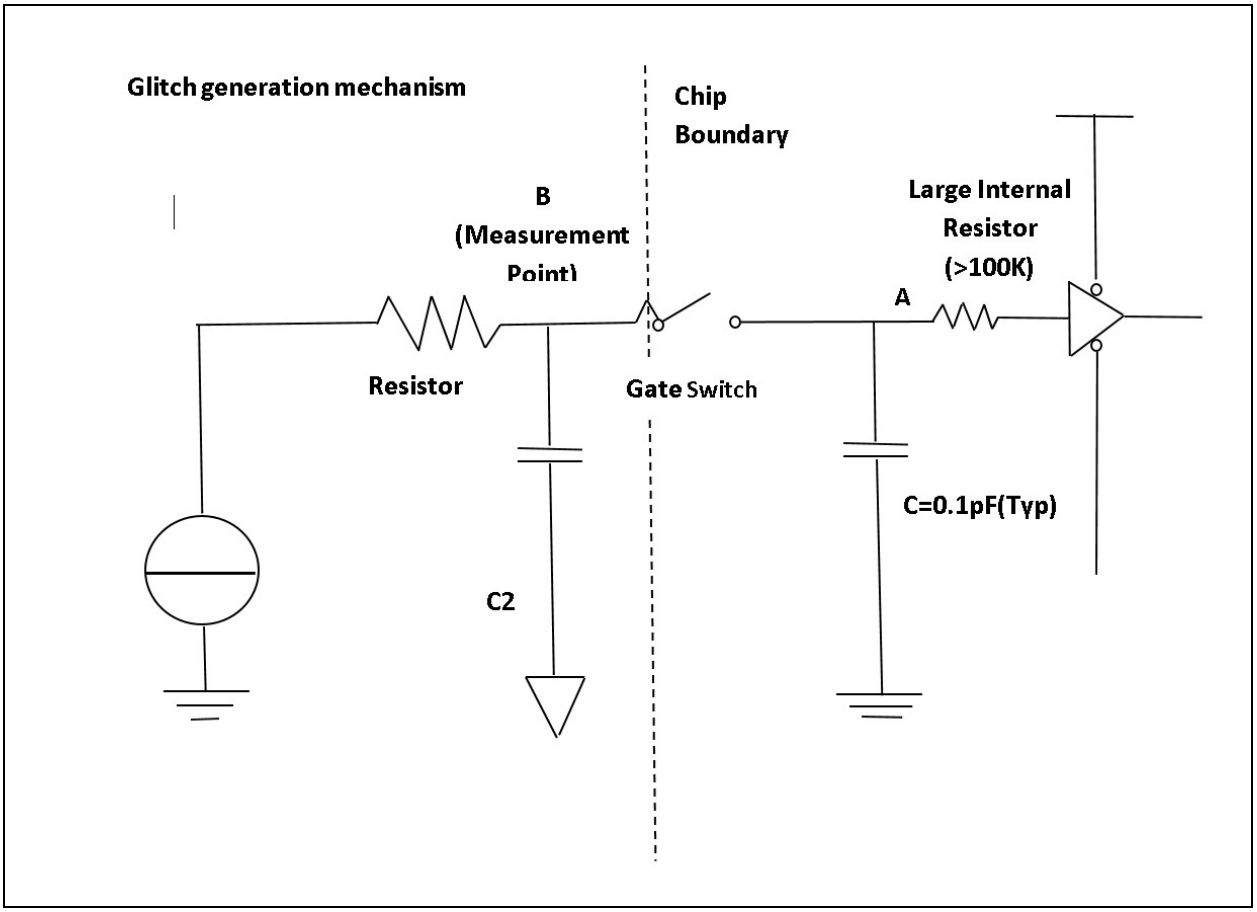
In this case, glitch will be observed on the next sampling point.

If an external capacitor with value between 0.1uF and 0.01uF (point C2) is placed on the input terminal, the charged value at point A will be kept as it is instead of discharging it and then glitch will not be observed.

For high sampling frequencies, it is recommend to set the cut off frequency of the R/C at ½ of the ADC sampling frequency / 10.

Please also refer to the white paper at ww1.microchip.com/downloads/en/AppNotes/00699b.pdf for more information.

FIGURE 2-3: ADC INPUT LOW PASS FILTER



2.8 SPI Flash Implementation

The MEC170x SPI flash interface enables the host and embedded controller (EC) access to an external SPI flash device. The MEC170x Data Sheet and Boot ROM Application Note have more details on detail information (see References on page 1). This section describes specific PCB layout design considerations to setup this feature.

Note:	The SPI Flash Interface of MEC170x can be selected either 3.3V or 1.8V. The SHD SPI interface is on VTR2 power rail, and PVT SPI interface is on VTR1 power rail.

The standard set of SPI flash signals are designated with “SHD_” for shared connections, for example, SHD_CLK; for details, see Section 2.8.3, "Shared SPI Flash Interface". MEC170x has an added set of signals for connection to another SPI flash device as private, protected data; these signals are designated with “PVT_,” for example, PVT_CLK; for details, see Section 2.8.4, "Non-shared SPI Flash Interface". The MEC170x has a third SPI interface as a general SPI interface labeled as “SPI_,” for example, SPI_CLK.

TABLE 2-2: SPI INTERFACE SIGNALS

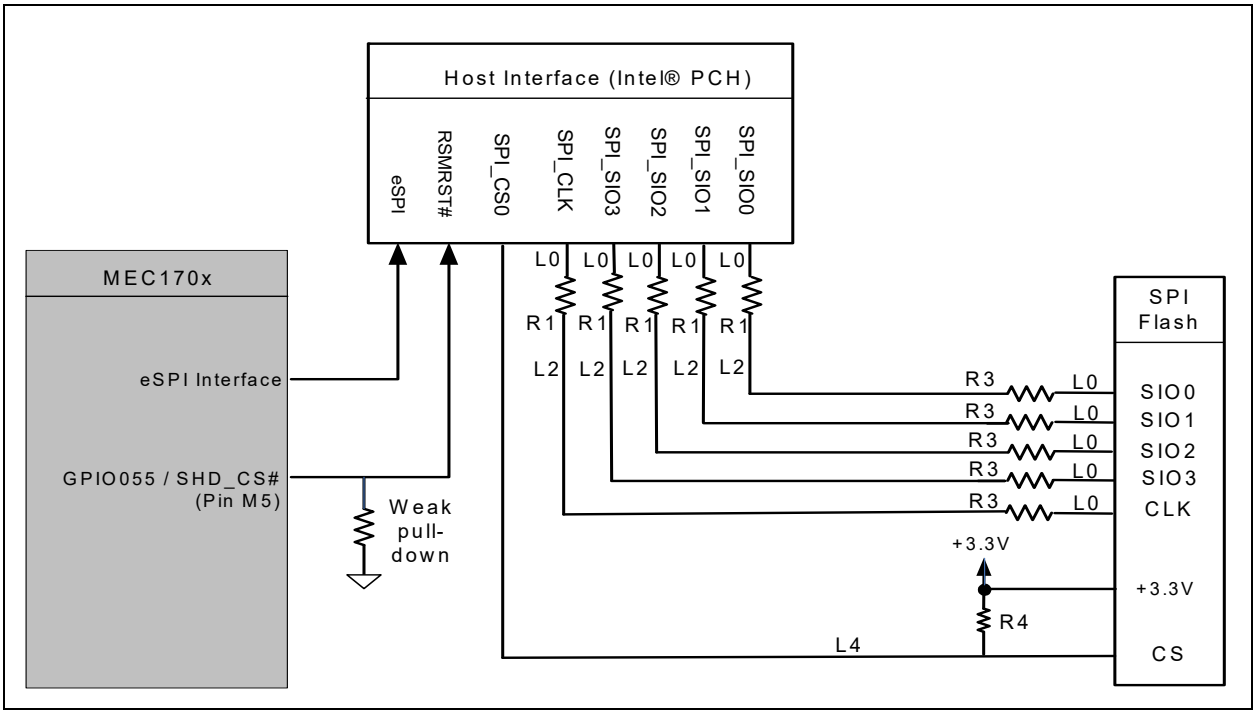
Generic Pin Signal Name	Pin Signal Function name	Pin Function Signal Description
SPICLK	SHD_CLK	Shared SPI Clock
	PVT_CLK	Private SPI Clock
SPI_CS#	SHD_CS#	Shared SPI Chip Select
	PVT_CS#	Private SPI Chip Select
IO0 / MOSI	SHD_IO0 / SHD_MOSI	Shared SPI Data I/O 0.
	PVT_IO0 / PVT_MOSI	Private SPI Data I/O 0.
	Note: Also used as SPI_MOSI when the interface is used in single wire mode.	
IO1 / MISO	SHD_IO1 / SHD_MISO	Shared SPI Data I/O 1.
	PVT_IO1 / PVT_MISO	Private SPI Data I/O 1.
	Note: Also used as SPI_MISO when the interface is used in single wire mode.	
IO2	SHD_IO2	Shared SPI Data I/O 2
	PVT_IO2	Private SPI Data I/O 2
	Note: Only used in Quad Mode. Also can be used by firmware as WP.	
IO3	SHD_IO3	Shared SPI Data I/O 3
	PVT_IO3	Private SPI Data I/O 3
	Note: Only used in Quad Mode. Also can be used by firmware as HOLD.	

2.8.1 SELECTION OF SPI PORT & RSMRST#

The MEC170x Boot ROM firmware selects two potential sources, the Shared SPI port or the eSPI Flash Channel, from which to load the application firmware. The selection is done by sampling the GPIO055.

When used with a PC-based core logic, the EC must supply the RSMRST# signal to the core. If the eSPI Flash Channel is used as the source for EC firmware, the **GPIO055/SHD_CS# pin MUST be used as the RSMRST# signal**. A weak-pulldown resistor to ground must be connected to the pin as shown inFigure 2-4. The pull-down both holds RSMRST# low glitch-free during the power-on sequence, as required by the core logic, and informs the Boot ROM in the MEC170x to use the eSPI Flash Channel.

FIGURE 2-4: MEC170X SHARED SPI FLASH DEVICE THRU ESPI FLASH CHANNEL



If the EC firmware is sourced from an external SPI Flash device directly to the Shared SPI Flash interface, **the GPIO055/SHD_CS# pin MUST NOT be used as the RSMRST# signal**. Any other GPIO can serve as RSMRST#, if connected to ground with a weak pull-down resistor as shown in Figure 2-5. Once firmware is loaded and executed, it can release RSMRST# by setting the selected GPIO high.

2.8.2 SHARED VS. NON-SHARED SPI IMPLEMENTATION

Section 2.8.3, "Shared SPI Flash Interface" describes implementing the SPI Flash Interface using the shared signals (for example, SHD_CLK); Section 2.8.4, "Non-shared SPI Flash Interface" describes implementing the SPI Flash Interface using private signals (for example, PVT_CLK).

See Section 2.8.4, "Non-shared SPI Flash Interface" for further details of this setup.

2.8.3 SHARED SPI FLASH INTERFACE

2.8.3.1 Shared SPI Flash Implementation

Figure 2-5 is a topology for implementing a single MEC170x SPI flash for shared SPI flash devices. See Table 2-3 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-5: MEC170X SHARED SPI FLASH DEVICE THRU SHD SPI INTERFACE

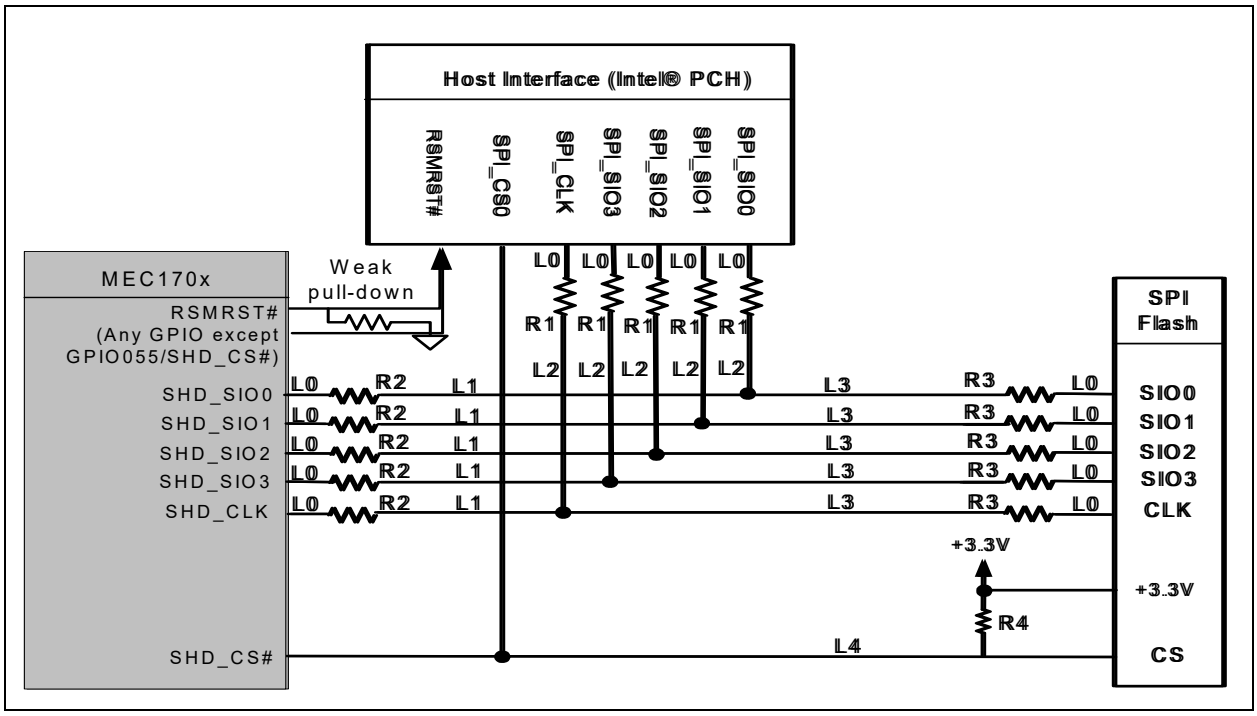


TABLE 2-3: MEC170X SHARED SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between MEC170x, Host/PCH, or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	PCB trace from the MEC170x termination resistor to the PCB trace connection from the SPI flash and Host/PCH.	L1 = L2 = L3 These trace connections can equal 1-inch up to 5-inches. See Note 2-5
L2	PCB trace from the Host/PCH termination resistor to the PCB trace connection from the SPI flash and MEC170x.	
L3	PCB trace from the SPI flash termination resistor to the PCB trace connection from the MEC170x or Host/PCH.	
L4	PCB trace from Host/PCH or MEC170x to SPI flash for chip select.	L4 = L1 + L3 + (2 x L0) or L4 = L2 + L3 + (2 x L0) +/- 0.100 inches.
R1	These resistors are between the PCB trace and the Host/PCH.	25 ohm, see Note 2-3, Note 2-4
R2	These resistors are between the PCB trace and the MEC170x.	15 ohm, see Note 2-3, Note 2-4
R3	These resistors are between the PCB trace and the SPI flash.	15 ohm, see Note 2-3, Note 2-4
R4	Pull-high resistor to +3.3V for SPI CS connections; between the MEC170x or Host/PCH and the SPI flash device. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-3 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC,

PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC170x (-0.3V min. to VTR+0.3V max).

Note 2-4 Resistor recommendations are based on testing with 180nm PCH and SPI flash drivers. Any change to a driver would require a change to the related termination resistors, see also Note 2-3.

Note 2-5 L1, L2, L3 must be equal to each other. For example, if L1 = 2-inches, then L3 must be 2-inches.

2.8.4 NON-SHARED SPI FLASH INTERFACE

Note:	Either Shared SPI or Private SPI interface can support a dedicated SPI chip.

2.8.4.1 Non-Shared SPI Flash Implementation

Figure 2-6 and Figure 2-7 are topologies for implementing the MEC170x SPI flash for a single SPI flash device. The selection between PVT or SHD SPI flash interface is determined by the GPIO045 in the Boot Rom. See Table 2-4 for specifications on PCB trace recommendations represented by “L1,” “L2,” and so forth.

FIGURE 2-6: SINGLE SPI FLASH ON PRIVATE SPI FLASH I/F (GPIO045 = 0)

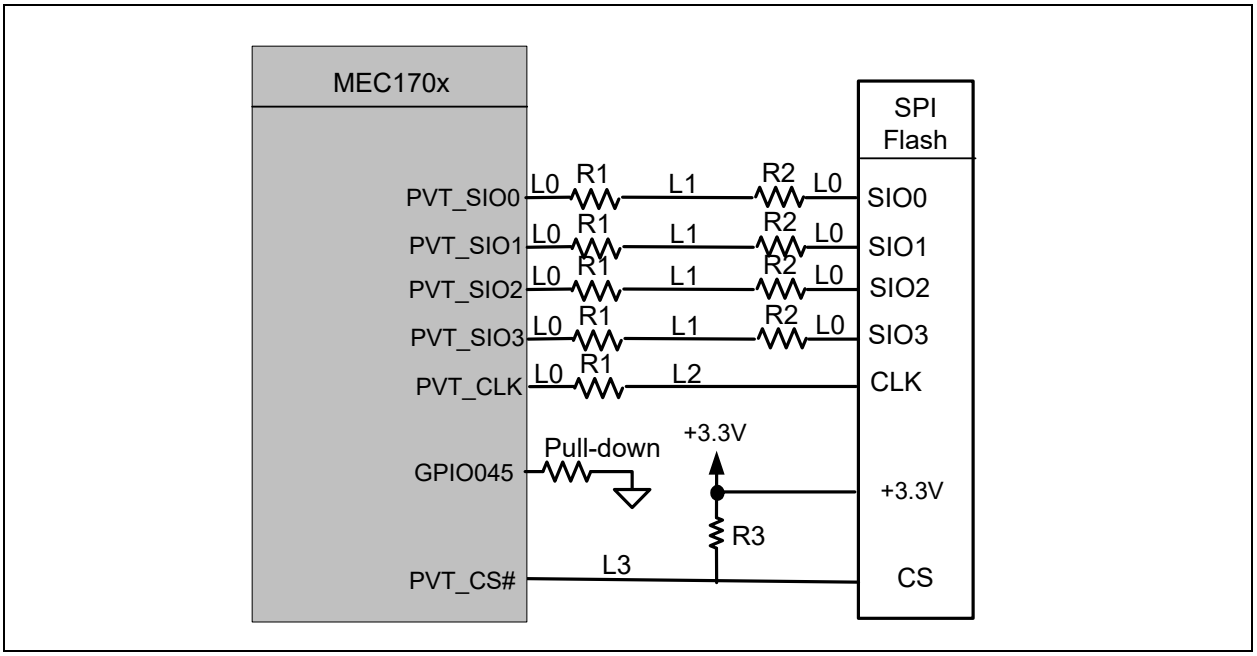


FIGURE 2-7: SINGLE SPI FLASH ON SHARED SPI FLASH I/F (GPIO45 = 1, GPIO55 = 1)

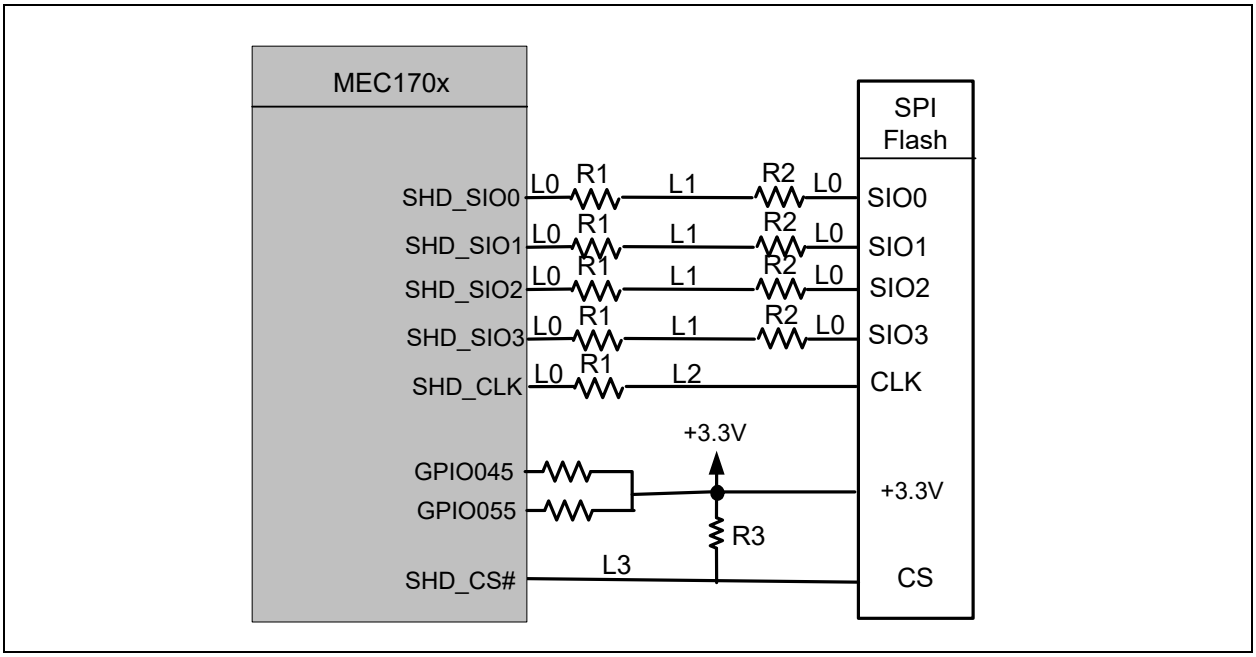


TABLE 2-4: MEC170X SINGLE SPI FLASH DEVICE SPECIFICATIONS

	Description	Spec
L0	Connection between MEC170x or SPI flash device and termination resistors.	0.1-inch to 0.5-inch
L1	The PCB trace between terminating resistors on the IO lines.	1-inch to 10-inch
L2	The PCB trace from MEC170x or R1 resistor to SPI flash.	1-inch to 10-inch
L3	PCB trace from MEC170x to SPI flash for chip select.	L3 = L0 + L1
R1	These resistors are between the trace and the MEC170x.	25 ohm, see also Note 2-6
R2	This resistor is on the IO lines between the SPI flash and trace.	45 ohm, see Note 2-6.
R3	This is a Pull-High resistor (to +3.3V) for SPI CS connections. This pull-high must connect to the same power rail of the SPI flash.	4.7K ohm

Note 2-6 The final value of the series resistors should be chosen based on performing electrical analysis to ensure the electrical timings and min/max voltage specifications are met for each device (SPI, EC, PCH or other Host SPI controller) including the undershoot/ overshoot specifications for the MEC170x (-0.3V min. to VTR +0.3V max).

2.8.5 SPI FLASH IMPLEMENTATION RECOMMENDATIONS

The following recommendations are for both Shared and Private SPI Flash Implementations.

- The MEC170x SPI memory interface has serial flash device compatibility requirements that are defined in the MEC170x Data Sheet. Please make sure the selected SPI flash meets these requirements.
- SPI_CLK must be 20mils spacing from any other high frequency (>1GHz) signal.
- The SPI flash parts should support operating at 12MHz for the ROM code loader, and up to 48MHz clock speed in RAM code loading.
- The designer should follow the SPI interface host design guidelines.
- IBIS models are available to aid in simulating the SPI system topology.
- The chip select CS# signals should have weak pullup resistors to the same power rail as the SPI flash. The pullup resistor value should meet the rise time requirements of the SPI flash.
- EC firmware must configure the MEC170x SPI memory interface to disable mode, which will tri-state the SPI memory interface from MEC170x to the SPI flash, before releasing the RSMRST# signal.

- This configuration requires that the PCH tri-state its SPI flash pins when RSMRST# is asserted.
- The characteristic impedance of the PCB trace should be 50 ohms +/-15% at 50MHz operating frequency.
- Within the SPI flash device, Schmitt trigger inputs are assumed on both the clock line and IO data lines.
- Within the Intel PCH, a Schmitt trigger input is assumed on the IO data lines.
- The output drivers for the SPI flash chip select pins should be programmed as open-drain using the GPIO Pin Control registers.
- The SPI Data IO traces should be length-matched to the CLK lines within 0.100-inch.
- Signal Integrity should be checked for each SPI part on your BOM.

2.8.6 SPI FLASH EXTERNAL PROGRAMMER

The SPI Flash on either Shared or Private SPI Flash interface must be programmed externally using a suitable programmer, such as Dediprog's SF100 (http://www.dediprog.com/pd/spi-flash-solution/sf100).

Provisions for a programming header on each SPI flash are recommended if the SPI is not socketed.

2.9 1MHz Pullup Resistor Requirement

Please refer to the I^2C-bus specification and user manual as indicated in the section References on page 1 for more information.

2.10 5V Tolerant Pins

There are fourteen 3.3V/5V tolerant pins on the MEC170x. Please see the MEC170x Data Sheet "Over-voltage Protection" section for more information.

2.11 1.8V Capability

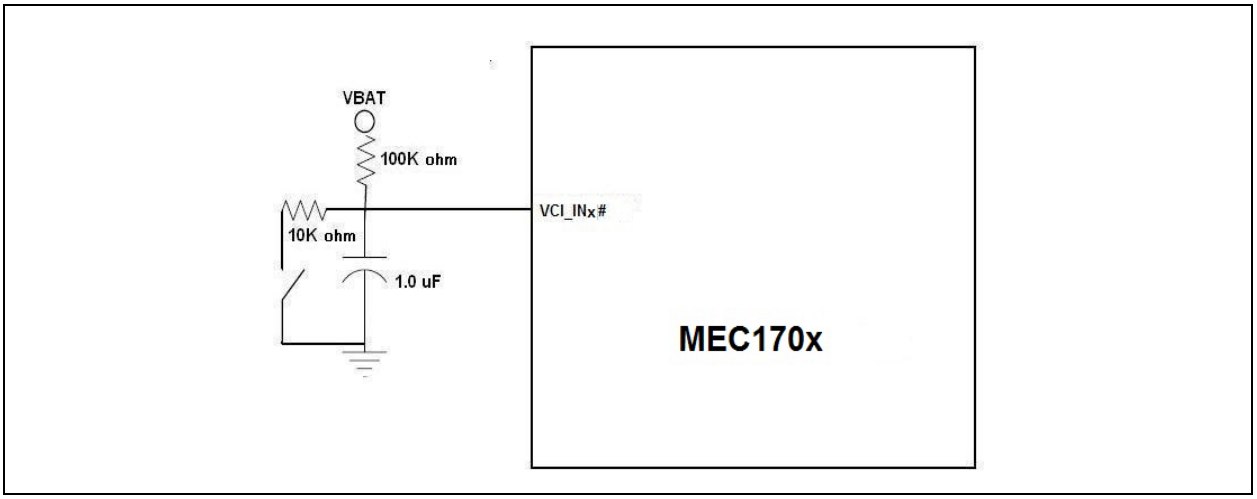
There are three voltage supply regions for all GPIO pins powered by VTR1, VTR2, and VTR3. Each region may be either 3.3V or 1.8V. Please refer to the MEC170x Data Sheet section 2 for more information.

Note:	The LPC Interface Signals require the VTR3 power pin to be connected to the 3.3V or 1.8V VTR rail. The eSPI Interface signals require the VTR3 power pin to be connected to the 1.8V rail.

2.12 Power Switch Input

For the VBAT-powered power switch inputs (VCI_INx#) there is a specific requirement for the input circuit as illustrated in Figure 2-8. The resistors can use any typical 1/10W, +/- 1% carbon, thick, metal, or thin film. The capacitors can use any typical 16V 10% ceramic. Unused VCI pins should be pulled up to VBAT via a 100K resistor. Please refer to the MEC170x EVB Schematics and Bill of Materials.

FIGURE 2-8: VBAT-POWERED CONTROL INPUT CIRCUIT



2.13 VCI_IN Pins when Used as GPIO

All the VCI_IN pins can be used as GPIOs. This is required the firmware to program the VCI_BUFFER_EN bit[6:0] at VCI Buffer Enable Register to disable power up functionality on these VCI pins if these are used as GPIOs.

2.14 PECI

The PECI Interface core logic is powered by VTR1; the physical interface power domain is VREF_VTT. If PECI is not used, the corresponding MUX_CONTROL field for GPIO044 should be set to GPIO in order to minimize leakage current when VREF_VTT is not required.

2.15 MEC170x Shared SPI Flash Isolation Requirement

The MEC170x uses the GPIO055/SHD_CS# pin as a strap to determine the boot source (eSPI Flash channel or shared SPI).

There is a new requirement to put isolation on the board if the Shared SPI flash is used so that the SPI_CS# is detected high while RSMRST# is low.

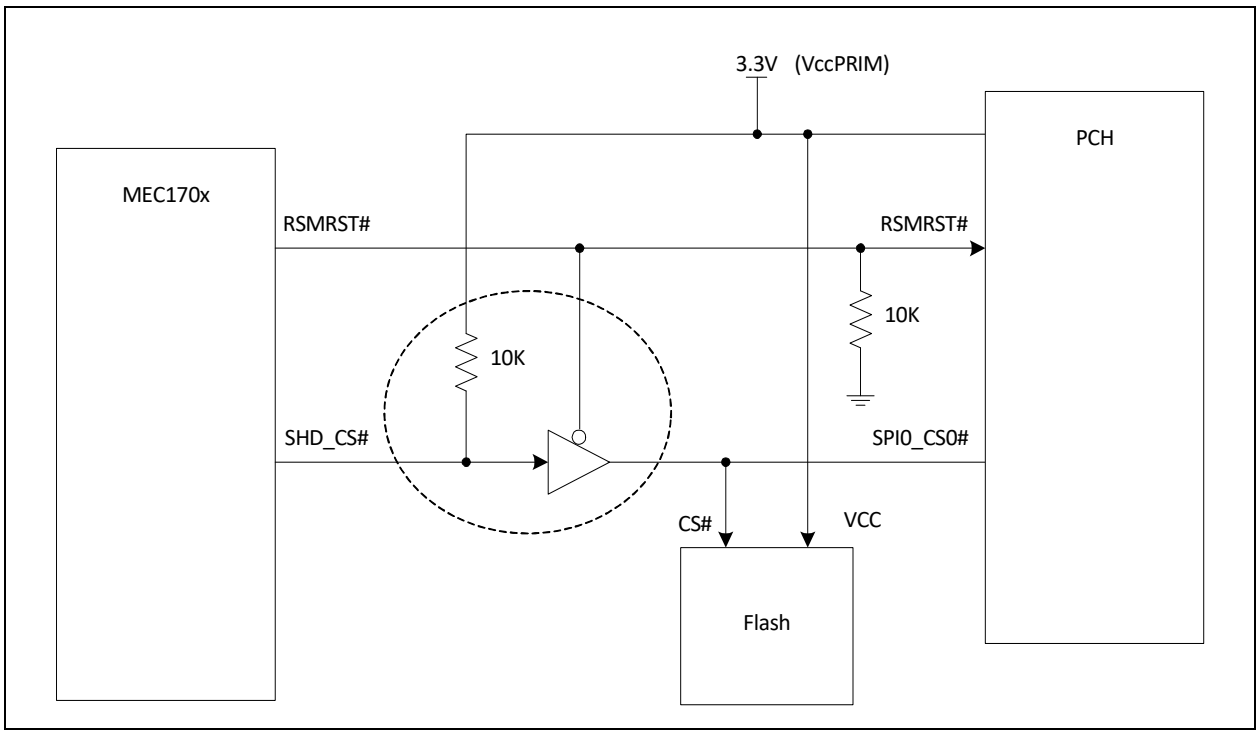
This requirement is due to the following information in the current Intel PCH device specification regarding the SPI0_CS0# pin:

SPI0_CS0# is pulled low instead of high (internally in the PCH)

The “pull” strength is about 1K ohms.

One example of a recommended isolation circuit requires an external tri-state buffer, so that the pull-up for the strap can be of reasonable strength. One possible buffer is the 74LVC1G125 which has a small propagation delay that will not impact the timing of the existing Boot ROM code.

The buffer and pull-up on the SHD_CS# pin is shown in the figure below.



2.16 Glitch Protection Pins

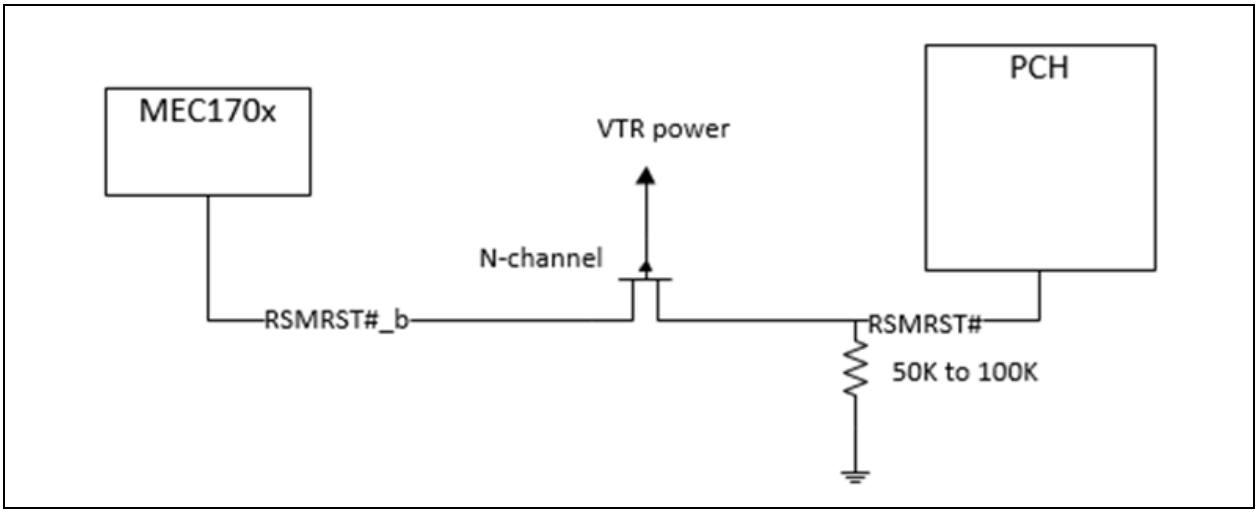
Glitch protection pins are de-featured for MEC170x family devices. If the customer design has any glitch sensitive signals, such as PCH RSMRST#, please see our recommendation below.

Option 1: (Preferred solution)

Do not cycle VBAT to the MEC170x devices – If the MEC170x VBAT is the same as the Intel PCH, then the glitch will only happen when the coin cell is changed – at that time, the CMOS is not valid, so there is no issue.

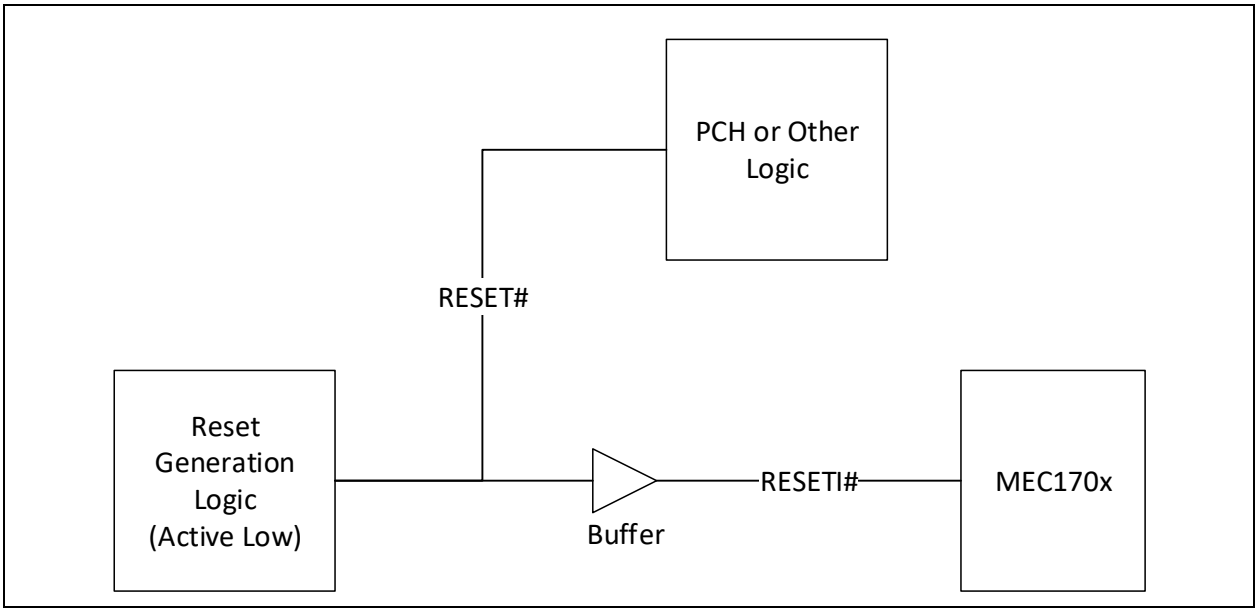
Option 2:

Put a glitch suppression RC circuit on the pin or a glitch protection circuit. This needs to keep the glitch below approximately 1.0Volts. Example as shown below.



2.17 Glitch on ResetI#

ResetI# must not be connected directly to a PCH critical pin, such as RSRMRST# or DSW_PWROK on PCH. Below is an example of a circuit that will prevent back driving to other logic.



3.0 JTAG DESIGN AND LAYOUT GUIDE

This section provides general hardware information for using the MEC170x JTAG interface and working with JTAG master and slaves.

This document includes the following topics:

3.1 MEC170x JTAG Capabilities

MEC170x devices have the following debug capabilities:

- JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
- Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
- Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
- Accessed via 4-wire JTAG or 2-wire ARM SWD
- Comprehensive ARM-Standard Trace Support: Full DWT, ITM, ETM, TPIU functionalities

3.2 General PCB Layout Considerations for JTAG

Please follow the PCI Specification's Routing and Layout Guidelines for the JTAG interface signals to support the JTAG interface speed up to 33MHz.

- In order to improve the clock transmission line's signal integrity, the following is recommended:
  - Keep the clock traces as straight as possible
  - Use arc-shaped traces instead of right-angle bends
  - Do not use multiple signal layers
  - Do not use vias to reduce impedance change and reflection
  - Place a ground plane next to the outer layer to minimize noise effect
  - Terminate clock signals to minimize reflection
- The JTAG cable that attaches to the MEC170x motherboard has a standard 20-pin .1" spacing female connector on it. Normally, the MEC170x motherboard just has a 20-pin 0.1" spacing pin strip on the board to mate with it.
- If the MEC170x motherboard design does not have the space for a 20-pin male pin strip, then the board designer can place a 6 pin header on the motherboard and build a 6-pin to 20-pin adapter cable to attach to the 20-pin female connector on the JTAG cable. This is shown in Figure 3-1, "6-Pin to 20-Pin Adapter Board (w/ BOM)".

3.3 Pin Connections

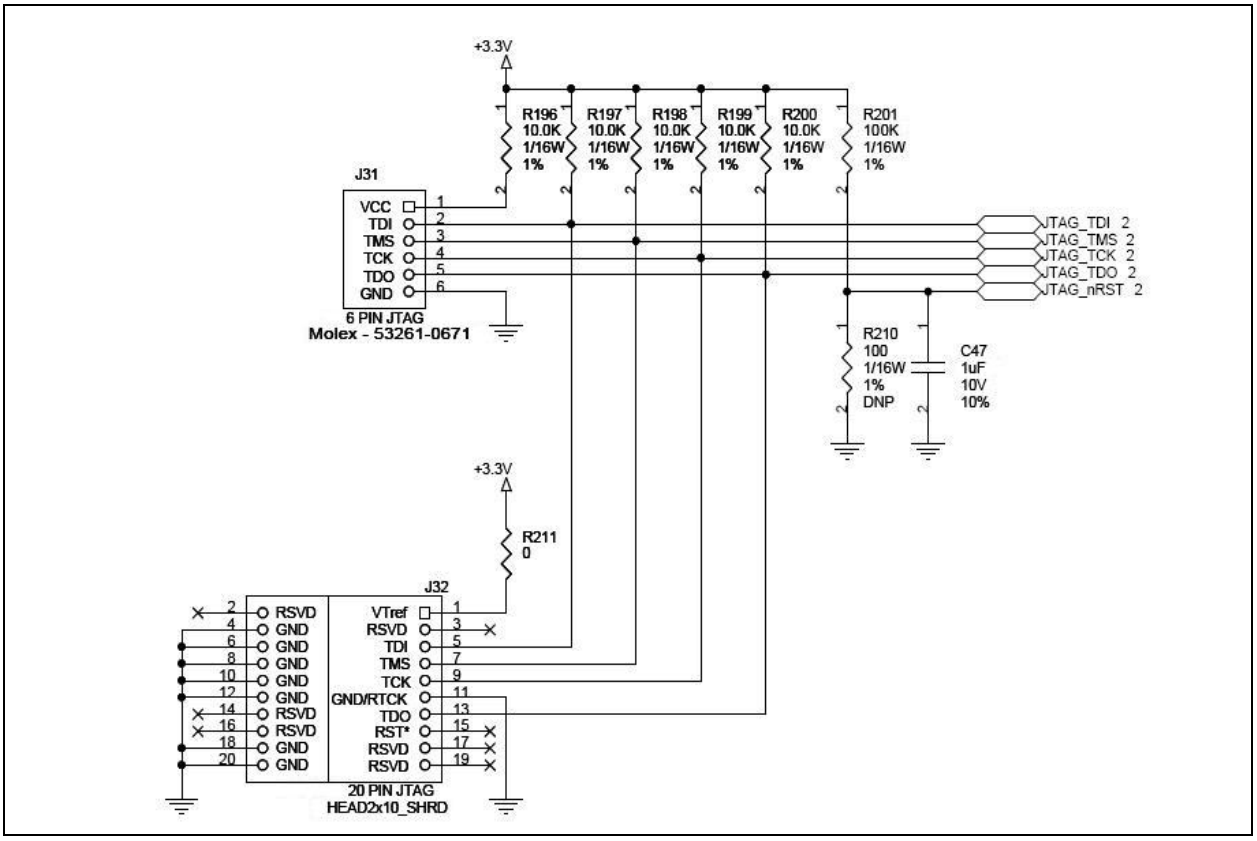
3.3.1 4-WIRE JTAG CONNECTION

Six signals are the minimum number required on the motherboard side; these are described in Table 3-1 and illustrated in FIGURE 3-1: 6-Pin to 20-Pin Adapter Board (w/ BOM) on page 25.

TABLE 3-1: MEC170X 4-WIRE JTAG PINS

Name	JTAG Cable Connection
VTR	The motherboard VTR is always 3.3V. It is recommended to add a 49-ohm series resistor for motherboard protection. The JTAG cable senses the voltage level on this line and drives the JTAG logic levels to the same voltage level from the target system.
TDI	Test Data In
TMS	Test Mode Select
CLK	Test Clock
TDO	Test Data Out
GND	Motherboard ground connect

FIGURE 3-1: 6-PIN TO 20-PIN ADAPTER BOARD (W/ BOM)



Note 1: The 10K pullups that are shown in Figure 3-1 are used on MEC170x JTAG inputs to prevent them from floating when the JTAG cable is not attached.

2: The MEC170x JTAG RST# pin connects to a 100K pullup to always enable the JTAG interface. Board design can provide pads for a pullup and pulldown for this pin in motherboard layout.

3: In order to prevent potential damage, use a keyed connector to avoid plugging the cable in backward which would result in a short between VTR and ground.

4: Add zero-ohm resistors to the JTAG link if there is a JTAG chain is used.

3.3.2 2-WIRE JTAG CONNECTION

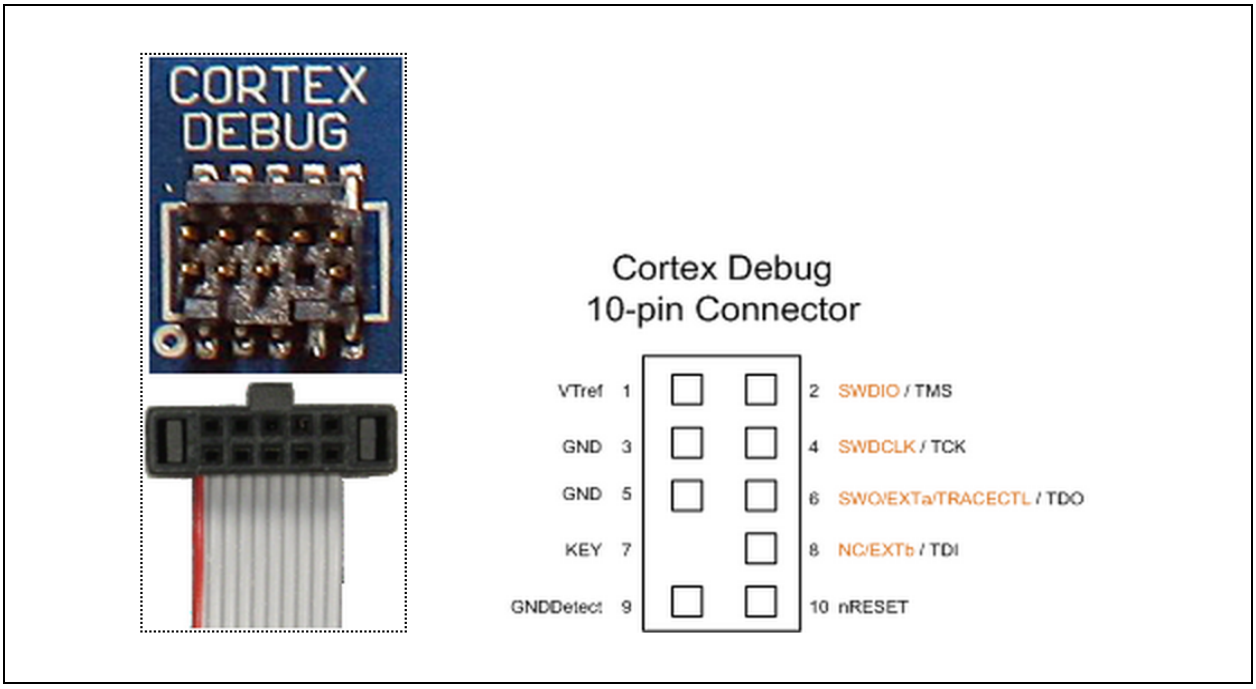
Five signals are the minimum number required on the motherboard side; these are described in Table 3-2.

TABLE 3-2: MEC170X 2-WIRE JTAG PINS

Name	JTAG Cable Connection
VTR	The motherboard VTR is always 3.3V.
SWDCLK	Use on JTAG_CLK pin if selected.
SWO	Use on JTAG_TDO pin if selected.
SWDIO	Use on JTAG_TMS pin if selected.
GND	Motherboard ground connect

Figure 3-2 shows the standard ARM Cortex 10 pins connector (a Samtec FTSH-105-01 w/ pin 7 removed).

FIGURE 3-2: 10-PIN CORTEX DEBUG (0.05”) CONNECTOR



3.3.3 TRACE FUNCTIONS CONNECTION

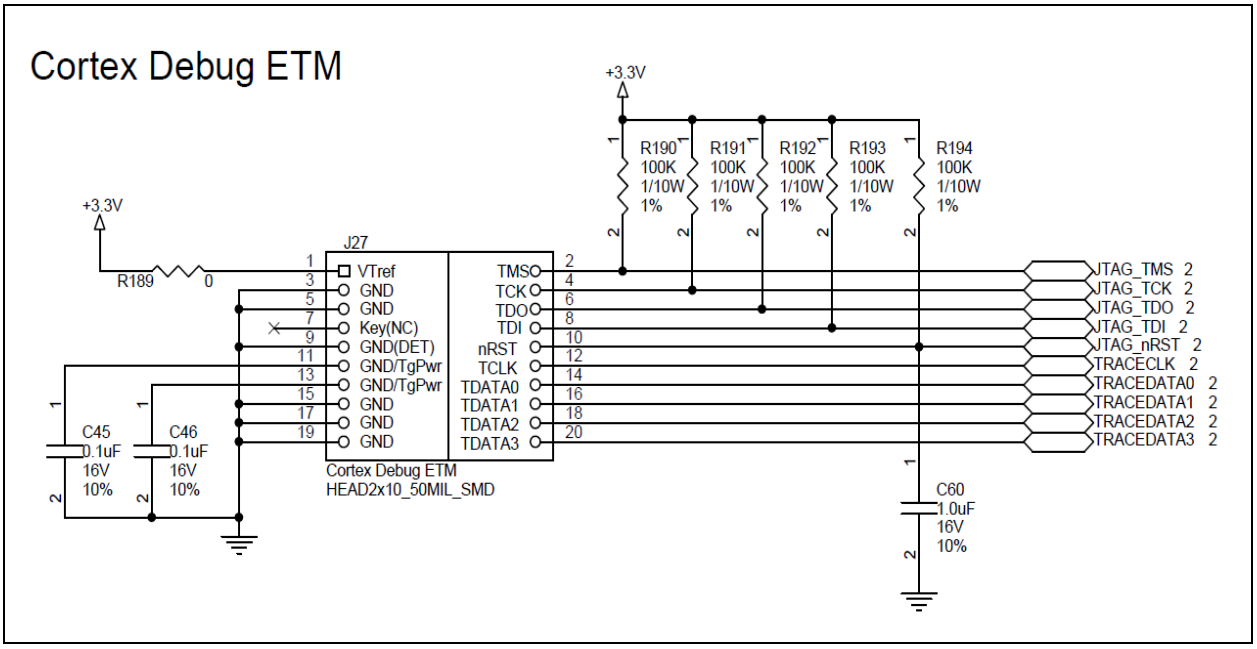
To use the trace support functionalities, the additional signals are required on the motherboard side; these are described in Table 3-3 and illustrated in FIGURE 3-3: 20-Pin cortex debug with trace support (0.05”) Connector on page 27.

TABLE 3-3: MEC170X JTAG PINS TO SUPPORT TRACE FUNCTIONS

Name	JTAG Cable Connection
TRACEDAT0	ARM Embedded Trace Macro Data 0
TRACEDAT1	ARM Embedded Trace Macro Data 1
TRACEDAT2	ARM Embedded Trace Macro Data 2
TRACEDAT3	ARM Embedded Trace Macro Data 3
TRACECLK	ARM Embedded Trace Macro Data Clock

The 20 pin connector is a Samtec FTSH-110-01 with pin 7 removed.

FIGURE 3-3: 20-PIN CORTEX DEBUG WITH TRACE SUPPORT (0.05”) CONNECTOR



3.4 JTAG Internal Pull-Up

The firmware can select which debug pins to enable the internal pull-high. Default is disabled. Please see the MEC170x Data Sheet DEBUG ENABLE REGISTER (4000_FC20h) for more information.

3.5 JTAG Reset

When the JTAG_RST# pin is not asserted (logic'1'), the JTAG_TDI, JTAG_TDO, JTAG_TCK, JTAG_TMS signal functions in the JTAG interface are unconditionally routed to the JTAG interface; the Pin Control register for these pins has no effect. When the JTAG_RST# pin is asserted (logic'0'), the JTAG_TDI, JTAG_TDO, JTAG_TCK, JTAG_TMS signal functions in the JTAG interface are not routed to the interface and the Pin Control Register for these pins controls the muxing. The pin control registers cannot route the JTAG interface to the pins. The system board designer should terminate this pin in all functional states using jumpers, pullup or pulldown resistors, and so forth.

JTAG registers are set to their initial values by the assertion of the JTAG_RST# pin. The JTAG_RST# pin must be held low while the MEC170x devices are powering up so the registers can be set to their proper default values. If JTAG_RST# is high during power up, the JTAG registers may be set to unpredictable values. This can trigger unwanted test modes and the system may not run correctly. As a result, the JTAG_RST# pin must be held low for at least 5.00 msec when applying VTR power.

Note:	For more details on the JTAG_RST# pin, in particular JTAG_RST# functionality with respect to VTR power up events, as well as RESETI# reset input pin transitions, see the JTAG section in the MEC170x Data Sheet.

The minimum required JTAG signals as shown in Table 3-1 does not include the JTAG_RST# signal. There are several options to handle the absence of this pin as followed:

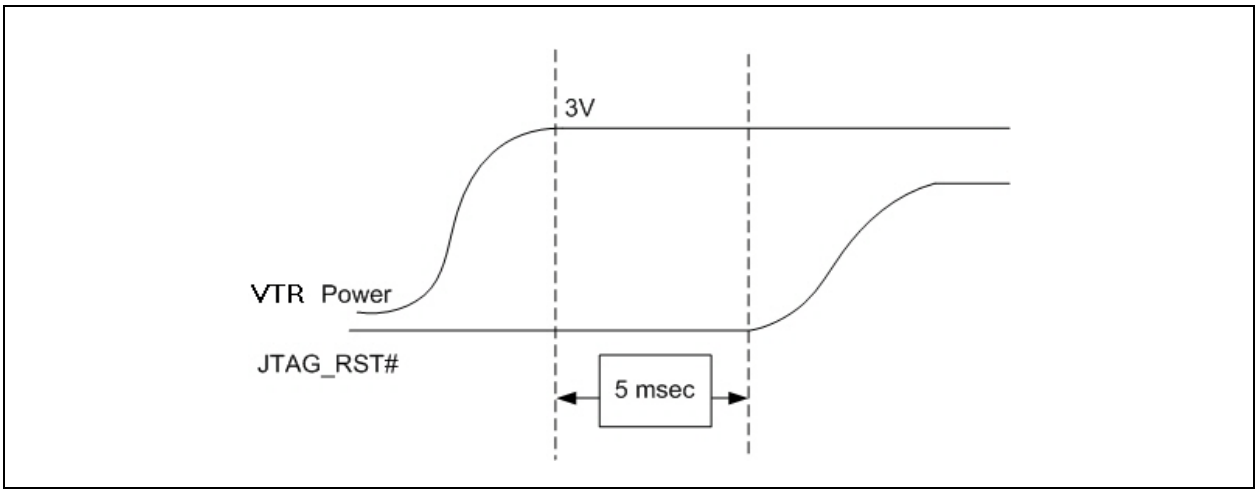
- Production Mode with JTAG Port Disable:
  - Hold the JTAG_RST# pin low with pulldown resistor to disable the JTAG port. Add a pullup resistor option (do not populate) for potential failure analysis to allow use of the JTAG interface. In this case, the JTAG_RST# pin must be manually held low at least 5.00 msec on power up.
- Production Mode with JTAG Port Enable:
  - Add a jumper to hold the JTAG_RST# line low during power up, then remove the jumper in order to ensure that it meets the 5.00 msec timing requirement.

Optionally, put in hardware Resistor-Capacitor (RC) circuitry to force the JTAG_RST# signal low for at least 5.00 msec. For example:

1. Use a MEC170x EVB with external power supply which shows the rise time less than 100µs.
2. RC = 100K ohms resistor pullup to VTR and 1µF capacitor.
3. The rising timing of VTR related to the JTAG_RST# signal is shown in Figure 3-4; the falling time should be a reverse of the rising time.

Note:	The RC values need to be changed in order to compensate for the power supply time to ensure a 5.00 msec reset pulse, measured from VTR = 3.3V to JTAG_RST# = 0.8V.

FIGURE 3-4: VTR VS. JTAG RISING TIME



APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002014C (06-14-21)	Section 2.16, "Glitch Protection Pins" and Section 2.17, "Glitch on ResetI#"	Added sections.
DS00002014B (03-09-18)	Section 2.7, "ADC Input Layout Requirements for Regular Sampling"	Section modified, Figure 2-3, "ADC Input Low Pass Filter" updated.
	Added Section 2.15, "MEC170x Shared SPI Flash Isolation Requirement".	
DS00002014A (11-30-15)	Document Release	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable." Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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China - Guangzhou
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China - Hong Kong SAR
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China - Nanjing
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China - Xian
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China - Xiamen
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China - Zhuhai
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India - New Delhi
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India - Pune
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Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
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Korea - Daegu
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Korea - Seoul
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Malaysia - Kuala Lumpur
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Malaysia - Penang
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Philippines - Manila
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Singapore
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Taiwan - Hsin Chu
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Taiwan - Kaohsiung
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Taiwan - Taipei
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Thailand - Bangkok
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Vietnam - Ho Chi Minh
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EUROPE

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Finland - Espoo
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Germany - Karlsruhe
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Germany - Rosenheim
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Israel - Ra'anana
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Italy - Milan
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Italy - Padova
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Netherlands - Drunen
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Norway - Trondheim
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Spain - Madrid
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Sweden - Gothenberg
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Sweden - Stockholm
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UK - Wokingham
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