REV	CHANGE DESCRIPTION	NAME	DATE
A	Release		5-16-12
B	Added Maximum Input Level High Value For Clock Input		12-19-12

DOCUMENT DESCRIPTION

Schematic Checklist for the LAN89530, 56-pin QFN Package

SMSC
80 Arkay Drive
Hauppauge, New York 11788

Document Number	Revision
SC471238	B

Schematic Checklist for LAN89530

Information Particular for the 56-pin QFN Package

LAN89530 QFN Phy Interface:

1. TXP (pin 3); This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. TXN (pin 2); This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. RXP (pin 6); This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. RXN (pin 5); This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.

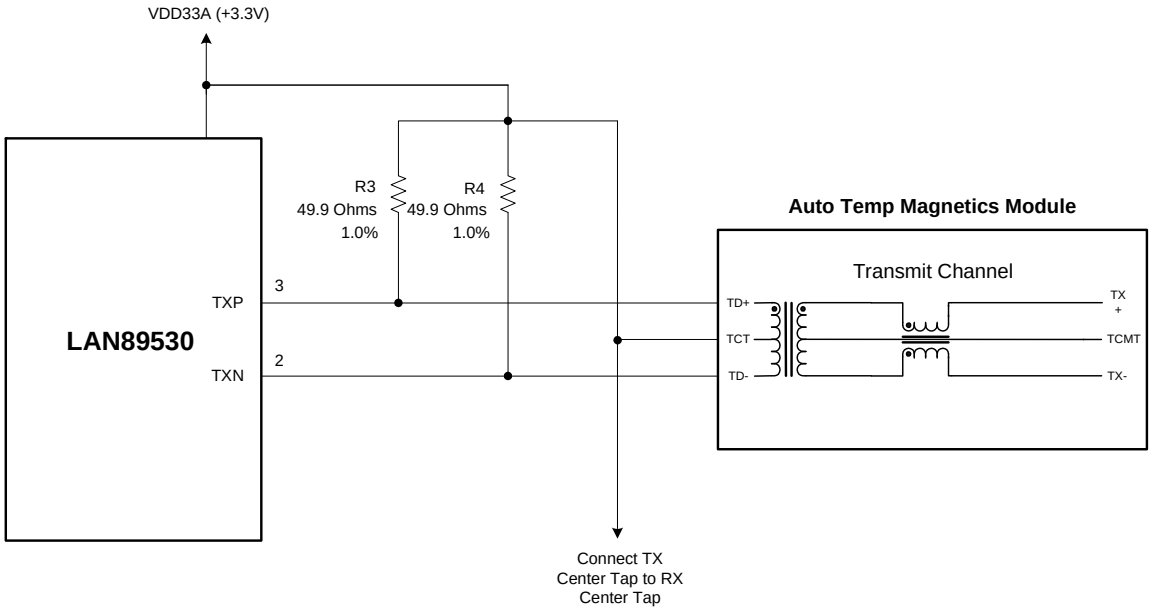


Figure 1 – Transmit Channel Connections and Terminations

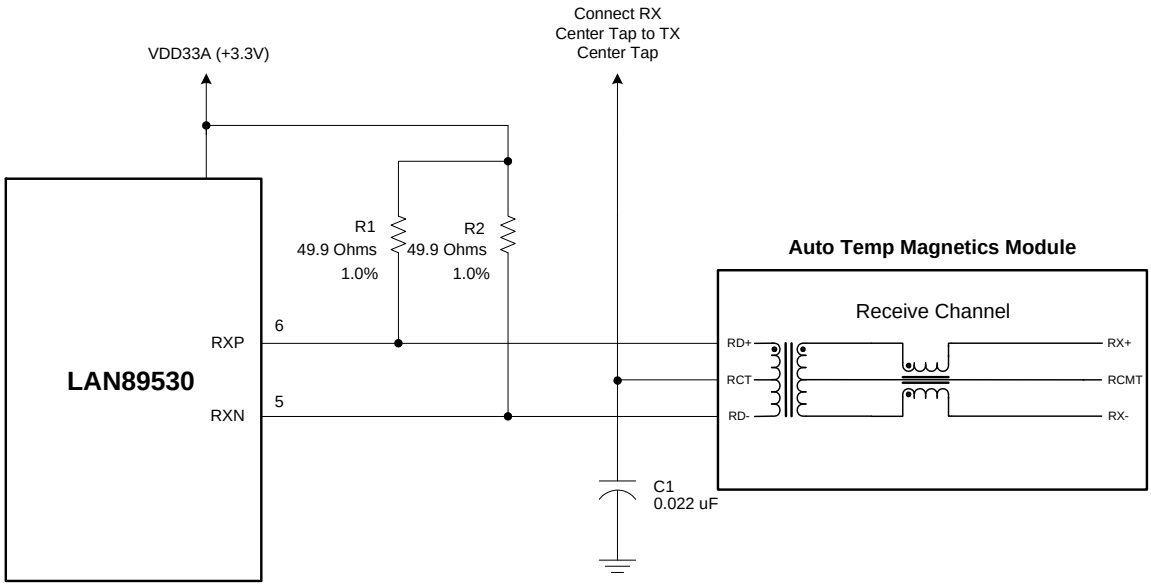


Figure 2 - Receive Channel Connections and Terminations

LAN89530 QFN Magnetics:

1. The center tap connection on the LAN89530 side for the transmit channel must be connected to VDDA (created from +3.3V) directly. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN89530 side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground.

5. Only one 1000 ρF, 2KV capacitor ($C_{magterm}$) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXP (pin 3) of the LAN89530 QFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TXN (pin 2) of the LAN89530 QFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to RXP (pin 6) of the LAN89530 QFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to RXN (pin 5) of the LAN89530 QFN.

10. When using the SMSC LAN89530 in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required.

11. In order to guarantee IEEE / AEC-Q100 compliancy over the entire temperature range of operation, the magnetics used in conjunction with the LAN89530 must be rated for Automotive Temperature use.

RJ45 Connector:

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 ρF, 2KV capacitor (C_{rjterm}). There are two methods of accomplishing this:

    a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 ρF, 2KV capacitor (C_{rjterm}).

    b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 ρF, 2KV capacitor (C_{rjterm}) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.

+3.3V Power Supply Connections:

1. The digital supply (VDD33IO) pins on the LAN89530 QFN are 25, 35, 48, 51 & 52. They require a connection to +3.3V.

2. Each power pin should have one .01 μF (or smaller) capacitor to decouple the LAN89530. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33A) pins on the LAN89530 QFN are 4, 9 & 15. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD33A pin should have one .01 μF (or smaller) capacitor to decouple the LAN89530. The capacitor size should be SMD_0603 or smaller.

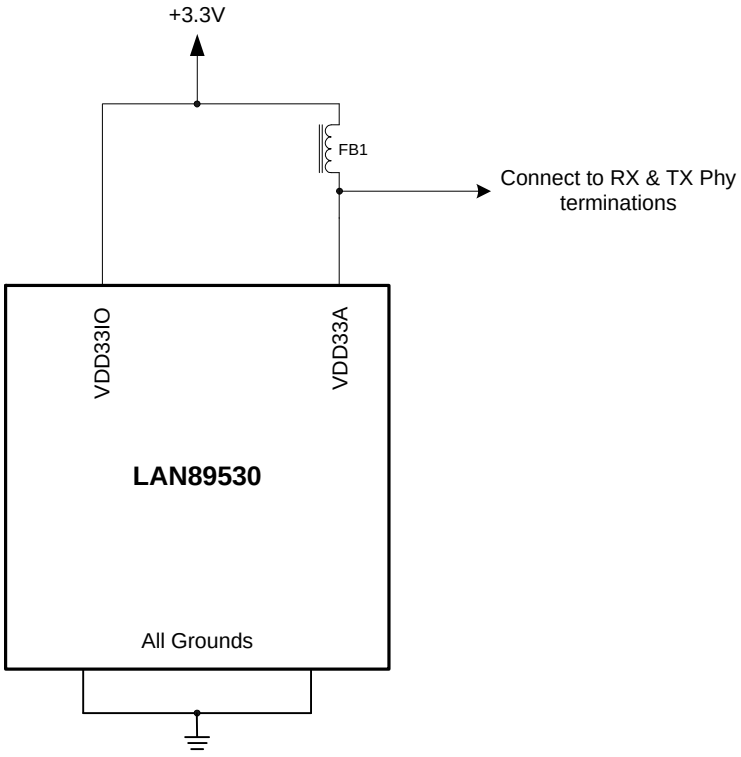


Figure 3 - +3.3V Power Supply Connections

VDD12CORE:

1. VDD12CORE (pins 21 & 50), these two pins are used to provide bypassing for the +1.2V core regulator. Each pin requires a 0.01 μF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 50 requires a bulk capacitor placed as close as possible to pin 50. The bulk capacitor must have a value of at least 1.0 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.2V supply is for internal logic only and LAN89530 use only. **Do Not** power other external circuits or devices with this supply.

2. VDD12PLL (pin 10), this pin supplies power for the core PLL. This pin must be connected to VDD12CORE through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

3. The VDD12PLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN89530. The capacitor size should be SMD_0603 or smaller.

4. VDD12USBPLL (pin 17), this pin supplies power for the USB PLL. This pin must be connected to VDD12CORE through a second ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

5. The VDD12USBPLL pin should have one .01 μF (or smaller) capacitor to decouple the LAN89530. The capacitor size should be SMD_0603 or smaller.

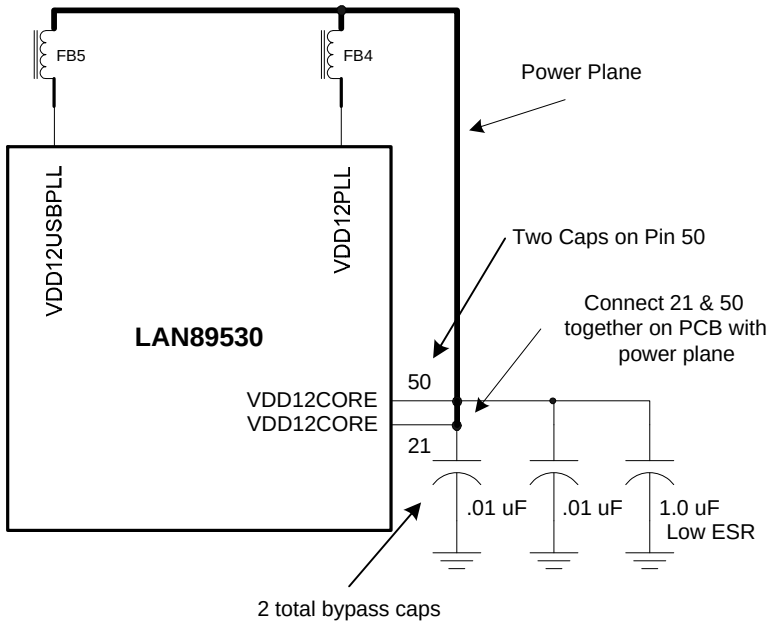


Figure 4 - LAN89530 +1.2V Power Connections

Ground Connections:

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN89530 QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN89530 must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

Crystal Connections:

1. A 25.000 MHz crystal must be used with the LAN89530 QFN. For exact specifications and tolerances refer to the latest revision LAN89530 data sheet.

2. XI (pin 18) on the LAN89530 QFN is the clock circuit input. This pin requires a 15 – 33 ρF capacitor to digital ground. One side of the crystal connects to this pin.

3. XO (pin 19) on the LAN89530 QFN is the clock circuit output. This pin requires a matching 15 – 33 ρF capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the capacitor values are system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, the additional external 1.0M Ω resistor across the crystal is no longer required. The necessary resistance has been designed-in internally on the LAN89530 QFN.

6. In order to guarantee IEEE compliancy over the entire temperature range of operation, the crystal / oscillator used in conjunction with the LAN89530 must be rated for Automotive Temperature use.

7. For single-ended clock applications, the maximum input voltage level high for the clock is +1.26 volts.

EEPROM Interface:

1. EECS (pin 30) on the LAN89530 QFN connects to the external EEPROM's CS pin.

2. EECLK (pin 29) on the LAN89530 QFN connects to the external EEPROM's serial clock pin.

3. EEDI (pin 32) on the LAN89530 QFN connects to the external EEPROM's Data Out pin.

4. EEDO (pin 31) on the LAN89530 QFN connects to the external EEPROM's Data In pin.

5. Be sure to select a 3-wire style 2K/4K EEPROM that is organized for 256/512 x 8-bit operation. 1K EEPROMs that are organized for 128 x 8-bit operation are not supported.

6. In order to guarantee IEEE compliancy over the entire temperature range of operation, the EEPROM used in conjunction with the LAN89530 must be rated for Automotive Temperature use.

EXRES Resistor:

1. EXRES (pin 8) on the LAN89530 QFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.

USBRBIAS Resistor:

1. USBRBIAS (pin 16) on the LAN89530 QFN should connect to digital ground through a 12.0K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded USB Physical device.

Required External Pull-ups/Pull-downs:

1. GPIO0 (pin 46) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

2. GPIO1 (pin 23) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

3. GPIO2 (pin 22) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

4. GPIO3 (pin 45) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

5. GPIO4 (pin 56) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

6. GPIO5 (pin 55) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

7. GPIO6 (pin 54) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

8. GPIO7 (pin 53) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

9. GPIO8 (pin 26) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

10. GPIO9 (pin 27) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

11. GPIO10 (pin 28) A pull-up resistor would be required if this pin is programmed as an Open Drain Output.

MII Interface:

1. When utilizing either an external MII Phy or an MII Connector, the following table indicates the proper connections for the 18 signals.

From:	Connects To:	
LAN89530 QFN	**MII Physical Device**	**MII Connector**
RXD0 (pin 36)	RXD<0>	RXD<0> (contact 7)
RXD1 (pin 38)	RXD<1>	RXD<1> (contact 6)
RXD2 (pin 39)	RXD<2>	RXD<2> (contact 5)
RXD3 (pin 40)	RXD<3>	RXD<3> (contact 4)
RX_DV (pin 42)	RX_DV	RX_DV (contact 8)
RX_ER (pin 44)	RX_ER	RX_ER (contact 10)
RX_CLK (pin 41)	RX_CLK	RX_CLK (contact 9)
TX_ER (pin14)	TX_ER	TX_ER (contact 11)
TXD0 (pin 56)	TXD<0>	TXD<0> (contact 14)
TXD1 (pin 55)	TXD<1>	TXD<1> (contact 15)
TXD2 (pin 54)	TXD<2>	TXD<2> (contact 16)
TXD3 (pin 53)	TXD<3>	TXD<3> (contact 17)
TX_EN (pin 43)	TX_EN	TX_EN (contact 13)
TX_CLK (pin 47)	TX_CLK	TX_CLK (contact 12)
CRS (pin 45)	CRS	CRS (contact 19)
COL (pin 46)	COL	COL (contact 18)
MDIO (pin 23)	MDIO	MDIO (contact 2)
MDC (pin 22)	MDC	MDC (contact 3)

2. If the MII interface is not used by the system, do not terminate on the board level. These pins have the proper internal terminations and should be left as no-connects.

USB Interface:

1. USBDP (pin 12), this pin is the USB channel positive data pin. This pin should be connected directly to pin 3 (D+) on a standard 4-pin, upstream USB connector (Type “B”).

2. USBDM (pin 11), this pin is the USB channel negative data pin. This pin should be connected directly to pin 2 (D-) on a standard 4-pin, upstream USB connector (Type “B”).

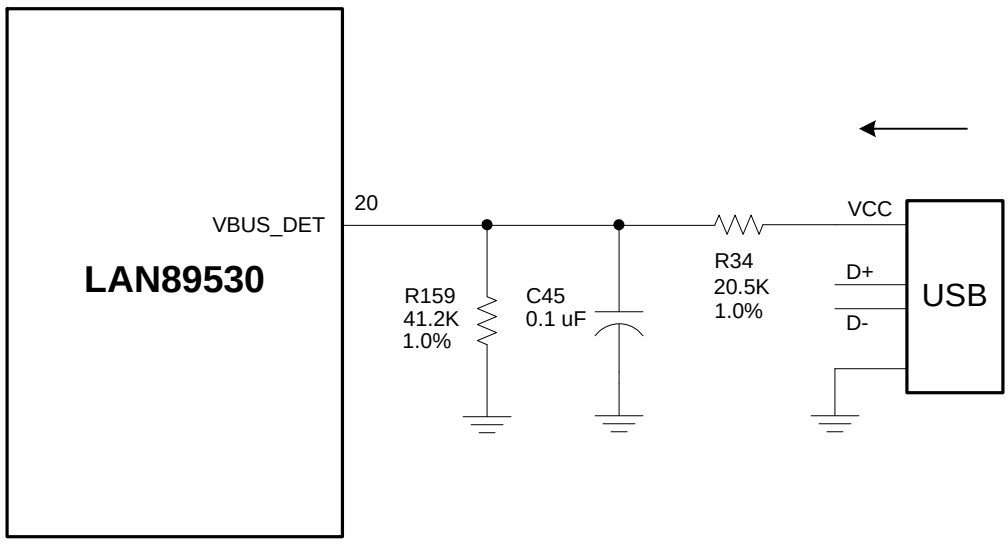
3. Typical Bus Powered applications will connect pin 1 (VCC) on a standard 4-pin, upstream USB connector (Type “B”) directly to a 2000 mA ferrite bead. This ferrite bead will in turn feed a LDO +5.0V-to-+3.3V voltage regulator to power the LAN89530.

4. We recommend no bulk capacitance be placed on pin 1 (VCC) of the USB connector in Bus Powered applications. On the voltage regulator side of the ferrite bead, we recommend limiting the bulk capacitance to 4.7 uF. This should satisfy the 10.0 uF total capacitance to limit in-rush current as required by the USB specification.

5. Typical applications will connect pin 4 (Ground) on a standard 4-pin, upstream USB connector (Type “B”) directly to digital ground.

6. The two metal shield connections on the USB connector should be connected directly to a suitable chassis ground plane.

7. VBUS_DET (pin 20), this pin detects the state of the supplied downstream power. This pin must be tied to VDD33IO when operating in Bus-Powered mode. When using the LAN89530 in Self-Powered mode, this pin should be tied to the USB power through the recommended circuit below. This pin has a weak internal pull-down.



Self-Powered Mode Circuitry

Configuration Straps:

1. All configuration strap values are latched in on Power-On Reset and System Reset. For more detailed information of each bit and functionality, consult the latest version of the LAN89530 data sheet.

2. PWR_SEL (pin 29), this pin determines the default power setting when no EEPROM is present. This strap is overridden by the EEPROM. The settings are as follows:

   0 = LAN89530 is bus powered
   1 = LAN89530 is self powered

   See the latest version of the LAN89530 data sheet for complete details. This pin has a weak internal pull-down and can be driven high with an external 10.0K Ω resistor to VDD33IO.

3. AUTOMDIX_EN (pin 31), this pin determines the default Auto MDIX setting. The settings are as follows:

   0 = Auto MDIX is disabled
   1 = Auto MDIX is enabled

   See the latest version of the LAN89530 data sheet for complete details. This pin has a weak internal pull-up and can be driven low with an external 10.0K Ω resistor to digital ground.

4. PORT_SWAP (pin 54), this pin determines the mapping of the USB +/- pins. The settings are as follows:

   0 = USBDP maps to USB D+ & USBDM maps to USB D-
   1 = USBDP maps to USB D- & USBDM maps to USB D+

   See the latest version of the LAN89530 data sheet for complete details. This pin has a weak internal pull-down and can be driven high with an external 10.0K Ω resistor to VDD33IO.

5. PHY_SEL (pin 34), this pin determines whether the internal Ethernet Phy is enabled or the LAN89530 will be used with an external Ethernet Phy. The settings are as follows:

   0 = Internal Phy is used
   1 = External Phy is used

   See the latest version of the LAN89530 data sheet for complete details. This pin has a weak internal pull-down and can be driven high with an external 10.0K Ω resistor to VDD33IO.

6. RMT_WKP (pin 55), this pin determines the default descriptor values for remote wakeup functionality. This strap is overridden by the EEPROM. The settings are as follows:

   0 = Remote wakeup is not supported
   1 = Remote wakeup is supported

   See the latest version of the LAN89530 data sheet for complete details. This pin has a weak internal pull-down and can be driven high with an external 10.0K Ω resistor to VDD33IO.

7. EEP_DISABLE (pin 56), this pin disables autoloading of the EEPROM contents. The assertion of this strap does not prevent register access to the EEPROM. The settings are as follows:

   0 = EEPROM is recognized if present
   1 = EEPROM is not recognized even if it is present

   See the latest version of the LAN89530 data sheet for complete details. This pin has a weak internal pull-down and can be driven high with an external 10.0K Ω resistor to VDD33IO.

8. CORE_REG_ENABLE (pin 49), this pin enables/disables the internal core logic voltage regulator. When tied low to VSS, the internal core regulator is disabled and +1.2V must be supplied to the device by an external source.

   When tied high to +3.3V, the internal core regulator is enabled.

Miscellaneous:

1. There is one No-Connect pin on the LAN89530. It is very important that this pin (pin 7) remain a no-connect.

2. nRESET (pin 24), this pin is an active-low reset input. This signal resets all logic and registers within the LAN89530. This signal is pulled high with a weak internal pull-up resistor.

3. nPHY_INT (pin 1), this pin is configured as either an output or input depending upon the Ethernet Phy configuration. When using the internal Ethernet Phy, this pin is configured as an output and indicates the Phy interrupt status. This signal is an active low indication.

   When using an external Ethernet Phy with the LAN89530, this pin is configured as an input to the internal MAC and indicates the Phy interrupt status. This signal is an active low indication. When in this mode, this input is configured with a weak internal pull-up.

4. nPHY_RST (pin 37), this pin is configured as an output when the LAN89530 is in external Ethernet Phy mode. This signal is an active low indication. This signal should be routed to the nRESET input of the external Phy to reset all registers.

5. nFDX_LED (pin 26), nLNKA_LED (pin 27) & nSPD_LED (pin 28), can be programmed via register settings to display various Ethernet activity such as Speed, Link & Duplex Status. See the latest version of the LAN89530 data sheet for complete details. These pins have weak internal pull-ups.

6. The LAN89530 has an IEEE 1149.1 compliant JTAG Boundary Scan interface. This test interface can be utilized to accomplish board level testing to ensure system functionality and board manufacturability. For details, see the LAN89530 data sheet.

7. TEST1 (pin 33), this pin must be tied directly to VSS in order to ensure proper operation.

8. TEST2 (pin 13), this pin must be tied directly to +3.3V in order to ensure proper operation.

9. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

10. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

11. In order to guarantee IEEE / AEC-Q100 compliancy over the entire temperature range of operation, all components used in the customer's application must be rated for Automotive Temperature use. Processors, crystals, oscillators, magnetics and all integrated circuits must be rated properly to avoid operational inconsistencies.

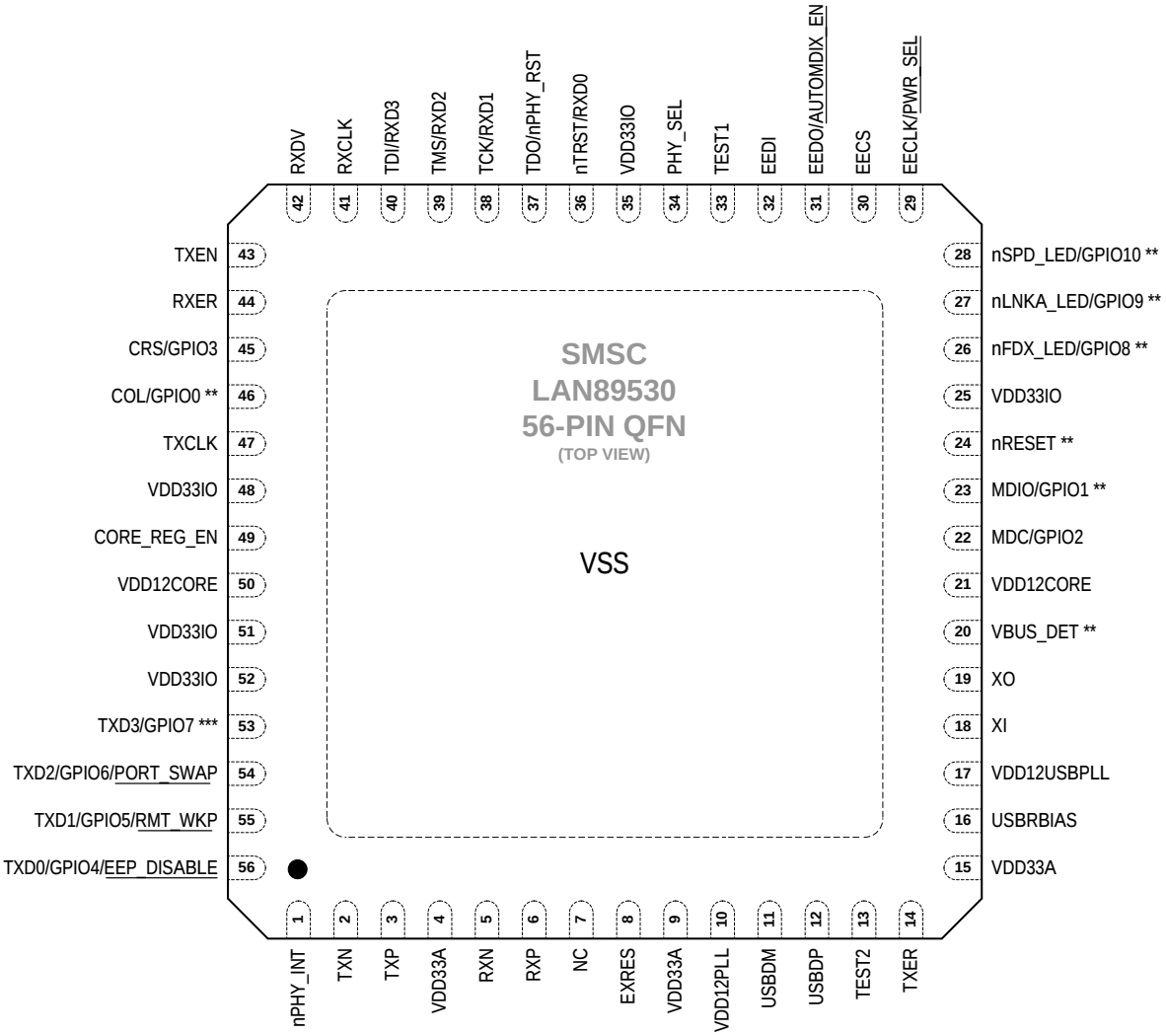
LAN89530 QFN QuickCheck Pinout Table:

Use the following table to check the LAN89530 QFN shape in your schematic.

LAN89530 QFN			
Pin No.	**Pin Name**	**Pin No.**	**Pin Name**
1	nPHY_INT	29	EECLK / PWR_SEL
2	TXN	30	EECS
3	TXP	31	EEDO / AUTOMDIX_EN
4	VDD33A	32	EEDI
5	RXN	33	TEST1
6	RXP	34	PHY_SEL
7	NC	35	VDD33IO
8	EXRES	36	nTRST / RXD0
9	VDD33A	37	TDO / nPHY_RST
10	VDD12PLL	38	TCK / RXD1
11	USBDM	39	TMS / RXD2
12	USBDP	40	TDI / RXD3
13	TEST2	41	RXCLK
14	TXER	42	RXDV
15	VDD33A	43	TXEN
16	USBRBIAS	44	RXER
17	VDD12USBPLL	45	CRS / GPIO3
18	XI	46	COL / GPIO0
19	XO	47	TXCLK
20	VBUS_DET	48	VDD33IO
21	VDD12CORE	49	CORE_REG_EN
22	MDC / GPIO2	50	VDD12CORE
23	MDIO / GPIO1	51	VDD33IO
24	nRESET	52	VDD33IO
25	VDD33IO	53	TXD3 / GPIO7
26	nFDX_LED / GPIO8	54	TXD2 / GPIO6 / PORT_SWAP
27	nLNKA_LED / GPIO9	55	TXD1 / GPIO5 / RMT_WKP
28	nSPD_LED / GPIO10	56	TXD0 / GPIO4 / EEP_DISABLE
57		**EDP Ground Connection Exposed Die Paddle Ground Pad on Bottom of Package**	

Notes:

LAN89530 QFN Package Drawing:



Reference Material:

1. SMSC LAN89530 Data Sheet; check web site for latest revision.
2. SMSC LAN89530 CEB Schematic, Assembly No. 6663 ; check web site for latest revision.
3. SMSC LAN89530 CEB PCB, Assembly No. 6663 ; order PCB from web site.
4. SMSC LAN89530 CEB PCB Bill of Materials, Assembly No. 6663 ; check web site for latest revision.
5. CEB stands for Customer Evaluation Board.
6. SMSC LAN89530 Reference Design, check web site for latest revision.
7. SMSC Reference Designs are schematics only; there are no associated PCBs.
8. For Qualified / Suggested Magnetics, use these two links to the SMSC LANCheck website:

https://www2.smsc.com/mkt/web_lancheck.nsf/MagList?OpenForm

https://www2.smsc.com/mkt/web_lancheck.nsf/MagCheck?OpenForm