AT91SAM7S64 USB Certification

1. Introduction

This Application Note describes the USB certification process for the AT91SAM7S64 ARM® Thumb®-based microcontroller that contains a USB V2.0 Full Speed Device. It describes the full USB peripheral environment required for USB-IF compliancy.

The following table gives the references of the documents and their denominations in this document.

Document Reference	Denomination
Atmel lit° 6112	AT91SAM7S-EK Evaluation Board User Guide
Atmel lit° 6070B (1) Atmel lit° 6175	AT91SAM7S64
Atmel lit° 6193	Mass Storage Demo User Guide
Atmel lit° 6194	Mass Storage Module Documentation
usb_ms_overview_1.2	Mass Storage Overview (from www.usb.org)
usbmassbulk_10	Mass Storage Bulk Only (from www.usb.org)
compliance tools_usb-if reps-2	USB-IF Compliance Program Web Tools (from www.usb.org)
compchkperisil080205.pdf	USB Compliance Checklist, Peripheral Silicon (from www.usb.org)

Notes: 1. This document is no longer available but has been replaced by Atmel lit° 6175, AT91SAM7S256/128/64/321/32 datasheet.

AT91
ARM Thumb
Microcontrollers

Application
Note

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2. USB Certification

Information used in this chapter is available on the USB web site

http://www.usb.org/home

2.1 The Purpose of USB Certification

The Universal Serial Bus (USB) is a huge success! This presents a great market opportunity for USB vendors. In order to realize this opportunity, USB products must continue to enhance the consumer's experience through high quality and ease of use. That's why **USB Implementers Forum, Inc.** introduced a trademark-protected logo for use with qualified products. To qualify for the right to display the certified USB logo in conjunction with a product, the product must pass USB-IF compliance testing for product quality.

Figure 2-1. USB Full Speed/Low Speed Logo

Each type of USB product requires specific testing to get on the USB Integrator's List. End user products (peripherals), have to fill the USB Compliance Checklist. For instance, peripherals which require identification of the receptacles, cable assembly or, if the cable is captive, the A connector, and manufacturer and model identifier of the USB Silicon used in the peripheral.

If the silicon used in the peripheral is **not** listed on the USB Integrator's List, then a Peripheral Silicon Checklist covering this peripheral's USB silicon must be provided.

Atmel has already submitted the AT91SAM7S64 and this product is now referenced in the USB integrator list:

```
AT91SAM7S64
Revision G
TID 40000036
```

To pass the peripheral silicon testing, it was necessary for Atmel to construct a final product based on the AT91SAM7S64 and test that product as anyone using the AT91SAM7S64 would do. The final product application is a mass-storage based application using the AT91SAM7S-EK board which has been modified so that the final product can be bus powered.

2.2 Where to Apply for USB Certification

The USB-IF logos may be used only in conjunction with products that have passed USB-IF compliance testing and are currently on the USB Integrator's List. This requires that the company be assigned a USB vendor ID number. Atmel's USB vendor ID is 03EBh.

There is a logo administration fee of US $1500 for non-USB-IF members, to be submitted with the signed agreement and a Vendor ID form:

http://www.usb.org/developers/vendor/VID_ONLY_Form.pdf

if your company does not already have a Vendor ID. The fee is waived for USB-IF members. Registration to the USB-IF community can be done on-line:

There are two mechanisms for testing products to get them on the USB Integrator's List. You can participate in the USB-IF Sponsored Compliance Workshops or contact one of the Independent Test Labs.

A complete list of test labs and contact information is available at:

http//www.usb.org/developers/compliance

To qualify the AT91SAM7S64 product, Atmel has been working with the following lab:

```
Professional Multimedia Testing Centre (PMTC)
Johan Craeybeckx
Wetenschapspark 5,
3590 Diepenbeek
Belgium
Tel: +32 11 30 36 53
Fax: +32 11 30 36 90
Email: johan@pimc.be
URL: www.pmtctest.com
```

Companies should contact the lab of their choice directly for pricing and scheduling. To submit a testing request to the lab of choice, follow the instructions below:

- Go to the "Compliance Member Tools" section of the Web site:

  http://www.usb.org/kcompliance/members
- Click on "Register a Product for testing"
- Select the type of the product to submit for testing, the test lab of choice and enter the product information completely. The product submission will be in the "New" state. The selected test lab will receive email notification of the request. Once the test lab reviews and accepts the testing request, the product's status will be "Accepted for Testing".

2.3 Peripheral Test Requirements

The following must be successfully completed for Peripherals:

- Electrical Tests
- Interoperability Tests
- Functional Tests
- Submission of Completed Peripheral Checklist

Additional information at:

http://www.usb.org/developers/docs/USB-IFTestProc1_3.pdf

3. AT91SAM7S64 Test Product Description

3.1 System Description

To pass the peripheral silicon testing, Atmel built a final product based on the AT91SAM7S64.The final product application is a mass-storage based application using the AT91SAM7S-EK board which has been modified so that the final product can be bus powered.

Once the AT91SAM7-EK board is connected to the host PC, a new disk drive appears in on screen. The Internal Flash of the AT91SAM7S64 product appears as a new flash drive. Through Windows®OS, applications can perform file transfer with the target internal flash. As the peripheral enumerates as a standard mass-storage device (please refer to the USB Mass-storage class specification), this application does not require any Windows 2000 drivers.

The mass-storage source code is delivered by Atmel on-demand. Very few modifications have been done. These modifications concern the configuration of the microcontroller in low power mode.

The AT91SAM7-EK board has been modified to match the power constraints of a bus-powered peripheral.

3.2 Main Constraints

The tested peripheral should match all requirements specified in the USB Specification V2.0. Only a few constraints with immediate consequences on application programing and board design are highlighted here.

3.2.1 Power Constraints

All devices must support the suspend state. Devices can go into the suspend state from any powered state.

The device power allocation into any powered state without negociation can not exceed (I_{CCLPF}) 100 mA. The device power allocation into the suspend state can not exceed (I_{CCSL}) 500 µA. Refer to table 7.7 in the USB V2.0 specification. Device power consumption is that of the AT91SAM7S-EK board consumption. It includes the AT91SAM7S64, USB pull-up, regulators and all powered discrete parts on the board.

While in the suspend state, a device may briefly draw more than the average current. The amplitude of the current spike cannot exceed the device power allocation 100 mA (or 500 mA). A maximum of 1.0 second is allowed for an averaging interval.

3.2.2 Clock Constraints

The full-speed data rate is nominally 12.000 Mb/s. For full-speed only functions, the required data-rate when transmitting (T_{FDRATE}) is 12.000 Mb/s 0.25% (2.500 ppm). The application firmware must configure clocks and PLL in order to match these requirements.

3.2.3 Timing Constraints

After connecting a peripheral to a host, the device has at least 100 ms after the detection of the pull-up by the host to configure and be able to answer host requests.

A peripheral begins the transition to the suspend state after it observes a constant Idle state on its upstream facing bus lines for more than 3.0 ms. The device must actually be suspended,

drawing only suspend current from the bus after no more than (T_{2SUSP}) 10 ms of bus inactivity on all its ports. Thus the application firmware has 7 ms to reduce power consumption of the board. Refer to Chapter 7.1.7.6 of the USB specification.

The host must provide a 10 ms resume recovery time (T_{RSMRCY}) during which it will not attempt to access any device connected to the affected (just-activated) bus segment. During this time the application firmware must restore clocks and software context.

3.3 AT91SAM7S-EK Certified Board Description

3.3.1 Hardware Description

Refer to the Atmel document “AT91SAM7S-EK Evaluation Board User Guide”, Atmel lit° 6112.

In order to reduce the power consumption of the AT91SAM7S-EK board, shown in Figure 3-1, the following components have been removed:

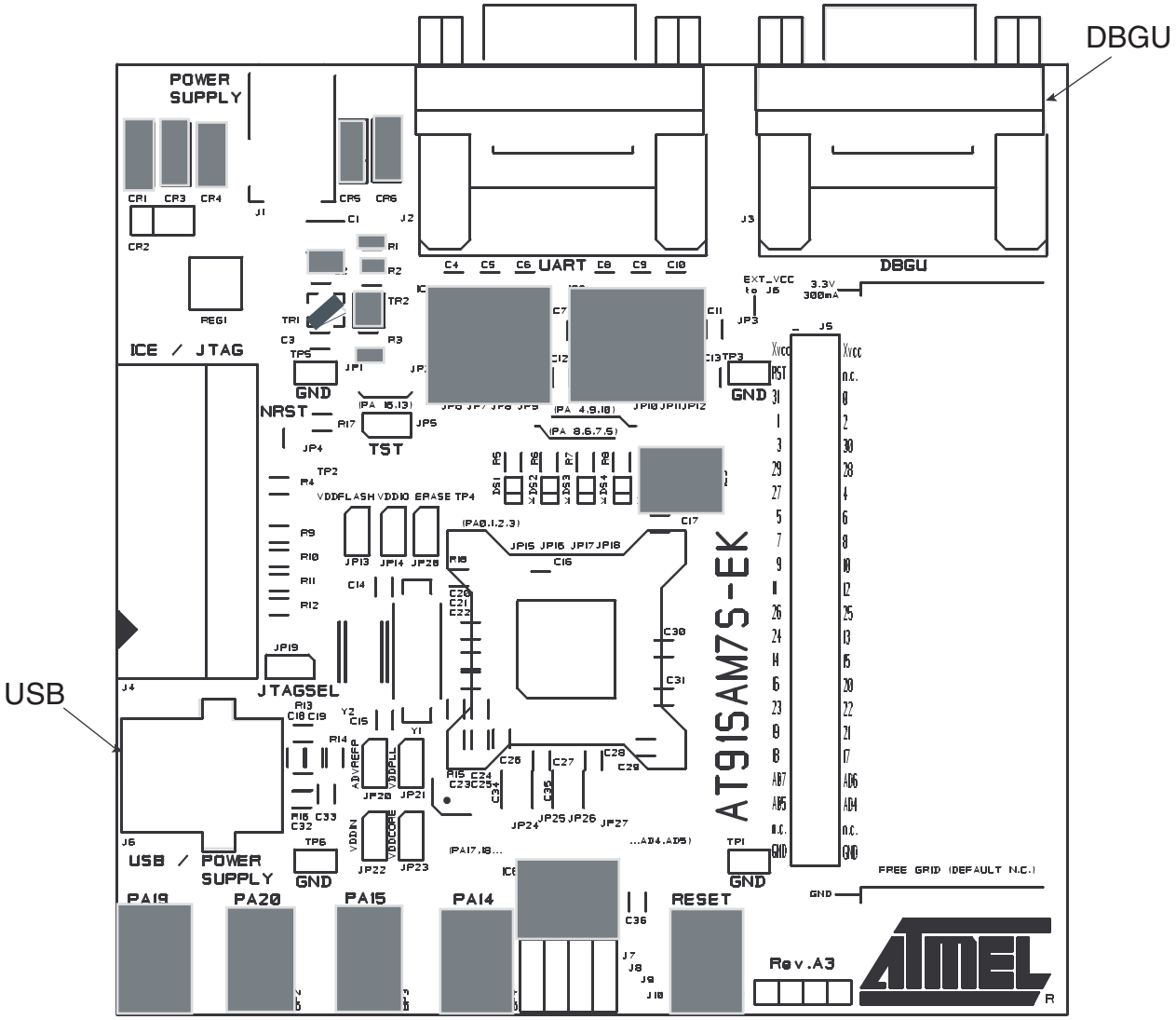
- the Atmel Crypto memory
- Four buffered analog inputs
- Four general-purpose LEDs and push buttons (for securing the IO of the chip).
- IC1, IC2, IC3, R1, R2, R3, TR1, TR2, C2, IC6, PA19, PA20, PA15, PA14, RESET,
- CR1, CR3, CR4, CR5, CR6.

In the place of TR1, a wire must be soldered between Drain (D) and Source (S). This maintains the pull-up on DP as always active and removes TR1 consumption.

The board regulator REG1 (KF33BDT) has been replaced by RP334. This reduces (few consumption for little power).

In this configuration, when the device is not in suspend mode, it drains 25 mA, in suspend mode, it drains 360 µA on USB VBUS.

Figure 3-1. AT91SAM7S-EK Board Modifications



3.3.2 Software Description

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Table 3-1. AT91SAM7S64 Software Configuration

Mode	PLL Configuration	MCK =
Default Address Configured	• Main Oscillator enabled (184242 kHz) • Voltage regulator of • USB transceiver enabled • PIO in output mode, pull-up disabled, forced to 1 • Code is running in Flash	MCK = 48.05 Mhz (0,11% error) USB bitrate: 11.97973 Mbps
Suspend	• PLL disabled • Main oscillator disabled • Voltage regulator in standby • USB transceiver disabled • Code is running in RAM	MCK = 32 kHz

PLL settings to generate 48.05 MHz from the 18.43 2 MHz oscillator are as follows:

```
AT91C_CKGR_DIV = 0x0E
AT91C_CKGR_PLLCOUNT = 28
AT91C_CKGR_MUL = 48
```

4. Appendix

The pages shown in the Appendix are scanned copies of the original documents as listed below.

USB Peripheral Compliance Checklist.

USB Certification Report for the AT91SAM7S64 Rev G

USB Compliance Checklist
Peripheral Silicon
(Excluding Hub Silicon)

For the 2.0 USB Specification
Checklist Version 1.08
December 18, 2001

USB Device Product Information

field	—all fields must be filled in—
Date	Jun 14, 2005
Vendor Name	ATMEL
Vendor Street Address	Zone Industrielle
Vendor City, State, Postal Code	ROUSSET 13106
Vendor Country	FRANCE
Vendor Phone Number	+33(0)4.42.53.90.00
Vendor Contact, Title	Support AT91
Vendor Email Address	AT91SUPPORT@ATMEL.COM
Product Name	AT91 SAM9S 64
Product Model Number	58814
Product Revision Level	
Test ID Number	
Manufacture, Model Identifier, and TID of peripheral used for testing	ATMEL, AT91 SAM9S-EK
Signature of Preparer	

Table of Contents

Revision History

version	changes	date
1.08	Delete TA4, covers data no longer in spec	2001.12.18
1.07	Delete B10	2001.11.28
1.06	Changes for 2.0	2001.10.5
1.05	revised FS6, LS5, RTA1, added FS7, LS6, fixed FS8, FS20	1999.8.19
1.04	added test ID field	1999.8.16
1.03	revised ST13, added LS6, FS7, FS8	1999.6.18
1.02	revised introduction, fixed μ, Ω, typos	1999.2.5
1.01	added preparer's signature and changed checklist contact info	1999.1.4
1.00	initial release: added contact info and some minor clarifications	1998.11.20
.95	first public review draft, released for Taipei USB Plugfest	1998.10.26

1 Introduction

This checklist helps designers of USB microcontrollers, transcievers, cores, or other ASICs for USB peripherals to asses their products' compliance with the Universal Serial Bus Specification, Revision 2.0. Unless explicitly stated otherwise, all references to the USB Specification refer to Revision 2.0.

This checklist is also used, in part, to qualify USB interface silicon for the USB-IF Integrators List. This document and other USB compliance tools, including USB Check, are available in the developers section of the USB-IF's website, http://www.usb.org/developers/. The compliance checklists are updated periodically, so developers should check for updates when starting new projects.

Section 5, Recommended Questions, contains questions covering areas not required by the USB Specification. Answering these questions is not a requirement for compliance with the Specification or acceptance to the Integrators List. However, vendors are strongly encouraged to take these questions into consideration when designing their products.

Questions or comments regarding the Integrators List, Compliance Workshop testing results, or checklist submissions should be sent to admin@usb.org. If you have questions regarding the checklist itself, feel it fails to adequately cover an aspect of the USB specification, have found an error, or would like to propose a question, please contact the USB-IF at checklists@usb.org.

1.1 General Notes and Glossary

- All voltages are referenced to the USB ground of the device being tested.
- Bit order is from left to right.

bitstream	A set of bits represented as NIBs or NZBs.
field	A particular group of bits represented as NIBs or NZBs. *E.g.* a SYNC field is KJKJKJKK in NIBs or 00000001 in NZBs.
NIB	NRZI bit. Represented as J, K and 0 (single ended 0).
NZB	NRZ bit. Represented as 1, 0 and S (single ended 0).
packet	The most frequently referenced data structure, built out of fields.
phase	of a transaction is made up of 0 or 1 packet e.g. token phase
sense	The relationship between D+ and D- voltages for J state on a USB connection. For full-speed, D+ > D-, for low-speed link D+ < D-.
stage	A set of one or more unidirectional transactions.
timeout period	The amount of time that an agent awaiting a response waits before invalidating the transaction.
target	Destination of a transaction., which could be a pipe in the host or an endpoint in a device.
transaction	The basic unit of unidirectional data transfer and a set of packets. For unidirectional endpoints (bulk, interrupt, isochronous) this is the final level of communication with protocol implications.
transfer	A unit of bi-directional data transfer built out of stages. It is used by only by control endpoints.
turnaround time	The time between an agent seeing the EOP for the previous packet and starting to drive the bus for a new packet. *I.e.*, the J period after the EOP as measured at the agent. This time also applies to the period between packets when the host is driving both packets.

2 Signals and Timing

ID	question	response	sections in spec
ST1	Is the data line crossover voltage between 1.3 and 2.0V?	yes no	7.1.2
ST2	Do all single ended receivers recognize 0.8V or below as a logic low?	yes no	7.1.4
ST3	Do all single-ended receivers recognize 2.0V or more as a logic high?	yes no	7.1.4
ST4	Do all differential receivers have an input sensitivity of at least 200mV between 0.8 and 2.5 volts common mode?	yes no	7.1.4
ST5	Is the device's pull up active only when V_{BUS} is 1.17V or more?	yes no	7.1.5
ST6	Is the input impedance of D+ and D-, without termination and pull up resistors, more than 300kΩ?	yes no	7.1.6
ST7	Does the device respond to a reset no sooner than 2.5µs and no later than 10ms after the SE0 begins, regardless of the SE0's position in a bitstream?	yes no	7.1.7.3
ST8	Is the device's reset recovery time less than 10ms?	yes no	7.1.7.3
ST9	At the end of reset is the device in the default state?	yes no	7.1.7.3 9.1.1
ST10	Does the device enter suspend if the bus is idle for 3ms or more?	yes no	7.1.7.4
ST11	Has the device's power consumption dropped to its suspended value after the hub's upstream bus segment has been idle for 10ms?	yes no	7.1.7.4
ST12	When suspended, does the device recognize any non-idle state on its upstream port, including a reset, as a resume signal?	yes no	7.1.7.5
ST13	Does the device recognize the end of resume signaling and return to the state it was in prior to suspend?	yes no	7.1.7.5
ST14	Is the device able to accept a SetAddress() request 10ms after resume is signaled?	yes no	7.1.7.5
ST15	Does the device complete its wakeup within 20ms?	yes no	7.1.7.5
ST16	Do active data line outputs drive to 2.8–3.6V with a 14.25kΩ load to ground?	yes no	7.3.2
ST17	Do active data line outputs drive to 0–0.3V with a 1.425kΩ load to 3.6V?	yes no	7.3.2

Note: the 1.17V threshold voltage for pull up activation is derived from a device using a resistor connected directly to V_{BUS}, assuming worst-case values for V_{BUS} (5.25V), pull up size (6.53kΩ, which holds Dx at 3.6V with a 5.25V V_{BUS}), pull down size (15.75kΩ), and single-ended receiver sensitivity (0.8V).

2.1 Low-Speed Ports

(applicable to any USB port which can operate at 1.5Mb/s)

LS1	Are data line rise times between 75ns and 300ns when driving into any single ended, capacitive load between 200 and 450pF?	yes no	7.1.2
LS2	Are data line fall times between 75ns and 300ns when driving into any single ended, capacitive load between 200 and 450pF?	yes no	7.1.2
LS3	Are the rise and fall times matched to within 20% for J→K transitions?	yes no	7.1.2
LS4	Are the rise and fall times matched to within 20% for K→J transitions?	yes no	7.1.2
LS5	Is a SE0 less than 210ns long ignored at all transitions in a bitstream?	yes no	7.1.4
LS6	Is a SE1 less than 100ns long ignored at all transitions in a bitstream?	yes no	
LS7	Does the device drive the J state at the end of an EOP for a full low-speed bit time?	yes no	7.1.7
LS8	Is the transmission data rate between 1.4775 and 1.5225Mb/s?	yes no	7.1.11
LS9	Is the differential driver jitter for consecutive transitions less than ±25ns?	yes no	7.1.13.1
LS10	Is the differential driver jitter for paired transitions less than ±10ns?	yes no	7.1.13.1
LS11	Is the EOP width between 1.25µs and 1.5µs at the transmitter?	yes no	7.1.13.2

LS12	Does the receiver accept an SE0 between 670ns and 1.76μs long, followed by a J, as an EOP?	yes	no	7.1.13.2
LS13	Does the receiver accept a packet whose first bit has been distorted by as much as ±25ns?	yes	no	7.1.14
LS14	Does the receiver accept a packet whose last bit has been lengthened by as much as 260ns (dribble bit)?	yes	no	7.1.14 7.1.9
LS15	Is the receiver data jitter tolerance at least ±141ns for consecutive transitions?	yes	no	7.1.15
LS16	Is the receiver jitter tolerance for paired transitions at least ±184ns?	yes	no	7.1.15
LS17	Is the device's turn-around time between two and 6.5 low-speed bit times, or 7.5 bit times if the device has a fixed cable?	yes	no	7.1.18
LS18	Is the time-out period 16–18 low-speed bit times?	yes	no	7.1.19
LS19	Is D- between 2.7 and 3.6V and D+ between 0.0 and 0.3V when the bus is idle?	yes	no	7.2.3

Note: the low-speed receiver jitter tolerances listed here do not apply to hosts and hubs. Consult section 7.1.15 for host and hub jitter requirements.

2.2 Full-Speed Ports

(applicable to any USB port which can operate at 12Mb/s)

FS1	With series termination resistors, does the device's source impedance remain in the shaded areas of Figure 7-3?	(yes)	no	7.1.1.1
FS2	Are data line rise times between 4.0 and 20ns when driving into a single-ended 50pF load?	(yes)	no	7.1.2
FS3	Are data line fall times between 4.0 and 20ns when driving into a single-ended 50pF load?	(yes)	no	7.1.2
FS4	Are the rise and fall times matched to within 10% for J→K transitions?	(yes)	no	7.1.2
FS5	Are the rise and fall times matched to within 10% for K→J transitions?	(yes)	no	7.1.2
FS6	Is a SE0 less than 14ns long ignored at all transitions in a bitstream?	(yes)	no	7.1.4
FS7	Is a SE1 less than 8ns long ignored at all transitions in a bitstream?	(yes)	no	
FS8	Does the device drive the J state at the end of an EOP for complete full-speed bit time?	(yes)	no	7.1.7
FS9	If the device tracks the K→low-speed EOP→J transition on its upstream port at the end of resume, does it correctly handle the low-speed EOP?	(yes)	no	7.1.7.5
FS10	Is the transmission data rate between 11.97 and 12.03Mb/s?	(yes)	no	7.1.11
FS11	Is the differential driver jitter for consecutive transitions less than ±2.0ns?	(yes)	no	7.1.13.1
FS12	Is the differential driver jitter for paired transitions less than ±1.0ns?	(yes)	no	7.1.13.1
FS13	Is the EOP width between 160ns and 175ns at the transmitter?	(yes)	no	7.1.13.2
FS14	Does the device accept an SE0 between 82ns and 250ns long, followed by a J, as an EOP?	(yes)	no	7.1.13.2 7.1.14
FS15	Does the receiver accept a packet whose first bit has been distorted by as much as ±25ns?	(yes)	no	7.1.14
FS16	Does the receiver accept a packet whose last bit has been lengthened by as much as 75ns?	(yes)	no	7.1.14 7.1.9
FS17	Is the receiver data jitter tolerance at least ±20.0 ns for consecutive transitions?	(yes)	no	7.1.15
FS18	Is the receiver jitter tolerance for paired transitions at least ±12.0 ns?	(yes)	no	7.1.15
FS19	Is the device's turn-around time between two and 6.5 full-speed bit times, or 7.5 bit times if the device has a fixed cable?	(yes)	no	7.1.18
FS20	Is the time-out period 18 full-speed bit times?	yes	(no)	7.1.19

FS21	Is D+ between 2.7 and 3.6V and D- between 0.0 and 0.3V when the bus is idle?	yes no	7.2.3

3 Signaling Protocol and Error Handling

3.1 Bitstreams

B1	Is the possibility of both D+ and D- registering as NIB 1 during bus transitions accounted for?	yes no	7.1.2 7.1.13.1
B2	Is the USB signaling either full-speed or low-speed but not both?	yes no	7.1.5
B3	Does the sense of USB signaling correspond to the signaling speed?	yes no	7.1.7
B4	Is the bitstream on the bus NRZI encoded?	yes no	7.1.8
B5	Is bit stuffing performed on all data transmitted, including CRCs, prior to NRZI encoding?	yes no	7.1.9 8.3.5
B6	Is bit stuffing performed even if the stuffed bit follows the last bit of a packet?	yes no	7.1.9
B7	Is NRZI to NRZ decoding done before bit unstuffing?	yes no	7.1.9
B8	Is bit unstuffing performed on all received data, including CRCs?	yes no	7.1.9 8.3.5
B9	Is bit unstuffing done before the bitstream is parsed?	yes no	7.1.9

3.2 Fields

A field is one of:

address	7 bit field
data	0 to 1023 byte field
data CRC	16 bit field
endpoint	4 bit field
EOP	3 bit field with NIB value 00J
frame number	11 bit field
PID	8 bit field, whose types are listed in section 8.3.1
SYNC	8 bit field with NZB value 00000001
token CRC	5 bit field

F1	Is the SYNC field, as measured on the bus wires, correct (NIB KJKJKJKK)?	yes no	8.2
F2	Are all PIDs used among those listed in Table 8-1?	yes no	8.3.1
F3	Are the PID check bits the ones complement of the packet type field?	yes no	8.3.1
F4	Are the CRC generator's contents inverted and sent to the checker MSb first?	yes no	8.3.5
F5	Is the token CRCs generated with the polynomial NZB 00101 on the ADDR and ENDP fields of IN, SETUP, and OUT tokens?	yes no	8.3.5.1
F6	If all bits are received without error, does the CRC computation on a token or SOF leave a residual of NZB 01100 at the EOP?	yes no	8.3.5.1
F7	Is the data CRC generated with the polynomial NZB 1000000000000101 on	yes no	8.3.5.2

	the data field of a data packet?		
F8	If all bits are received without error, does the CRC computation on the data field leave a residual of NZB 1000000000001101 at the EOP?	yes no	8.3.5.2

3.3 Packets

A packet can be one of the following:

packet	fields comprising packet
data	SYNC PID data data CRC EOP
handshake	SYNC PID EOP
PRE	SYNC PID
SOF	SYNC PID frame number token CRC EOP
token	SYNC PID endpoint token CRC EOP

P1	Are all token packets 32 bits long and followed by an EOP?	yes no	8.4.1
P2	Are all token packets of the form SYNC PID address endpoint token CRC EOP?	yes no	8.4.1
P3	Are all data packets an integral number of bytes long (4 to 1027) excluding the EOP?	yes no	8.4.3
P4	Is the data packet constituted as sync followed by PID followed by 0 to 1023 bytes of data followed by data CRC followed by EOP	yes no	8.4.3
P5	Are all handshake packets 16 bits + EOP?	yes no	8.4.4
P6	Are all handshake packets of the form SYNC PID EOP?	yes no	8.4.4
P7	Is the data payload of a low-speed packet limited to a maximum of 8 bytes?	yes no*	8.6.5
P8	Is the PRE packet 16 bits long?	yes no*	8.6.5
P9	Does the PRE packet consist of only a SYNC followed by a PID?	yes no*	8.6.5

3.4 Transactions

Transactions are sets of packets used for unidirectional data transfer. Transactions are discussed in detail in section 8.5 of the USB Specification.

TA1	Does an isochronous endpoint synthesize frame markers to replace SOFs which may be lost due to bus error?	yes no	5.10.6
TA2	Do handshakes conform to order of precedence described in section 8.4.5?	yes no	8.4.5
TA3	Does the generated packet comply with the flows show in Figure 8-9, 8-11, 8-13, or 8-14, as appropriate?	yes no	8.5 8.6.5
TA4	Is an unsuccessful (NAKed or timed-out in non-token phase) transaction retried?	yes no	8.6
TA5	Does the retried transaction use the same data PID as the original transaction?	yes no	8.6

3.5 Transfers

Transfers are data structures used by control endpoints. Each transfer is made up of setup and status stages, possibly with a data stage. Transfers can be one of:

setup0	*out1 out0 out1 ... out0/1*	in1
setup0	*in1 in0 in1 ... in0/1*	out1
setup0	in1	

Transactions in italics constitute the data stage. The suffix of 0 or 1 indicates the data PID used in the transaction.

TF1	Does the data stage always start with a data1 PID?	yes no	8.5.2
TF2	Are all the transactions of the data stage in the same direction?	yes no	8.5.2
TF3	Is there status stage's direction opposite that of the data stage?	yes no	8.5.2
TF4	Is the data packet used in the status stage zero bytes in length?	yes no	8.5.2

4 Recommended Questions

4.1 Device Robustness

4.1.1 Bitstreams

RB1	Is a single ended NIB 1 more than one bit time long ignored?	yes no	
RB2	Does an agent ignore a truncated (up to 90%) first bit of the sync field without impacting the rest of the bitstream?	yes no	
RB3	Is the state of the differential receiver ignored during single ended signaling?	yes no	
RB4	Does the target reject bitstreams less than one bit time long without impacting future transactions?	yes no	
RB5	Does the target adjust to the difference in frequency and phase between incoming clock and its internal clock?	yes no	
RB6	Is a packet with a bit-stuff error rejected by the target?	yes no	
RB7	Is a bitstream, which is not part of a packet, with bit stuff error ignored by the target?	yes no	
RB8	Does the target reject packets with bit stuff error at the last bit of the packet?	yes no	

4.1.2 Fields

RF1	Is the sync field recognized as valid even if the first two bits of it are corrupted? (Only the last 3 bits actually need to be decoded.)	yes no	
RF1	Is a packet with packet type not listed in Table 8-1 ignored by the target	yes no	
RF2	Is a packet with a corrupt PID (PID check error) ignored by the target?	yes no	
RF3	Is a token with a bad CRC ignored by the target?	yes no	
RF4	Is a CRC error on a data packet recognized by the target?	yes no	

4.1.3 Packets

RP1	Is a token whose address field doesn't match any address in the device ignored by the device?	yes no	
RP2	Is a token whose endpoint field doesn't match any endpoint in the address ignored by the device?	yes no	
RP3	Is a token which doesn't match the direction of its target endpoint ignored	yes no	

	by the device?		
RP4	Is a SETUP token to a unidirectional endpoint ignored by the device?	yes no	
RP5	Is every endpoint capable of handling zero length data packets in its assigned directions?	yes no	
RP6	Does an ISO endpoint use a zero length data packet if fresh frame data is not available?	yes no	
RP7	Is a packet whose length doesn't match the standard length for the packet type rejected by target?	yes no	
RP8	Does the measurement of packet length take into account the possibility of jitter and hub repeater skews in the EOP?	yes no	
RP9	Is a bitstream that does not constitute a valid packet rejected by the target?	yes no	
RP10	Are low-speed packets received by full-speed upstream ports ignored?	yes no	8.6.5

4.1.4 Transactions

RTA1	Do all pipes in the device return to normal operation when the device resumes from suspend?	yes no	
RTA2	Is a packet which doesn't fit the current phase of a transaction rejected by the target?	yes no	
RTA3	Does the receipt of a token always start a new transaction and end a pending transaction?	yes no	
RTA4	Is a data packet with same PID as the previous data packet to an endpoint ignored, other than ACKing the data packet?	yes no	
RTA5	Does a time-out or error in any phase cause the transaction to be terminated?	yes no	
RTA6	Is a transaction always started with a token?	yes no	
RTA7	Is the data toggle implemented independently for each unidirectional endpoint?	yes no	
RTA8	Does an isochronous data source ignore a handshake without impacting subsequent transactions?	yes no	
RTA9	Can consecutive packets in the same direction be handled , provided there are two or more bit times of interpacket gap between each packet?	yes no	

4.1.5 Transfers

RTF1	Does the receipt of a nonzero length data packet in the status stage cause the transfer to be terminated with an error indication?	yes no	

5 Explanations

This section should be used to explain any "no" answers or clarify answers on checklist items above. Please key entries to the appropriate checklist question.

FS20 : The device expecting the reponse will not timeout before 16 bits time but will time out before 18 bits times.

F2 : The PID Data2, MDATA, NYET, ERR, SPLIT, PING are not used. They are High Speed specific.

* P7. P8. P9 : reserved for Low Speed.

TA1 : not implemented

RB5 : The target adjust the phase.

RF1 : Only the first bit is rejected.

RTF1 : The host may only send a zero-length data packet in this phase but the function may accept any length packet as a valid status inquiry.

SUBJECT: AT91SAM7S64

DATE: 19 July 2005

USB 2.0 Certification Report

Customer:
ATMEL
ZI de Rousset
13106 ROUSSET
France

Device:
AT91SAM7S64
USBD0430
TID 40000036

Supplier:

Professional Multimedia Test Centre
Wetenschapspark 7
B-3590 Diepenbeek

Table Of Contents

1 Customer

ATMEL
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13106 ROUSSET
France
Tel : +33(0)4 42 53 61 49
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2 Supplied Hardware and Software

2.1 Assets

Description	Manufacturer	Model	Serial #
Device under test	ATMEL	AT91SAM7S64	0266
Backup Device	ATMEL	AT91SAM7S64	0668

2.2 Software

Description	Version
N/A	N/A

2.3 Test Procedures

Low/Full Speed Test Procedure	High Speed Test Procedure
1.3	N/A

3 Used measurement equipment by PMTC

Description	Manufacture	Identity	Serial NR	Calibration date	Calibration due date
Current Probe	Tektronix	TCP202	B019512	10-Feb-2005	10-Feb-2006
Probe	Tektronix	P6205	2600BCK	14-Feb-2005	14-Feb-2006
Probe	Tektronix	P6205	2600BCC	14-Feb-2005	14-Feb-2006
Digital real-time Oscilloscope	Tektronix	TDS654C	B020448	25-May-2005	25-May-2006
Digital Multimeter	Agilent	34401A	US36046603	16-Feb-2005	16-Feb-2006
Probe	Tektronix	P6245	3801GSW	10-Feb-2005	10-Feb-2006
Probe	Tektronix	P6245	3801GSX	10-Feb-2005	10-Feb-2006
Differential Probe	Tektronix	P6248	B012810	17-Feb-2005	17-Feb-2006
Data Generator	Tektronix/Sony	DG 2040	J300311	11-Feb-2005	11-Feb-2006
Digital real-time Oscilloscope	Tektronix	TDS694C	B011997	14-Feb-2005	14-Feb-2006

4 Summary of the performed test

Electrical Legacy

Signal Quality	*Pass*
Inrush	*Pass*

Device Framework

Chapter 9 full test (USBCV)	*Pass*

Power Measurements

Power Measurements Windows XP SP2	*Pass*
Back-Voltage	*Pass*

Golden Tree

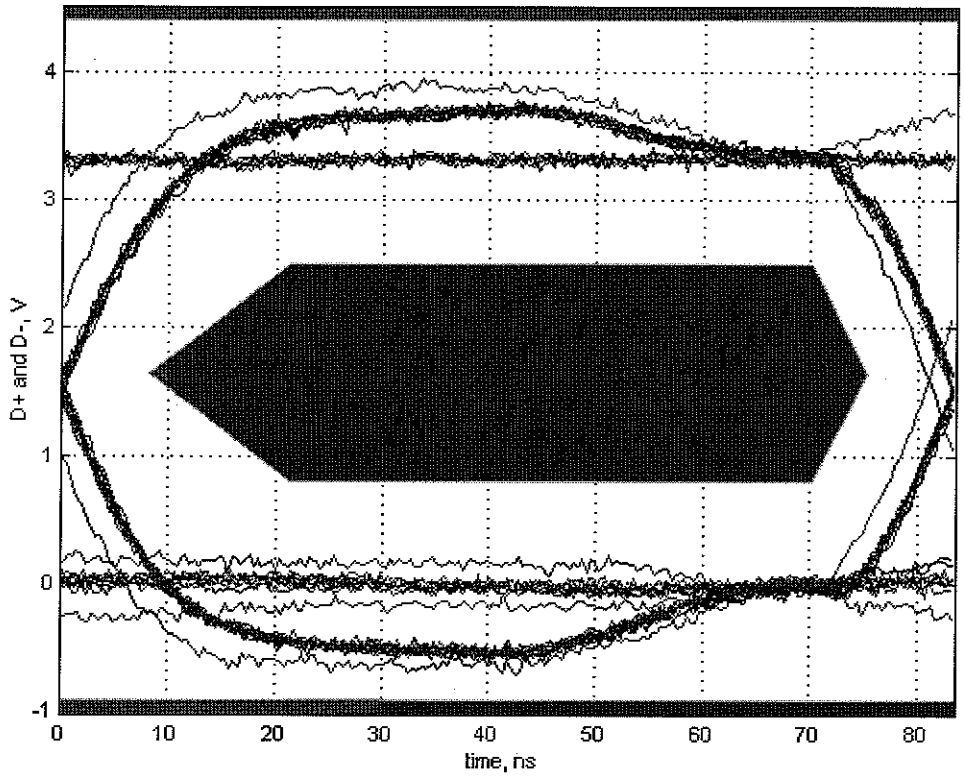
Interoperability Windows XP SP2	*Pass*

5 Results

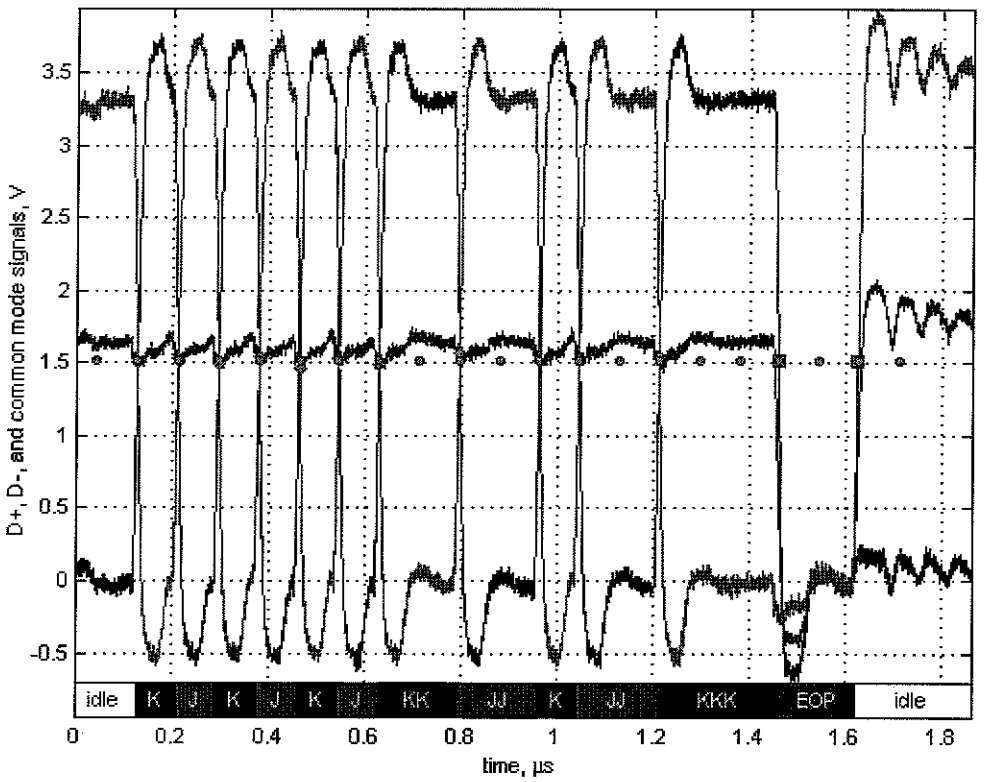
5.1 Electrical

5.1.1 Upstream Full Speed Signal Quality

The AT91SAM7S64 passed the Full speed Upstream Signal quality test in Bus Powered mode.



Signal Eye



Data and Common Mode Voltage

Comments:

Overall result: pass!

Signal eye:

Eye passes

EOP width: 166.17ns

EOP width passes

Receivers: reliable operation on tier 6

Receivers pass

Measured signaling rate: 11.9798MHz

Signal rate passes

Crossover voltage range: 1.47V to 1.57V, mean crossover 1.52V
(first crossover at 1.51V, 10 other differential crossovers checked)

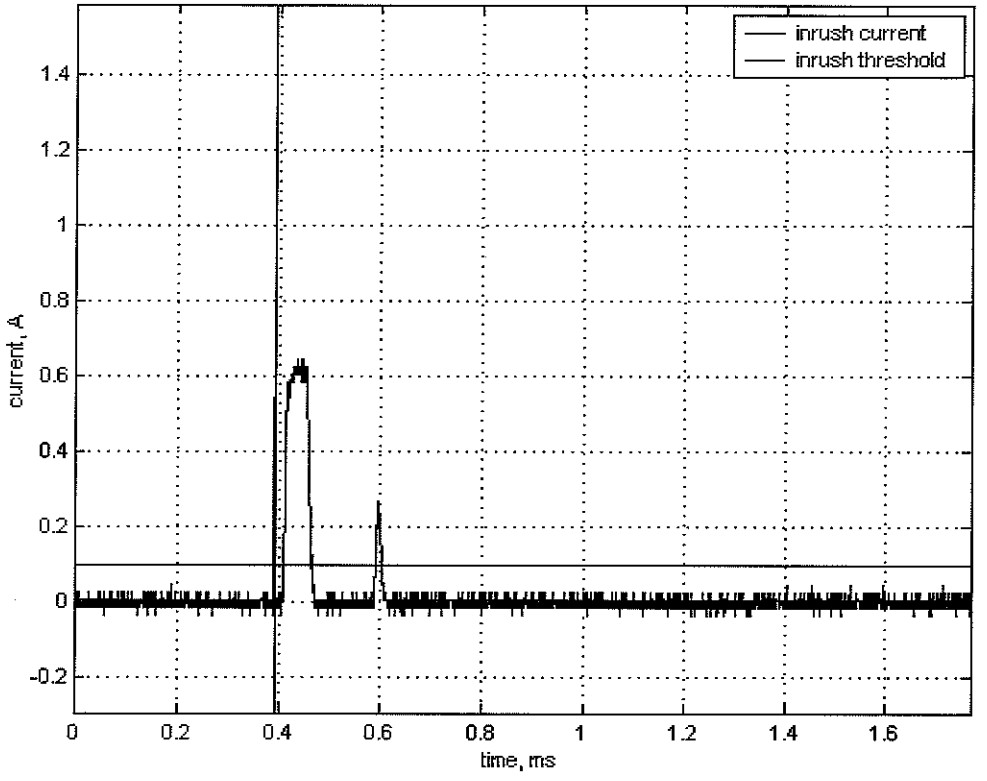
Crossover voltages pass

Consecutive jitter range: -0.4ns to 0.4ns, RMS jitter 0.2ns
Paired JK jitter range: -0.4ns to 0.5ns, RMS jitter 0.3ns
Paired KJ jitter range: -0.4ns to 0.3ns, RMS jitter 0.2ns

Jitter passes

5.1.2 Inrush Current

The measured Inrush current of the AT91SAM7S64 is 25,84µC. The USB spec allows up to 10µF to be hard started, which represents an allowed load of approximately 50µC. With a measured load of 25,84µC, the AT91SAM7S64 Passed the Inrush current test.



Inrush Current

5.2 Device Framework

The following tests where performed using the USBCV 1.2.1 test tool.

5.2.1 Chapter 9 full test

The AT91SAM7S64 Passed the Chapter 9 test USBCV 1.2.1.

Full Speed

Description	Value
Vendor ID	3eb
Product ID	6125
CFG 's	1
Interfaces	1
USB Spec.	2.0
Max. Power	200 mA
Result	Pass

5.3 Power Measurements

5.3.1 Windows XP SP2 Power Measurement

The AT91SAM7S64 passed the power measurement tests.

5.3.1.1 Bus Powered

Device State	Measurement	Status
Unconfigured State	22,7 mA	**Pass**
Configured State	22,7 mA	**Pass**
Operating State	25 mA	**Pass**
Suspended State	360 µA	**Pass**
Suspend support		**Yes**

5.4 Back voltage

The AT91SAM7S64 passed the Back Voltage test.

	DC Voltage Before enumeration	DC Voltage after enumeration and removal
Vbus	0 mV	0 mV
D+	0 mV	0 mV
D+	0 mV	0 mV

5.5 Golden Tree (Interoperability)

For more information about the test guides used by PMTC, please see the USB-IFTestProc1_3.pdf file that can be found at http://www.usb.org/developers/docs.

5.5.1 Windows XP SP2 Interoperability

The AT91SAM7S64 passed the Gold Tree tests.

Test No.	Test description	Result
1	Enumeration and driver installation test on EHCI	Pass
2	DUT demonstrates correct operation using default drivers	Pass
3	Update driver	N/A
4	Install software	N/A
5	Demonstrates functionality with updated driver and/or application	N/A
6	Verify the operating speed of the DUT	Pass
7	Interoperability (operate all the devices in Gold Tree)	Pass
8	Hot Detach & Reattach	Pass
9	Topology change	Pass
10	Warm boot	Pass
11	Cold boot	Pass
12	Active S1 Suspend	Pass
13	Active S1 Resume	Pass
14	Inactive S1 Suspend	Pass
15	Inactive S1 Resume	Pass
16	Active S3 Suspend	Pass
17	Active S3 Resume	Pass
18	Enumeration test on UHCI	Pass
19	Interoperability (operate all the devices in Gold Tree)	Pass
20	Hot Detach & Reattach	Pass
21	Topology change	Pass
22	Warm boot	Pass
23	Cold boot	Pass
24	Active S1 Suspend	Pass
25	Active S1 Resume	Pass
26	Inactive S1 Suspend	Pass
27	Inactive S1 Resume	Pass

28	Active S3 Suspend	Pass
29	Active S3 Resume	Pass
30	Enumeration test on OHCI	Pass
31	Interoperability (operate all the devices in Gold Tree)	Pass
32	Hot Detach & Reattach	Pass
33	Topology change	Pass
34	Warm boot	Pass
35	Cold boot	Pass
36	Active S1 Suspend	Pass
37	Active S1 Resume	Pass
38	Inactive S1 Suspend	Pass
39	Inactive S1 Resume	Pass
40	Active S3 Suspend	Pass
41	Active S3 Resume	Pass
42	Enumeration test on EHCI (PCI card)	Pass
43	Active S3 Suspend	Pass
44	Active S3 Resume	Pass

Driver information:

Microsoft Windows XP SP2 Mass Storage Class drivers

6 Other PMTC services

PMTC, Your hardware test centre.

PMTC operates as an independent Belgian based test centre for the validation and release of multimedia peripheral equipment and interfaces.

PMTC offers a wide range of testing activities an has become a professional test centre for numerous companies all over the world, a test house known for its quality of testing and its dynamic approach.

Thanks to the independence of the test laboratories, PMTC is ideally placed to offer an objective, third party opinion on overall quality of the products in development.

Currently, PMTC's experience is located in the following application areas:

Services:
- Alpha Testing
- Beta Testing
- Pre-WHQL Testing
- Compatibility Testing
- Functionality Testing
- Localisation Testing
- Spec Compliance
- Consultancy

Technologies:
- Optical Storage drives
- Firewire Certification
- PC, MAC systems and peripherals
- USB
- USB On-The-Go
- Mount-Rainier
- Bluetooth
- WIFI
- ...

Tools:
- Ch8ck tool
- Traffic Lab

Please visit our web site at http://www.pmtc.be for detailed information regarding PMTC's testing services

Revision History

Doc. Rev	Comments	Change Request Ref.
6213A	08-Nov-05 First issue 06-Feb-06 WEB	

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