Putting Adaptive Constant-ON-Time Buck ICs and Modules to Work in Inverting Buck-Boost Converters

Introduction

The inverting buck-boost converter is used in many applications to generate a local non-isolated negative voltage starting from a positive bus voltage. This topology is shown in Figure 1. A wide variety of application notes and reference designs addresses the implementation of this converter using PWM buck controllers and regulators, both synchronous and non-synchronous[1,2,3].

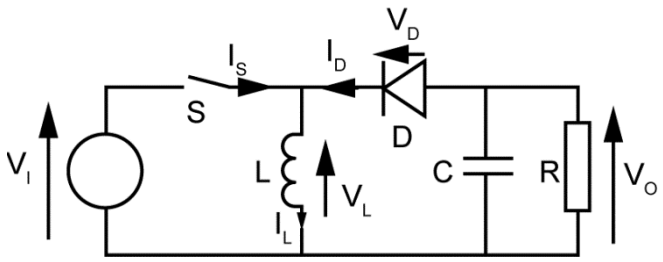

Figure 1. Buck-boost Converter

Despite the applicability of buck converter ICs for inverting buck-boost topology, the buck-boost converter's dynamics are very different from those of the buck converter. In the buck-boost, energy is transferred from the inductor to the output only during the OFF time of the active switch (S). This introduces the well-known Right Half-Plane Zero (RHPZ) in the control-to-output transfer function, as explained in detail by Lloyd Dixon[4]. The RHPZ is not suppressed by current-mode control. Consequently, compensation design for PWM converters in the inverting buck-boost topology must set the loop-gain crossover frequency low enough to be no-influential to the phase shift associated with the RHPZ.

Notes:

1. John Tucker, "Using a buck converter in an inverting buck-boost topology" - http://www.ti.com/lit/an/slyt286/slyt286.pdf
2. Matthew C. Kessler, "Designing an Inverting Buck Boost Using the ADP2300 and ADP2301 Switching Regulators" - http://www.analog.com/static/imported-files/application_notes/AN-1083.pdf
3. http://www.ti.com/tool/PMP3143
4. Lloyd Dixon, "The Right-Half-Plane Zero — A Simplified Explanation," Unitrode Seminars SEM-500.

It is suggested to apply a Constant ON-Time (COT) buck IC in this topology. The fact that energy only flows to the output during the active switch OFF time goes against the basics of COT control of the buck converter. Refer to Figure 2:

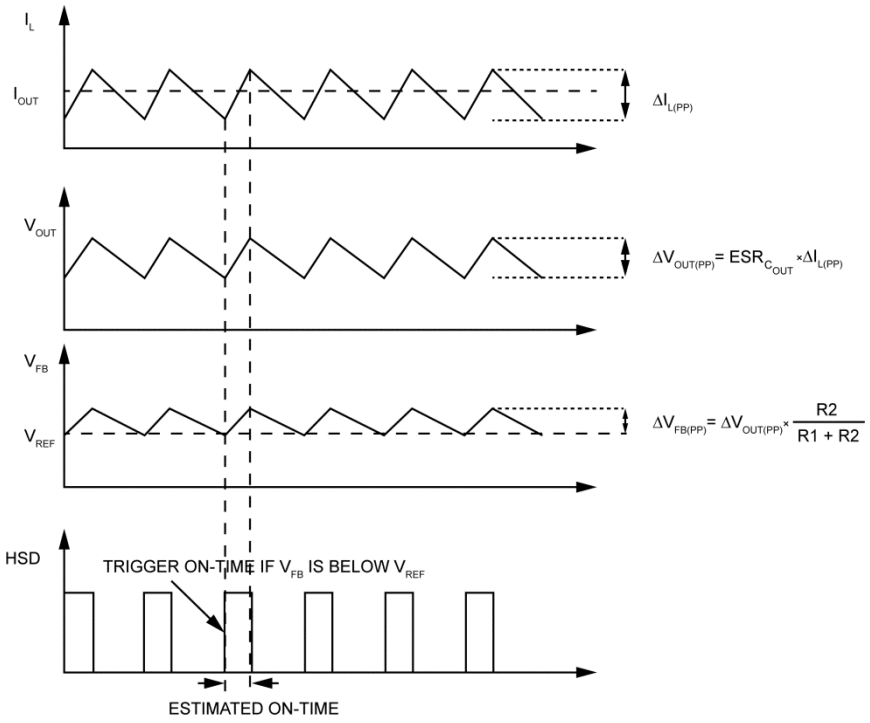

Figure 2. COT control waveforms in a Buck converter

In the COT control for buck converter, the threshold crossing of the *falling* output ripple waveform invokes a new active switch ON-time when the V_{FB} waveform crosses the regulation voltage V_{REF}. When the active switch is OFF, the output ripple waveform is expected to decrease until it eventually crosses the regulation threshold. Unfortunately with the buck-boost converter, the output ripple waveform as seen by the IC at the FB pin increases during the active switch OFF time. This is shown in the following Figure 3.

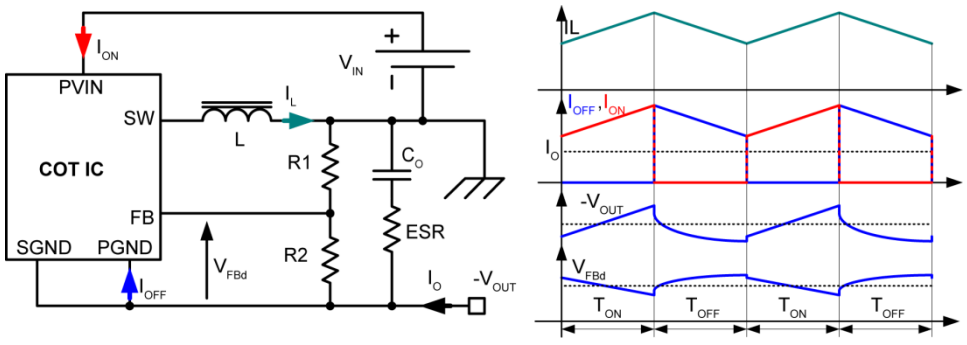

Figure 3. Buck-boost current and Voltage Ripple waveforms

Output ripple suppression and artificial ripple injection

The first step is to suppress the output ripple feed at the FB pin. This requirement calls for a relatively large, low-ESR output capacitor. Ceramic capacitors, which are often used in parallel with polarized capacitors, are the most effective due to their high-frequency characteristics which entail very low ESR and ESL. When using the buck-boost topology, adding some ceramic output capacitors is necessary, since the current in the output loop is discontinuous (see Figure 3). This differs from the buck converter running in continuous conduction mode, where the output loop current is continuous with some amount of superimposed AC ripple. Without a good high-frequency output ceramic capacitor, the output voltage ripple in the inverting buck-boost converter would be unacceptably large.

Once the output ripple appearing at the FB pin has been suppressed, the next step is to leverage the well-known ripple self-injection technique. An example of implementing this technique when there is a nearly insignificant level of output ripple is illustrated in the MIC2165 datasheet. Figure 4 shows the implementation of ripple self-injection in the inverting buck-boost topology (R_{INJ}, C_{INJ} and integration capacitor C1) and its effect on the waveform seen by the IC (V_{FBd}, differential signal taken between FB and SGND).

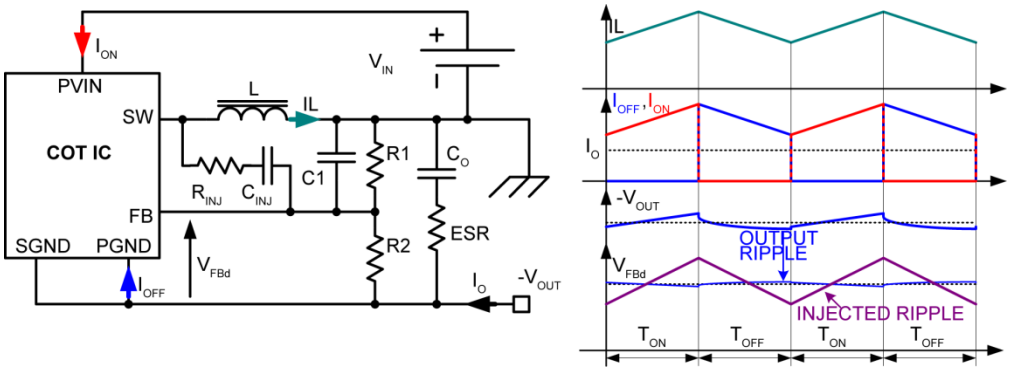

Figure 4. COT Inverting Buck-boost waveforms with predominant ripple self-injection

Because of the predominant self-injected ripple waveform (see Figure 4), the FB ripple wave-shape has the correct phase to allow the COT buck controller engine to work properly in the buck-boost topology. The self-injected ripple must be large enough to satisfy stability and controller-specific FB ripple amplitude requirements, as well as overcome any residual output voltage rippling that may have the wrong phase.

Figure 5 shows actual waveforms of the switch node (Ch1) and the feedback ripple signal ($V_{FBd;}$ Ch3, AC-coupled) when tested by a buck regulator IC (MIC24051) in an inverting buck-boost configuration. The slope of the FB waveform has indeed the *right* slope for proper operation of the buck COT control.

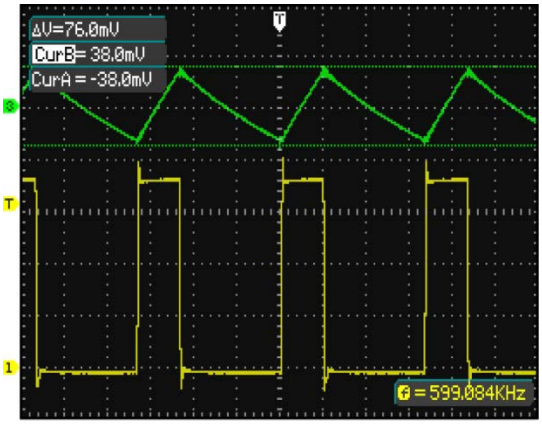

Figure 5. SW and FB ripple waveform in a MIC24051-based inverting buck-boost with ripple self-injection ($12V_{IN}$, $-5V_{OUT}$, no load, signals referred to $-5V_{OUT}$)

Pseudo-Constant Switching Frequency Operation

The COT control can also be made a pseudo-constant-frequency during steady-state operation by means of a suitable implementation of the T_{ON} timer. The concept is described in various product datasheets and related literature such as the MIC24051 datasheet. This concept is often referred to as “Adaptive Constant-ON-Time Control”.

The basic idea is to calculate the T_{ON} as to emulate the duty cycle of a fixed-frequency buck controller. This method is inherently topology-dependent, as it relies on the duty cycle formula for the particular topology being considered. Various proprietary methods also improve the frequency stability against load variations, by compensating the duty cycle increase determined by circuit inefficiencies. The conceptual implementation of the Adaptive COT control is illustrated in Figure 6.

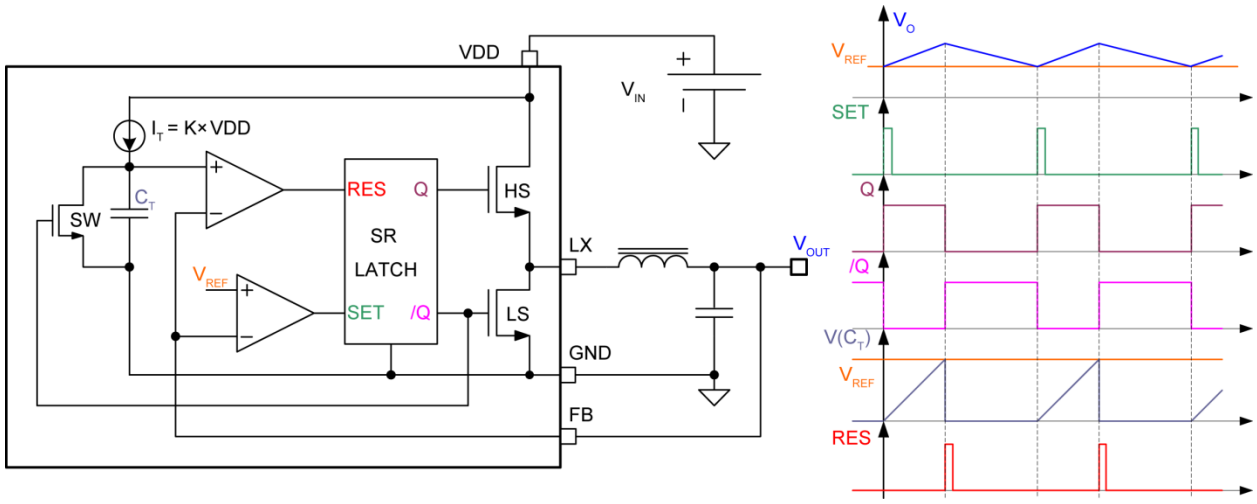

Figure 6. Pseudo-Constant-Frequency, Adaptive Constant-ON-Time Control Scheme

Despite the fact that the basic adaptive constant-on-time generator implementation is topology-dependent, the adaptive COT buck control engine will maintain its pseudo-constant-frequency characteristics when it’s used in an inverting buck-boost topology. Additionally, the steady-state switching frequencies also remain the same in an inverting buck-boost topology, for the same input and output voltages as seen by the IC.

The steps of the analysis are detailed in Figure 7. The analysis concludes that the switching period in both topologies is independent from the input (V_{IN}) and output voltages (V_O), and it is determined solely by internal IC parameters of the T_{ON} generator (timing capacitor C_T and voltage-controlled current-source trans-conductance k).

The analysis presented in Figure 7 is a classic, simplified model of the Adaptive COT control. It does not take into account any duty cycle corrections for losses compensation. More sophisticated T_{ON} generators typically rely on different, proprietary methods for duty cycle generation in presence of losses. In practice, when a load is applied, some differences may appear between the steady-state switching frequencies in the two topologies because of the loss compensation mechanism.

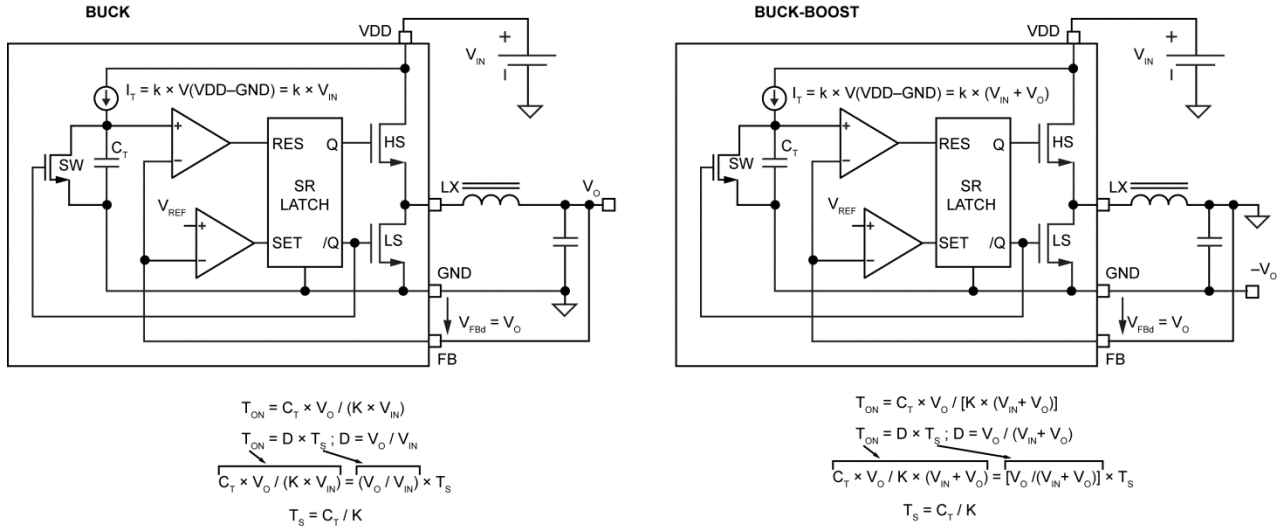

Figure 7. Analysis and Comparison of Adaptive COT control switching period in the Buck and Inverting Buck-Boost topologies

To verify this analysis, hook up a modified MIC24051 Evaluation Board in buck and inverting buck-boost configuration and compare the switching frequency values when the total voltage (V_{IN} to SGND) are the same, at no load. See the graph in Figure 8 for switching frequency numbers.

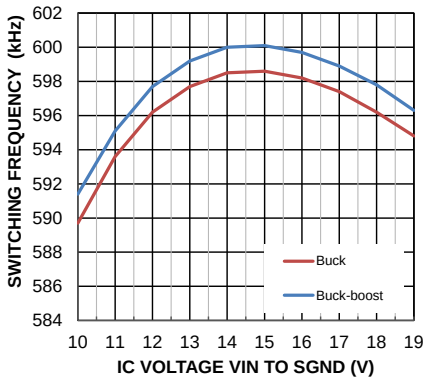

Figure 8. MIC24051 Measured Switching Frequency in Buck and Buck-Boost configuration vs. VIN to SGND voltage, at no load

For a quick evaluation of a buck Adaptive COT IC in the inverting buck-boost topology, use a standard buck Evaluation Board with slight modifications and some warnings. This basic idea is shown in Figure 9. Instead of connecting the power supply V_{IN_SYS} between the board VIN and GND, connect the power supply between the board VIN and VOUT while the negative output voltage system rail ($-V_{OUT\_SYS}$) is obtained at the board GND. This method was used to obtain a fair comparison between the switching frequencies in the two different topologies, i.e. the same board was hooked up in buck and inverting buck-boost configuration.

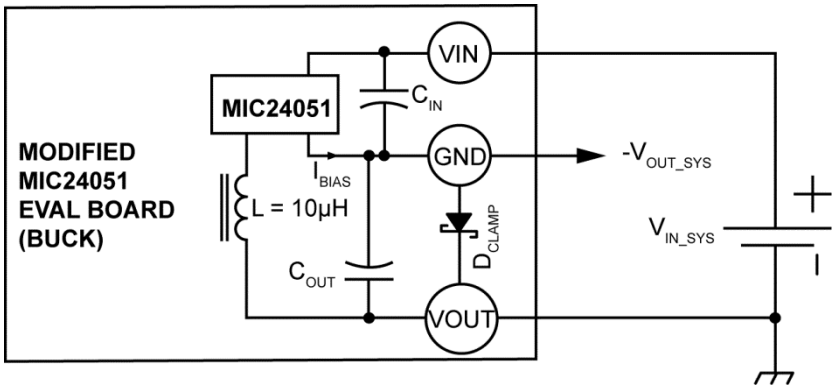

Figure 9. MIC24051 buck Eval Board hookup for quick evaluation in the inverting Buck-Boost topology

All the input-side components of the buck Eval Board, including the IC and the input capacitors (C_{IN}), will be exposed to the sum of the input voltage and the absolute value of the output voltage. For example, in a 12V to –5V inverting buck-boost configuration, all components that are connected between the board VIN and GND will see 12V + 5V = 17V, not just 12V. Another thing to note is that when the converter is disabled, any bias current, including the IC bias current (I_{BIAS}), that flows into the board GND node will tend to raise the system negative output voltage rail $-V_{OUT\_SYS}$ above the system 0V. In order to prevent damage of any polarized output capacitors added on the Eval Board (C_{OUT}) or at system level or the load itself, a small clamping diode D_{CLAMP} (preferably a Schottky, for its low V_F) should be connected as shown in Figure 9.

There is a subtle overshoot phenomenon, which is most evident when the V_{IN_SYS} supply is ramped down quickly and no load is present at the output ($-V_{OUT\_SYS}$). This is dependent on the V_{IN_SYS} ramp-down rate, the particular regulation voltage $-V_{OUT\_SYS\_NOM}$, and IC characteristics such as the Under-Voltage Lock-Out threshold (UVLO). This is outlined in Figure 10.

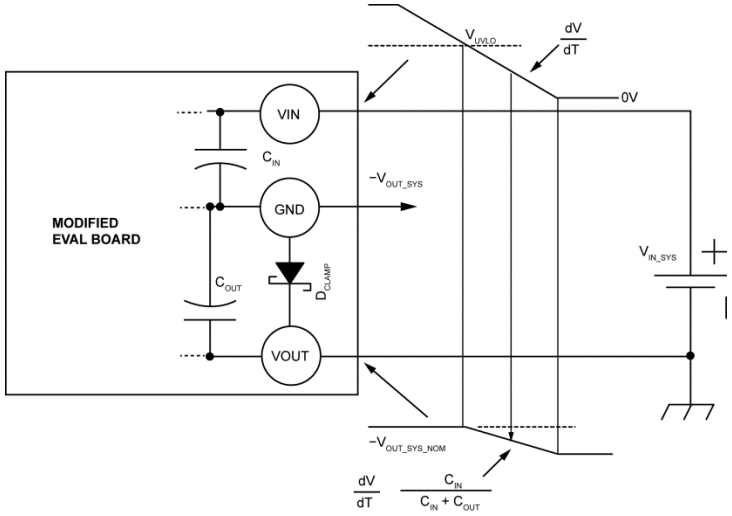

Figure 10. Output overshoot during VIN_SYS ramp-down at no load

At some point during the falling V_{IN_SYS} ramp, the falling threshold of the IC UVLO is crossed (V_{UVLO} level). The IC stops switching and its output stage becomes high-impedance, which removes its regulation capability and reduces the bias current to a lower level. From this point, the C_{IN} and C_{OUT} capacitors become the lowest impedances in the circuit and the scaled, falling V_{IN_SYS} ramp is impressed by the C_{IN}-C_{OUT} capacitive divider onto the output $-V_{OUT\_SYS}$. This causes it to go even lower than the target regulation voltage $-V_{OUT\_SYS\_NOM}$. The amount of energy that can be dumped during this transient is limited. Only a very small load is needed to sufficiently mask this effect.

Aside from the addition of a sufficient amount of ceramic capacitance at the output for ripple suppression, the inductor value/rating may need some adjustment for inverting buck-boost operation. Depending on the duty cycle value, the output current capability of the board has to be de-rated due to the average inductor current being necessarily higher that the DC output current in the buck-boost topology. Some level-shifting of the Enable and Power-Good signals might be needed at system level. Please reference Allag[5] for details.

Note:

5. Tahar Allag, Chris Glaser, “Using the TPS6215x in an Inverting Buck-Boost Topology” - http://www.ti.com/lit/an/slva469c/slva469c.pdf

Conclusion

Any Adaptive COT control based buck IC can be applied to the inverting buck-boost topology by following the guidelines presented in this application note.

At first-order approximation, the steady-state pseudo-constant-frequency property of the Adaptive COT control designed for buck will be maintained even in the inverting buck-boost topology. The no-load nominal switching frequency values will be the same in both configurations, for the same input and output voltages as seen by the IC.

A wide choice of Adaptive COT buck ICs, in controller, regulator and even module solutions are available from Micrel Inc., and the existing Evaluation Boards for the buck topology can be quickly adapted to check the performance of the circuit in the inverting buck-boost configuration.

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Revision History

Date	Change Description/Edits by:	Rev.
01/20/15	Initial release of application note. Submitted by P. Nora. Edited by D.Tanabe.	1.0